MCA
DISCOVISION®

MCA VIDEO DISC PLAYER
MODEL PR-7820

SERVICE MANUAL

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ABBREVIATION LIST

ABBREVIATION	FULL NAME
HEAD	Head Amplifier
VDEM	Video Demodulator
AUDB	Audio Board
ACOM	Audio Compensator
FOCS	Focus Servo
TRKG	Tracking Servo
CARG	Carriage Servo
SPDL	Spindle Servo
VTBC	Video & Time Base Corrector
MCPR	Micro Processor
DSPL	Character Display
D & CR	Data & Clock Recovery
STPM	Stop Motion
MIRB	Main Infrared Board
SIRB	Sub Infrared Board
LMPD	Lamp Driver Board
DADT	Data Detector Board
COMB	Control Mother Board
FTMB	Focus & Tracking Mother Board
CLMB	VTBC & Mother Board
SYPS	System Power Supply
LSPS	Laser Power Supply
CUST	Current Stabilizer
FFMP	Fuse & Focus Motor Protector
PHDB	Photo Detector Board
PFCB	Platform Connector Board
NFPB	Noise Filter Printed Board
LMP1	Lamp Board 1
LMP2	Lamp Board 2
LMP3	Lamp Board 3
RAMB	Ram Board
RFMD	RF Modulator
DOS	Dropout Sensor
TTL	Transistor Transistor Logic
ACS	Audio Compensator Signal
RAM	Randam Access Memory
ROM	Read Only Memory
NRZ	Non Return to Zero
CCD	Charge Coupled Device
VCO	Voltage Controlled Oscilator
PLL	Phase Lock Loop
PWM	Pulse Width Modulation
VDP	Video Disc Player
CAV	Constant Angular Velocity
CLV	Constant Line Velocity
D-A	Digital to Analogue
O/L	Open Loop
C/L	Close Loop

1. SPECIFICATIONS

Video Characteristics

Video response	NTSC specification (exclusive of de-emphasis).
Video output	75 ohm, unbalanced, sync negative; BNC type connector; 1 V P.P. terminated.

Audio Characteristics

Player audio output	Two channels; stereo, or two individual monaural channels with output to two RCA stereo jacks.
Audio output impedance	Less than 1.0K ohm unbalanced.
Audio output level	1.0 volt nominal.
Player audio distortion	Less than 0.5%.
Player audio frequency response.	40Hz to 20kHz ± 3dB

Functions

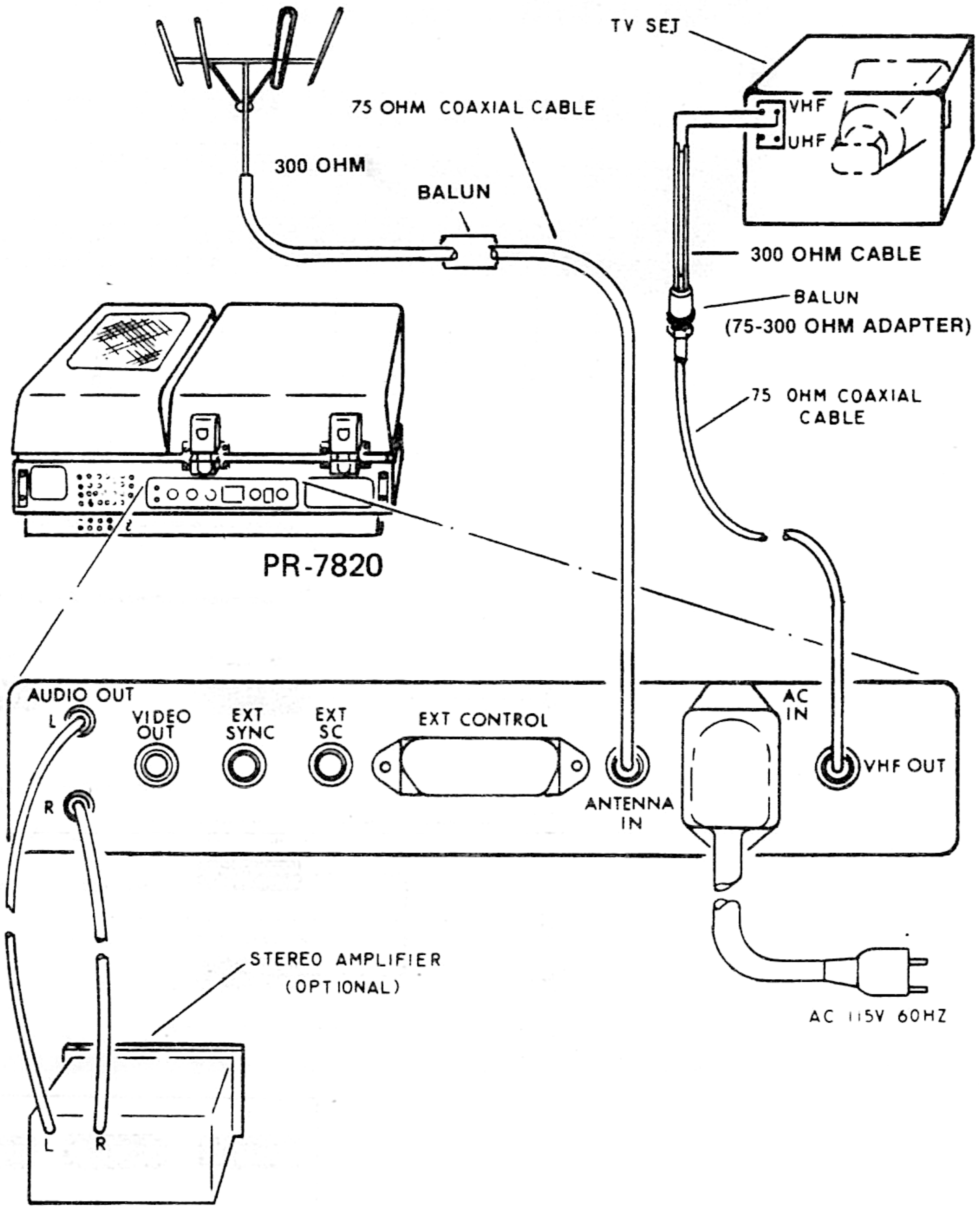
	Single frame step; Forward and reverse.
	Audio channels selectable; either, both, or neither.
	Selectable video display of frame numbers.
	Microprocessor control and storage per MCA, Disco-Vision specification.
	Interchangeable wireless or Remote control; Interchangeable wireless or hardwire to player.
	Cable of multi-player or external synchronization with 3.58MHz subcarrier and composit sync.
	Capable of control by external computer.
Fast scan (90mm travel)	15 sec. maximum.
Average search time	5 sec.
Slow motion	Variable control from 30 frames per sec to stop. Single frame display (freeze frame) with number lock.
Power requirements	115 VAC 60Hz
Power consumption	130 watts maximum
Weight	25kg maximum
Laser	6328 angstrom He-Ne
Dimension	570 x 448 x 191 (mm)

2. CONNECTION DIAGRAM

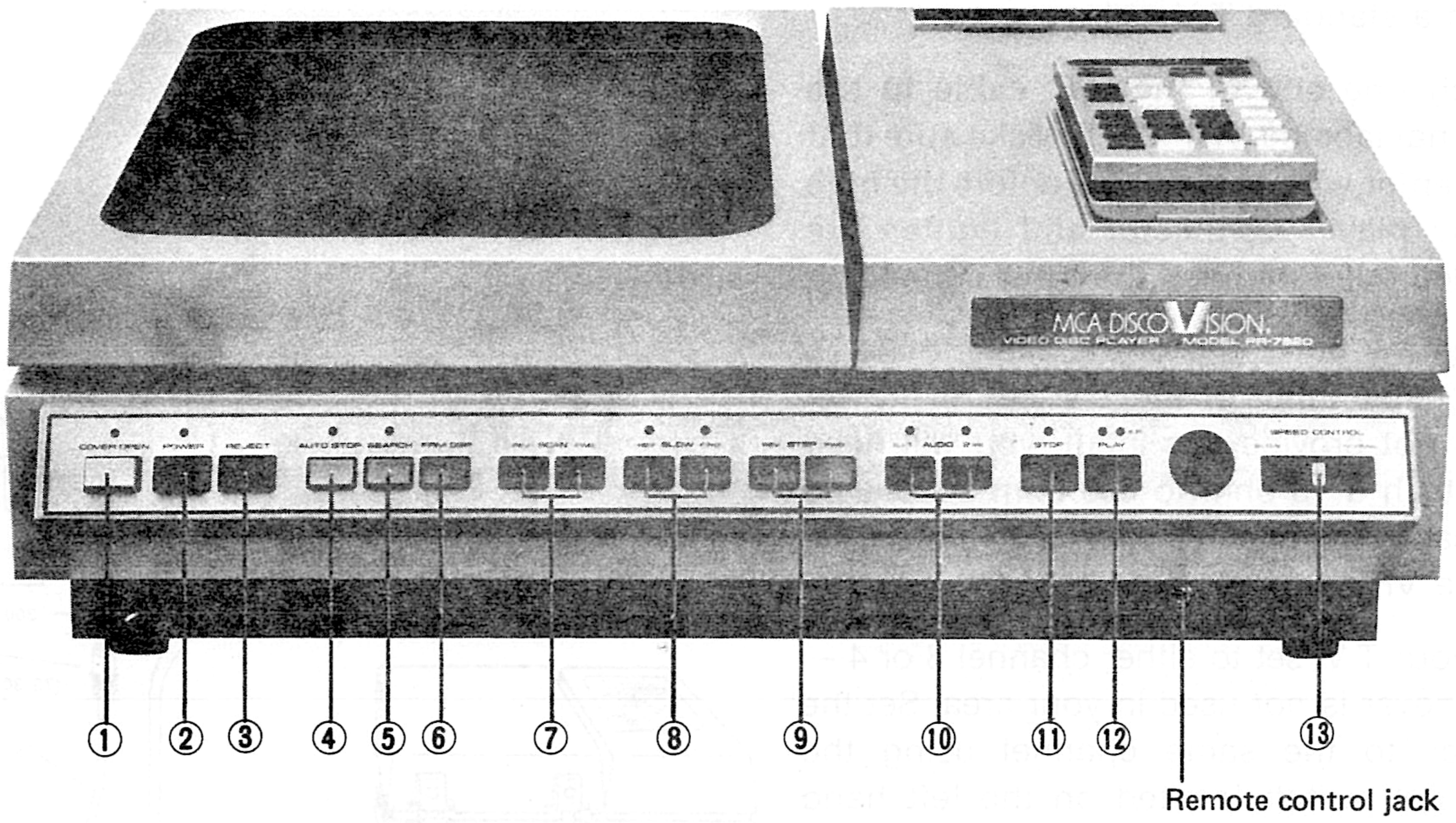
STANDARD T.V. SET SYSTEM

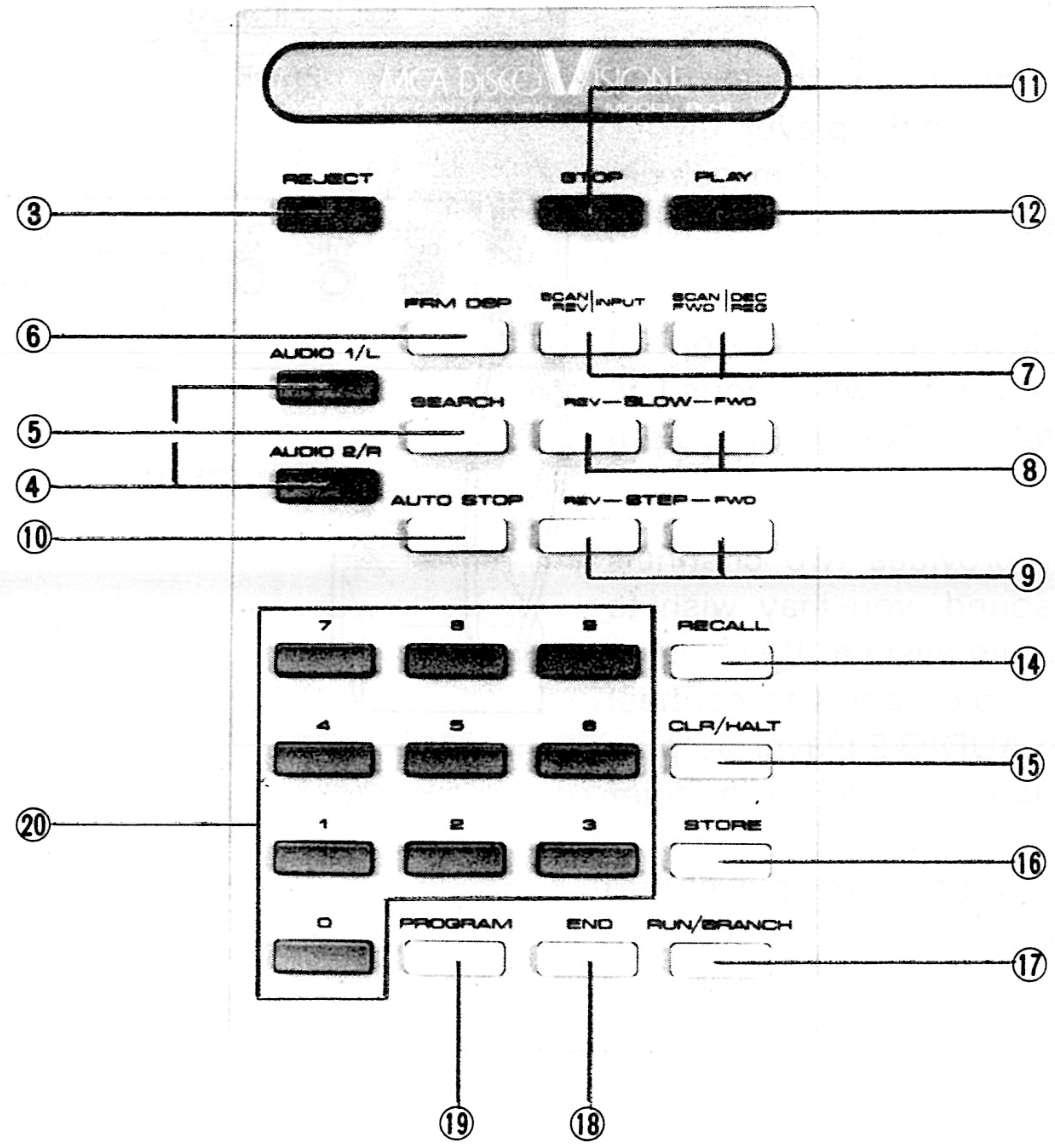
Figure shows how to connect the player for use with a standard T.V. set.

1. Attach one end of the R.F. cable to the terminal labeled VHF OUT. Make sure that the center wire of the cable enters the hole in the player connector and tighten the knurled outer barrel of the cable connector.
2. Attach the other end of the cable to the 75 ohm cable input of the T.V. set. If the set does not provide this input, you will need to attach a 75 ohm to 300 ohm adapter to the cable and attach the leads of the adapter to the VHF antenna screws of the T.V. set.
3. Set your T.V. set to either channel 3 or 4 — whichever is *not* used in your area. Set the player to the same channel using the channel switch located on the left hand side of the player.
4. Connect your T.V. antenna to the terminal labeled ANTENNA IN on the player. If your antenna lead-in is not a 75 ohm coaxial cable you will need a 300 ohm to 75 ohm adapter.
5. A switch on the lower left of the front of the player permits you to switch your T.V. to either the antenna (TV) or the output of the player (VDP).
6. Since the player provides two channels of high fidelity sound, you may wish to use a separate audio system. If so, use a pair of standard audio cables to connect the AUDIO 1 and AUDIO 2 player outputs to the auxilliary inputs of a stereo amplifier or receiver.
7. Plug the AC line cord from the player into a 115 VAC 60 HZ outlet.



3. FRONT PANEL FACILITIES





① COVER OPEN:

Press to open the cover. Close the cover by gently it downward by hand.

② POWER:

Power switch

③ REJECT:

a. This button starts the "soft reject" where the player squelches both video and audio and moves the disc at scan speed until it reaches the outside limit; here the mode changes to "hard reject" and continues to park position. The "soft reject" mode can be terminated by a play command or a scan fwd/rev command. Loss of focus during "soft reject" mode will cause the player to go into "hard reject."

b. When the cover is needed to be opened the "REJECT" button must be pressed to have the disc to move to park position. And then "cover open" button must be pressed.

④ AUTO STOP:

Plays to the frame number in the display memory register, at which time stop mode is initiated. If the number in the memory is smaller than the displayed frame number, search is initiated.

⑤ SEARCH:

Searches out the frame number in the display memory register. Audio and video squelched during search. Stop mode initiated at the conclusion of search with number lock to keep selected frame displayed.

⑥ FRM DSP:

Turns frame numbers on or off without affecting player functions.

⑦ SCAN FWD/REV:

a. From play — Rapidly traverses forward or reverse for the the duration the button is depressed. After the button is released the play mode is resumed. Audio is squelched during scan. If scan continues into the limits," stop mode will be initiated and locked in. To unlock this mode, reverse motion must be made outside the anticipated limits and a new command given.

b. From slow motion — Same as for play, except slow motion mode is restored after command is terminated.

c. From auto stop — Same as play, except Stop mode is initiated after scan mode is completed.

d. From search — Same as play and stop command is set.

⑧ SLOW FWD/REV:

From play, stop, auto stop, search — Terminates previous command and the frames are advanced forward or reverse at a rate determined by the slow motion control on player front panel. Audio is squelched. Continuous until a new command is given or limits are reached. See scan mode.

⑨ STEP FWD/REV:

a. From play, slow motion, auto stop, search — Generates stop mode and steps to the next frame forward or reverse for each depression of button.

b. From stop — Steps forward or reverse to the next frame.

⑩ AUDIO 1, AUDIO 2:

Independent control of either channel by toggling action to turn channel 1 and 2 on or off.

⑪ STOP:

From play, auto stop, search, slow motion — Motion will stop and current frame will be displayed indefinitely. Audio will be squelched. Previous function is cancelled. There is a number lock function to keep the selected frame displayed.

⑫ PLAY:

The only functioning control in park position except for Audio 1 and 2.

a. From park — Applies power to the spindle motor for about 4–6 sec. to allow spindle to reach normal speed. The disc is then rapidly (fast speed) positioned to the "anticipated inside limit" at which point the disc continues at "slow" speed until the "inside limit" is reached. At that point the carriage sits "idle" and waits for focus to be acquired and spindle servo locked. Then the carriage drive moves the disc at slow forward speed to position at the "anticipated inside" or program start. The carriage speed reduces to 50μm/sec (play speed) and the tracking loop closes. The player will remain in play mode until the "outside limit" is reached or END OF PROGRAM. At this point the reject mode is automatic.

b. From stop, auto stop, search, slow motion — Will go into play mode cancelling previous command.

c. From reject — Only during "soft reject" will the play button have any control. The player will start from the middle of the "play from park cycle" and will begin to play from START OF PROGRAM.

⑬ SPEED CONTROL:

Variable speed slow motion. Varying from normal 30 frames per second to 1 frame per minute.

⑭ RECALL:

Recall depressed after some other function was used. Will recall the last R = (location) without incrementing. Thereafter, recall will increment R = (location) each time it is depressed.

If a number is entered into the display memory register and recall depressed, then the memory location will correspond to the number entered and the display memory register will contain contents of this location.

⑮ CLR/HALT:

In addition to the function, this button will stop execution of the user program. It can be used in the user program as a halt statement to stop execution of the program at a pre-determined point.

⑯ STORE:

Stores the number in register display memory into memory location indicated R = (location) and advance R = (location) to the next location.

In absence of an input to the display memory register, the current frame number will be stored in successive memory location.

NOTE:
Frame numbers may be stored without the number display.

⑰ RUN/BRANCH:

From normal player mode this button causes execution of the user program, starting from step zero. If a # preceeds this button, execution will start at that step. If this button is pushed in the "write program" mode, its effect will be the same as a program "go to" when the "run program" mode is entered or when a branch is executed, the frame # display will be cleared and register # 1 will be indexed.

⑱ END:

This button causes termination of the "write program" mode. If when in the "write program" mode, its is desirable to index a distant program step; this button must be pushed first, then the step # , then the program button.

⑲ PROGRAM:

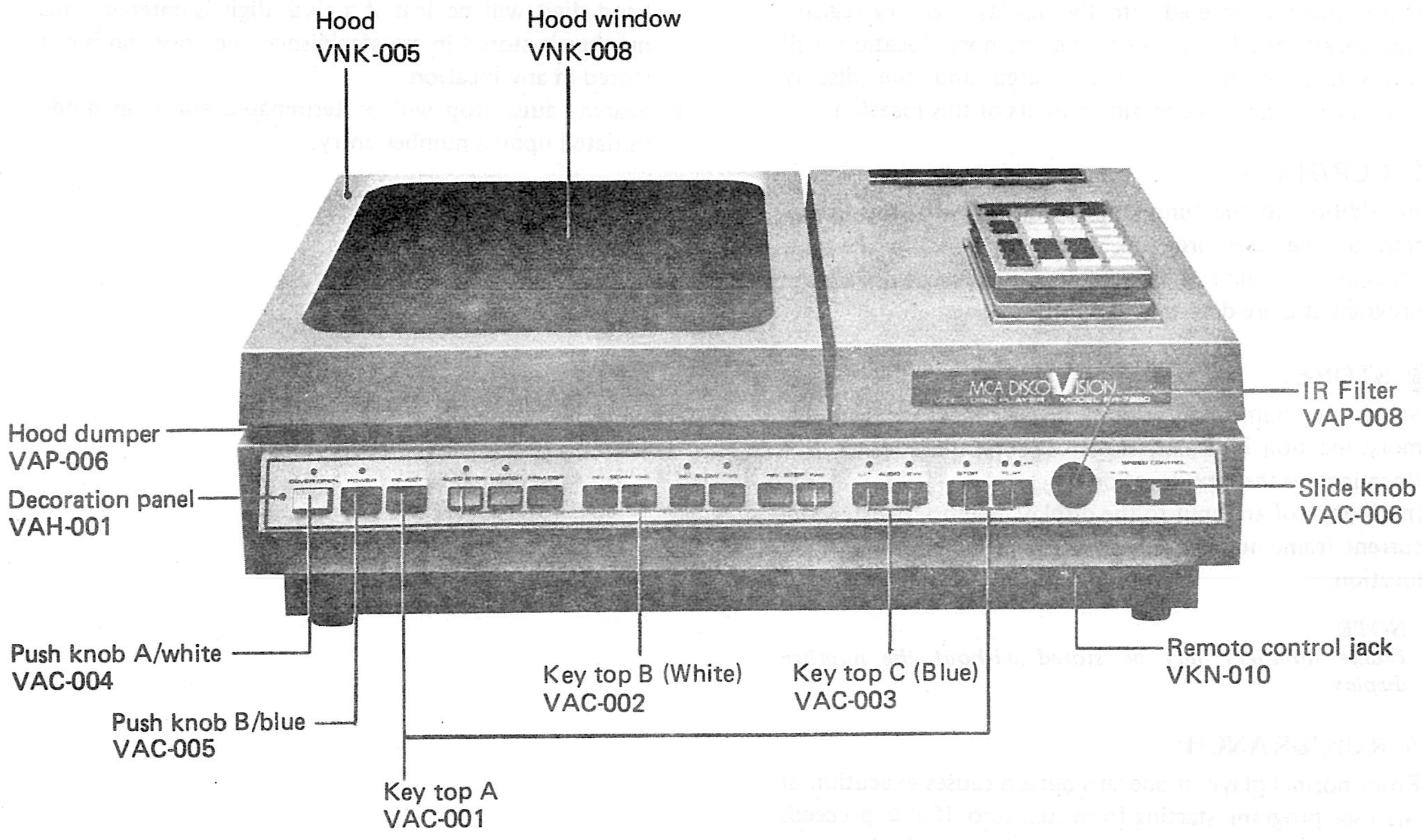
This button causes the player to enter the "write program" mode starting at program step zero. Subsequent pushing causes the program to step (1 step/push) for examination or editing. From normal player mode if the program button is preceeded by a # , (0-1023) the "write program" mode will be entered and displaying this program step and its.

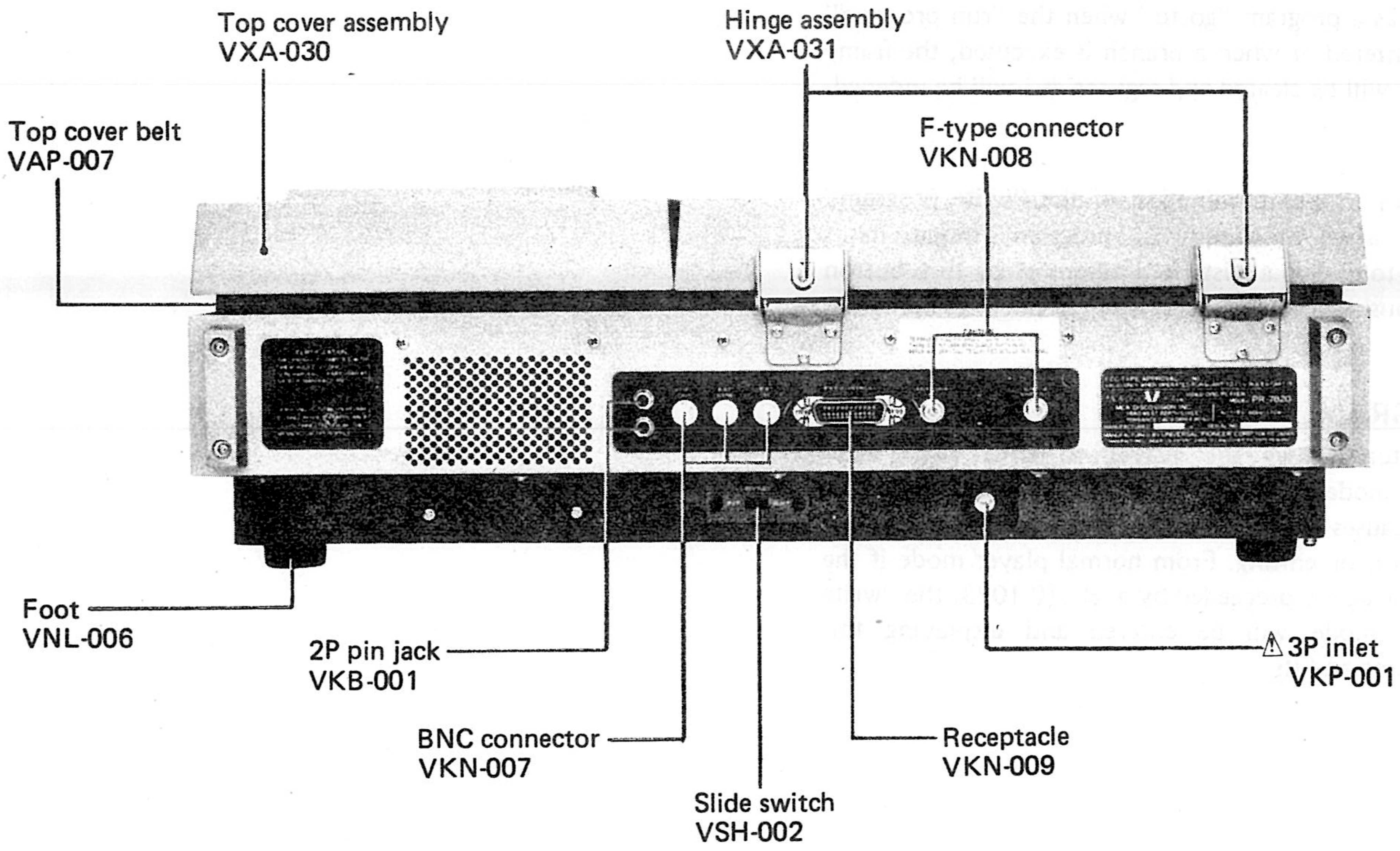
⑳ DIGITS 0-9:

a. From play, stop, slow fwd/rev – Depressing a number button will load that digit in the right-hand digit location and shift all other digits to the left by one location. When five digits are reached, the fifth left-hand digit will be lost if a sixth digit is entered. This number is stored in register display memory and is not stored in any location.

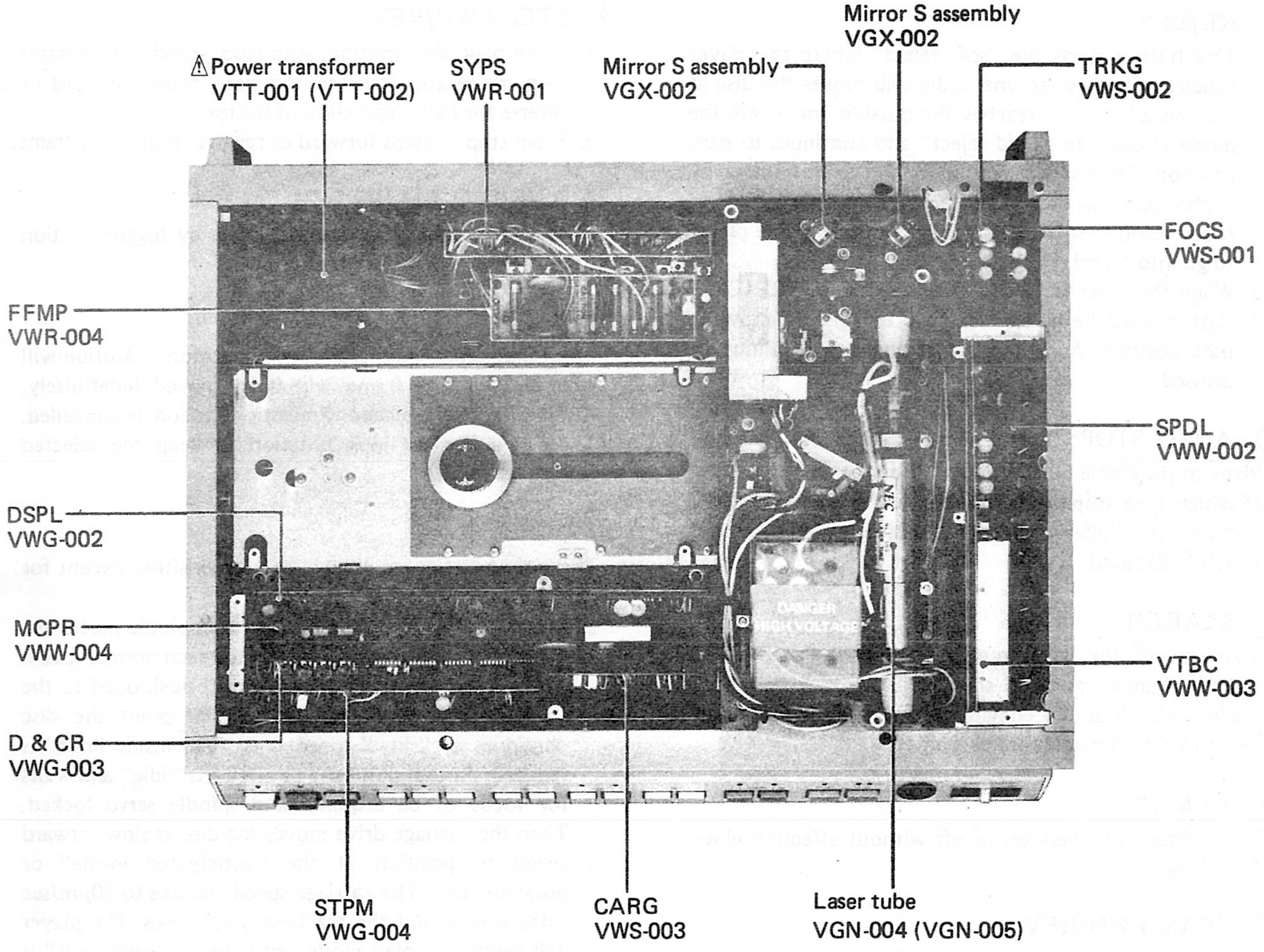
b. Search, auto stop will be terminated and stop mode initiated upon a number entry.

4. PARTS LOCATIONS





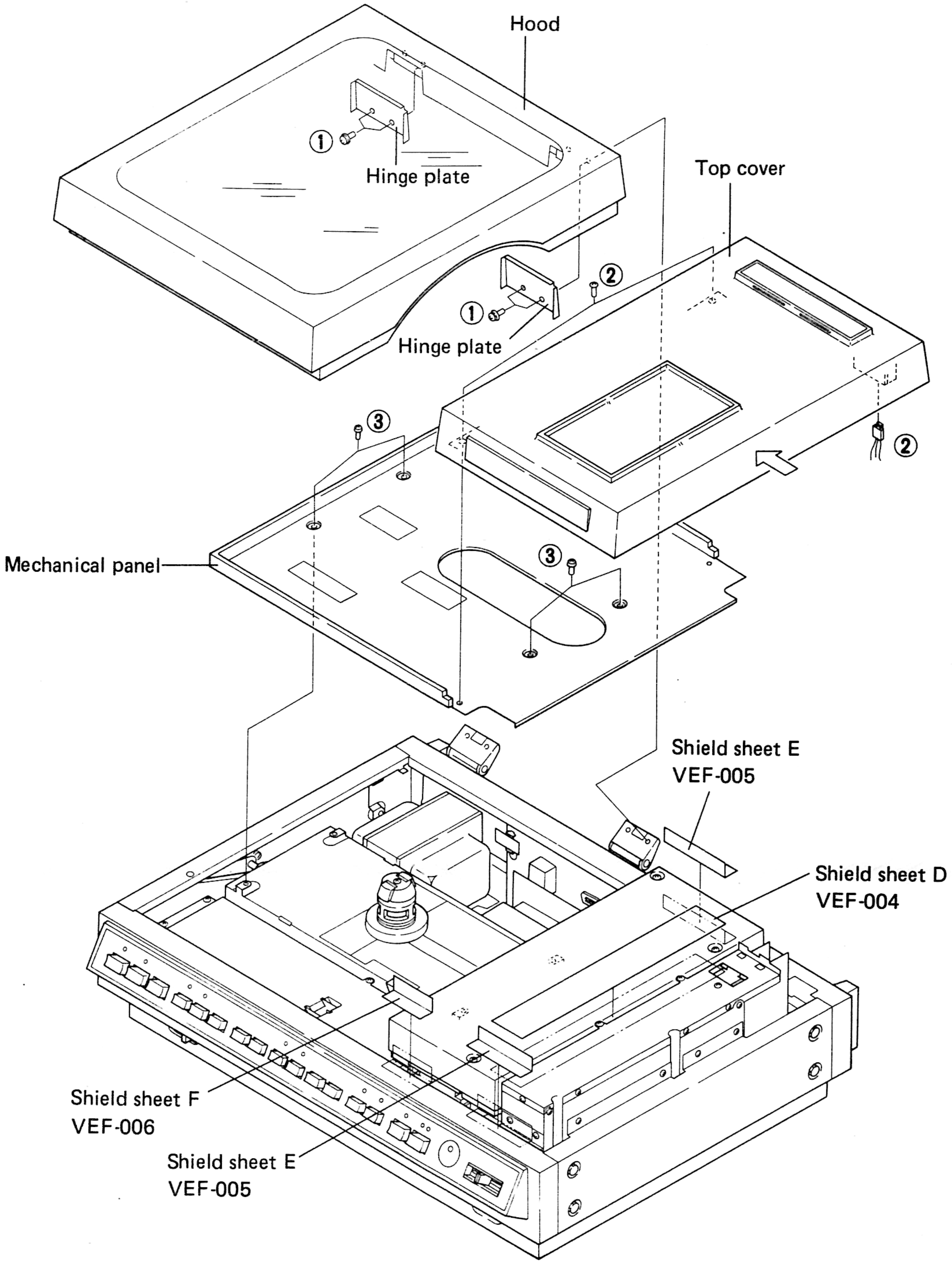
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*



5. DISASSEMBLY

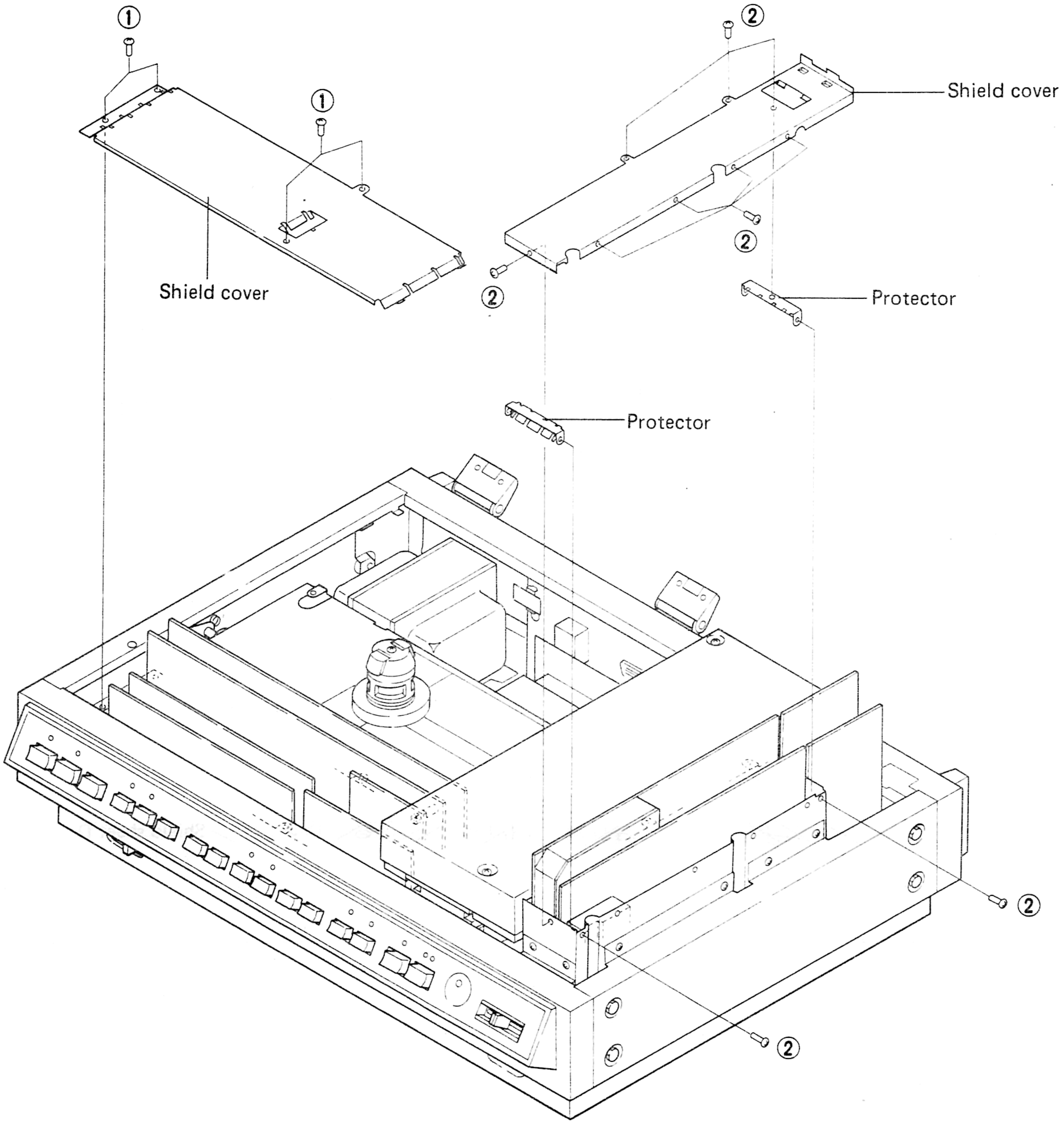
● Hood and Top plate

1. Remove the four screws ① to detach the hood.
2. Remove the two screws ② and connector to detach the top cover.
3. Remove the four screws ③ to detach the mechanical panel.

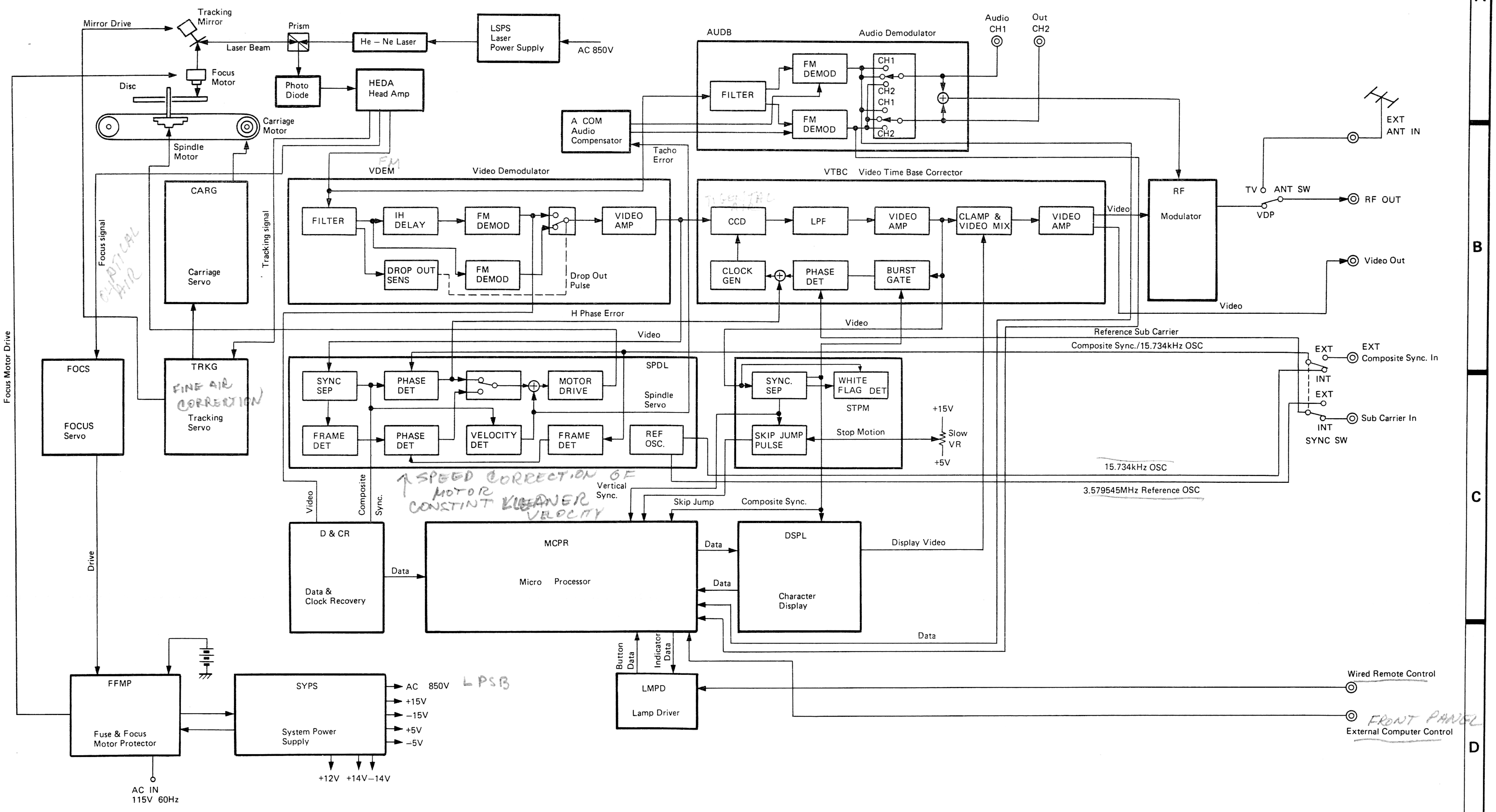


- **P.C. Board assembly**

Remove the two screws ①, ② to detach the shield cover.



6. BLOCK DIAGRAM



7. GENERAL INFORMATION

1. Disc Recording Method

A video signal plus a stereo audio signal are modulated into FM signals, and recorded in the form of pits in the disc track. The frequency spectrum is outline in Fig. 1 below.

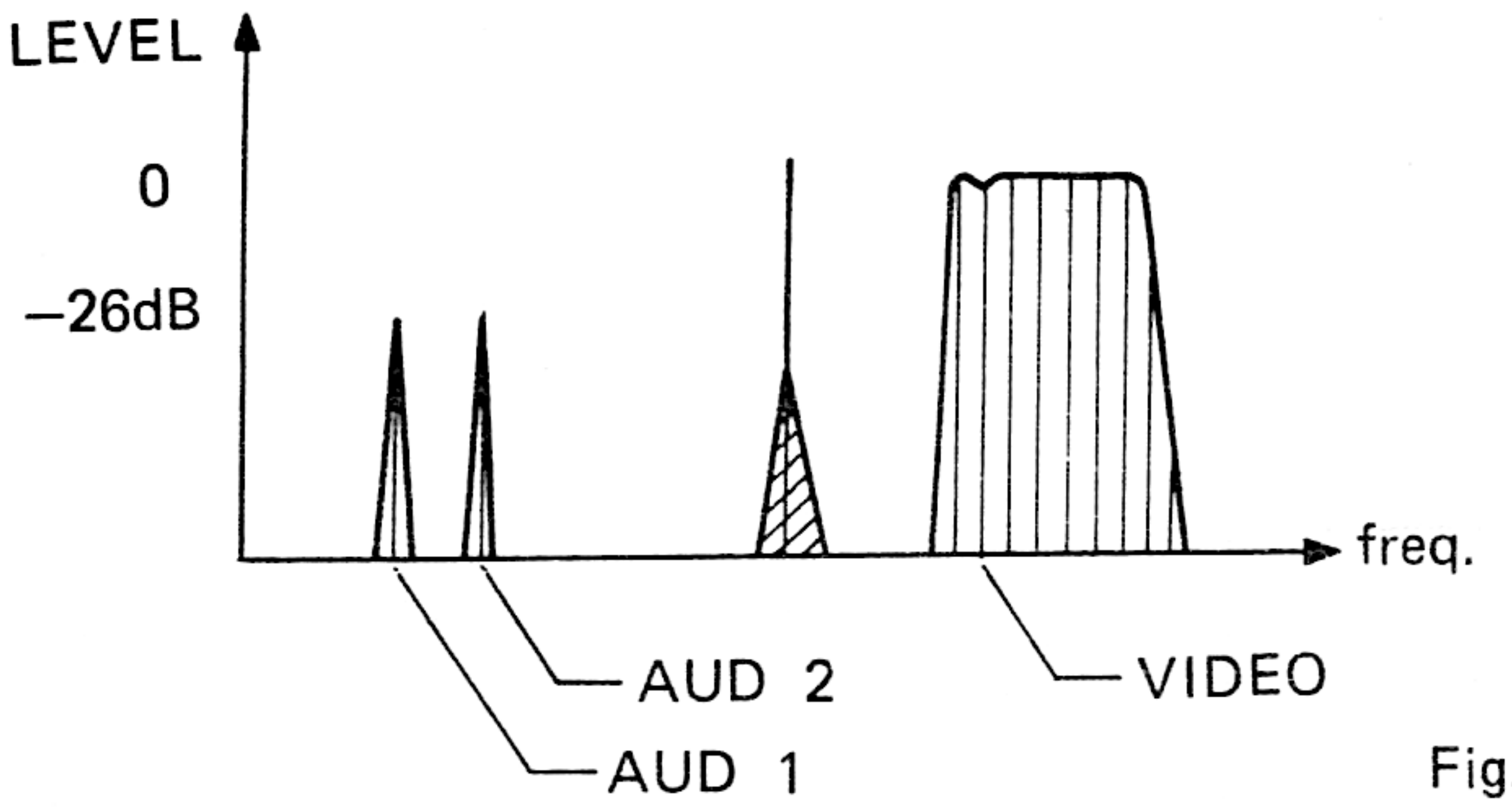


Fig. 1

2. Playback Method

A laser beam is directed into the disc track and reflected back onto photo-sensitive elements and converted into electrical signals which are subsequently amplified. The RF signal passed through a filter to remove the audio carrier signals is detected to the video signal by the frequency detector stage. The audio signals, on the other hand, are retrieved by first removing the video carrier signal by filter, then separating the AUD_1 and AUD_2 carrier signals (by band-pass filters) which are finally passed on to frequency detector stages to obtain the desired signals.

The servo circuits include a spindle servo circuit which maintains constant disc rotation speed, a focus servo which keeps the laser beam focussed exactly onto the disc track, a tracking servo which ensures that the laser beam continues to trace the same track, a carriage servo which maintains a constant carriage shift rate, and a video time base controller which compensates for error on the time base.

Control circuits include a slow motion circuit for still pictures, a data read out circuit which displays frame number in a part of the screen, a display circuit, and a microprocessor which transfers signals from the control panel to the relevant circuit boards according to the selected operation.

3. Structure

The positions of the various printed circuit boards are indicated in Fig. 2.

Circuit	Major Functions
VDEM	Video signal demodulation and drop out compensation.
AUDB	Audio board
VTBC	Video & time base corrector
CARG	Carriage servo
TRKG	Tracking servo
SPDL	Spindle servo
HEDA	Head amplifier
DSPL	Character display
MCPR	Microprocessor
D & CR	Data & clock recovery
STPM	Stop motion
SYPS	System power supply
LSPS	Laser power supply
ACOM	Audio compensator
LMPD	Lamp driver board
RF MO	RF modulator

4. Circuit Description

(1) HEDA

The faint voltage signals generated by the photo-sensitive elements (arranged as shown in Fig. 1) are amplified by the head amplifier.

Although the tracking signal depends on the difference in voltage between 1 and 2, these two voltages are simply amplified by the head amplifier as the 1 and 2 detector voltages.

For the focus signal, voltages 3 and 4, and voltages 5 and 6 are amplified by the head amplifier.

The RF signal is the amplified sum of voltages 3, 4, 5 and 6.

In order to eliminate unwanted radiations, the head amplifier has been mounted in a shielded case.

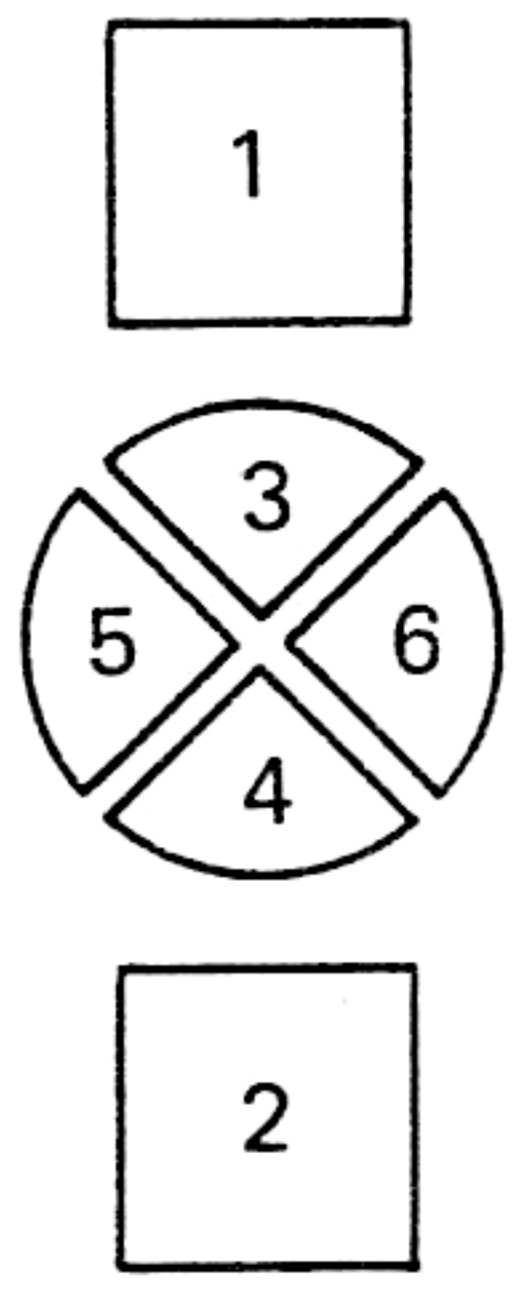


Fig. 2

(2) VDEM (Video Demodulator)

Mounted on a circuit board "pocket", this circuit obtains the video signal upon detection of the signals amplified by the head amplifier. The RF signal is obtained by removing the audio carrier signals via filters. Then after passing this signal through a limiter to remove the AM components, it is detected in the detector circuit by a pulse counting method. The VDEM circuit also contains a drop out compensator (1H delay line) which prevents the effects of drop outs (generated by scratches on the disc surface) from appearing in the playback picture. The drop out compensated signal is passed on to the VTBC and SPDL circuits.

(3) VTBC (Video Time Base Corrector)

The video signal demodulated by the VDEM still contains time base error due to disc eccentricity and motor rotational fluctuations. This time base error is corrected by comparing the phase of the color burst signal from the playback video signal with the reference oscillator output signal and subsequently controlling the CCD. Furthermore, in order to expand the color lock range the time base error in the horizontal synchronizing signal from the SPDL is added to the color burst phase comparison error.

(4) AUDB and ACOM (Audio Demodulator and Audio Compensator)

For detection of the audio signals recorded on the disc. The audio carrier signals are separated by passing the playback RF signal through band-pass filters, and then detected by FM detectors to obtain the audio signals. The channel 1 and channel 2 MIX signals are passed to the RF MOD to be modulated. Time base error is also generated in the audio signals by disc eccentricity, this error being corrected by changing the operational point of the FM detector by the SPDL speed error.

(5) SPDL (Spindle Servo)

The spindle motor is normally controlled by the output signal obtained by comparing the phase of the playback horizontal synchronizing signal and the reference oscillator signal. But when the rear panel INT/EXT switch is put in the EXT position and an external synchronizing signal applied, the frame lock circuit will be activated. Prior to the frame lock circuit, the phase of the playback frame pulse is compared with the EXT frame pulse, while after the frame lock, this is replaced by a horizontal synchronizing H lock loop.

The spindle servo circuit also includes a control circuit to ensure constant motor speed by detecting motor current and terminal voltage prior attaining proper focus. When using CLV discs, a carriage potentiometer is employed to vary the spindle motor free-run frequency while moving from the inner to the outer circumference.

(6) TRKG (Tracking Servo)

The tracking servo control circuit is designed to move the mirror in a radial direction. The tracking detector signal from the head amplifier is amplified in order to drive the mirror. During stop motion mode, a command signal from the MCPR causes the same track to be repeated once every complete turn of the disc.

(7) CARG (Carriage Servo)

This circuit ensures that the carriage is shifted at a constant speed (3 speed selector — fast, mid, slow). During play mode, the carriage servo is controlled by the tracking error. Hence any increase in swing angle as the tracking mirror traces the disc track will be absorbed by shifting the carriage.

(8) FOCS (Focus Servo)

This circuit ensures that a constant distance is maintained between the lens and disc track (by varying the current passed through the focus motor) in order to keep the laser beam properly focussed on the disc track. Focus error is detected by monitoring the distance between the track and lens (which is moved as a result of signals from the photo-sensitive elements) and subsequently controlled by using the signal amplified by the head amplifier.

(9) D & CR (Data and Clock Recovery)

Frame number data is recorded during the V blanking interval of the video signal. This frame number signal is read out by the D & CR circuit. The demodulated signal is first passed to the MCPR, and then to the DSPL (by MCPR command) to be finally displayed in a part of the screen.

(10) DSPL (Display)

When character data is transferred from the MCPR it is modulated into a video signal by the character generator. These character signals are then passed via the VTBC to be mixed with the main playback video signal to be displayed on the screen.

(11) STPM (Stop Motion)

This circuit is used to separate the synchronizing signal from the playback video signal, and to also detect the white flag signal required for stop motion mode.

(12) MCPR (Microprocessor)

The microprocessor passes the relevant signals to each circuit board according to the command signals from the front panel controls.

(13) SYPS (System Power Supply)

Each circuit board is supplied with regulated power after rectifying the output of the power transformer secondary coil.

(14) LSPS (Laser Power Supply)

This circuit provides the high voltage required to trigger laser oscillation. After rectifying the 850V on the secondary coil of the power transformer, a constant current (5mA) flow through the laser is maintained.

8. OPTICAL DESCRIPTIONS

1. Outline of platform

Optical platform and outline of the beam pass are shown in Fig. 3.

Laser Tube

A He-Ne gas laser with wavelength of 632.8μm.

Grating

Glass plate with large number of grooves etched in the surface, and used to split the laser beam into 3 separate beams.

Diverging Lens

A normal convex lens.

Prism

After passing the laser beam from the laser tube, the laser beam reflected from the disc is deflected by 90° inside the splitter.

In other words, the splitter is able to either pass or deflect the laser beam depending on the plane of light polarization.

This unit generates a phase difference of a quarter of a wave length, depending on the plane of light polarization, as the beam is passed through.

Objective Lens

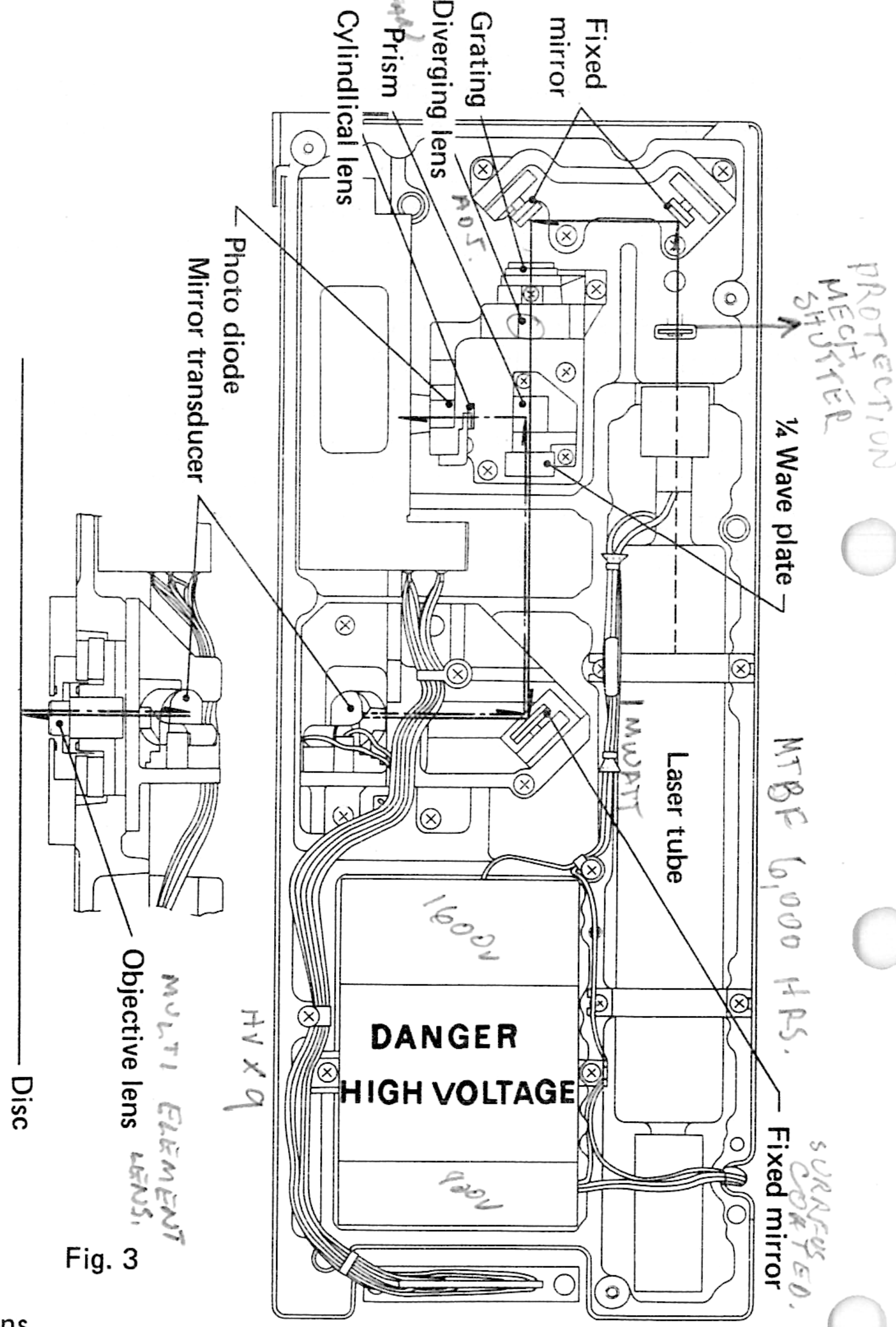
A normal objective lens.

Cylindrical lens

A lens in the shape of a cylinder divided down the center.

2. RF Signal

The beam from the laser tube which is linearly polarized in the horizontal direction is divided by a grating into 3 beams of the horizontal direction (see Fig. 4).



MIRRORS ARE REFLECTED COATED FROM THE FRONT.

CLEAN

ADJ.

PROTECTION MECH SHUTTER

1 MWATT

MTBF 6,000 HRS.

1600V

900V

HV x 9

MULTI ELEMENT LENS.

SURFACE COATED.

Fig. 3

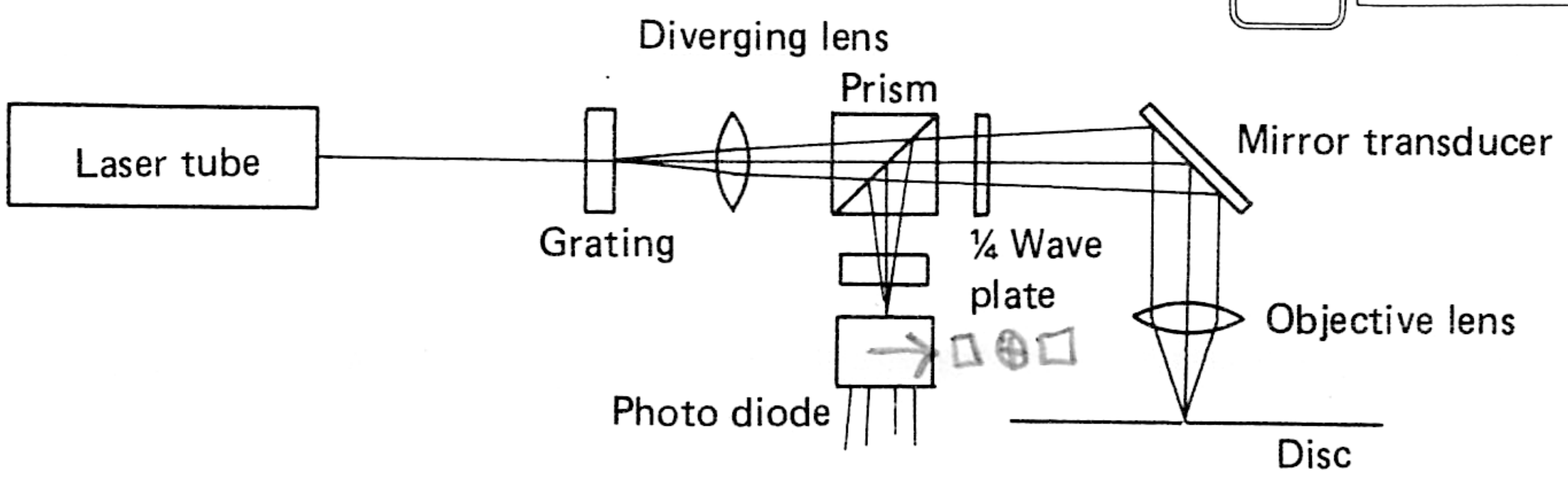


Fig. 4

LASER TUBE $200 TO $300 TO REBUILD

The center beam is used for focus servo control and to read the RF signal, while the 2 side beams are used for tracking servo control.

After being spread out by a diverging lens, these 3 beams are passed through a prism, and become circularly polarized light by passing the 1/4-wave plate. The beams are then passed through a mirror transducer, and focussed in a spot 1.5μ in diameter on the reflection film which is about 1.0mm below from the disc surface, by an objective lens.

This beam is reflected, and is passed back in the reverse direction along the input path, and then become a linearly polarized light beam in the vertical direction by passing the 1/4-wave plate. The beam is then deflected through 90° by a prism and passed via a cylindrical lens to photo diode (see Fig. 5). This photo diode consists of 6 parts, the 4 outputs being mixed ($B_1 + B_2 + B_3 + B_4$) to form the RF output.

760 NANOMETERS. RED.

3. Tracking Servo Control

The 2 beams of both sides are arranged slightly out of alignment from each other as shown in Fig. 6. The corresponding reflected beams are applied to photo diodes A and C respectively (see Fig. 5). The tracking servo control maintains the difference between the 2 diode outputs at zero.

4. Focus Servo Control

As can be seen in Fig. 5 photo diode B is divided into 4 separate parts. When the laser beam spot is correctly focussed on the disc surface, the reflected beam forms a circular spot as shown in Fig. 7-1. If, however, the disc surface shifts towards the objective lens, the spot will appear as shown in Fig. 7-2, while if it shifts away from the lens, it will appear as shown in Fig. 7-3.

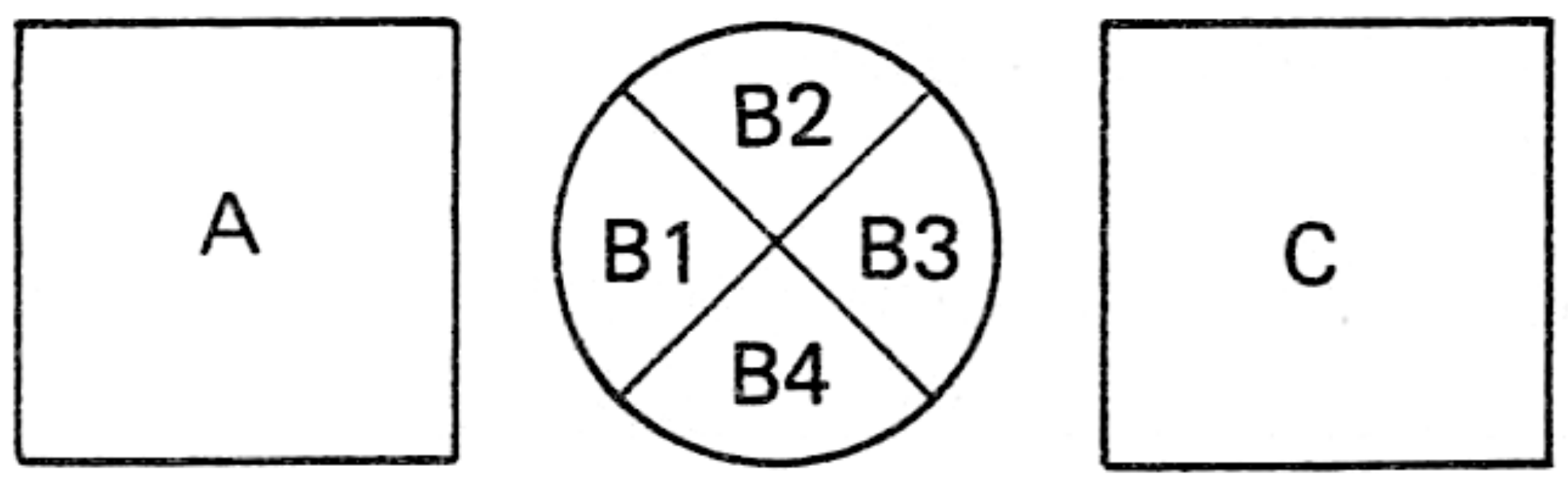


Fig. 5
Photo diode pattern

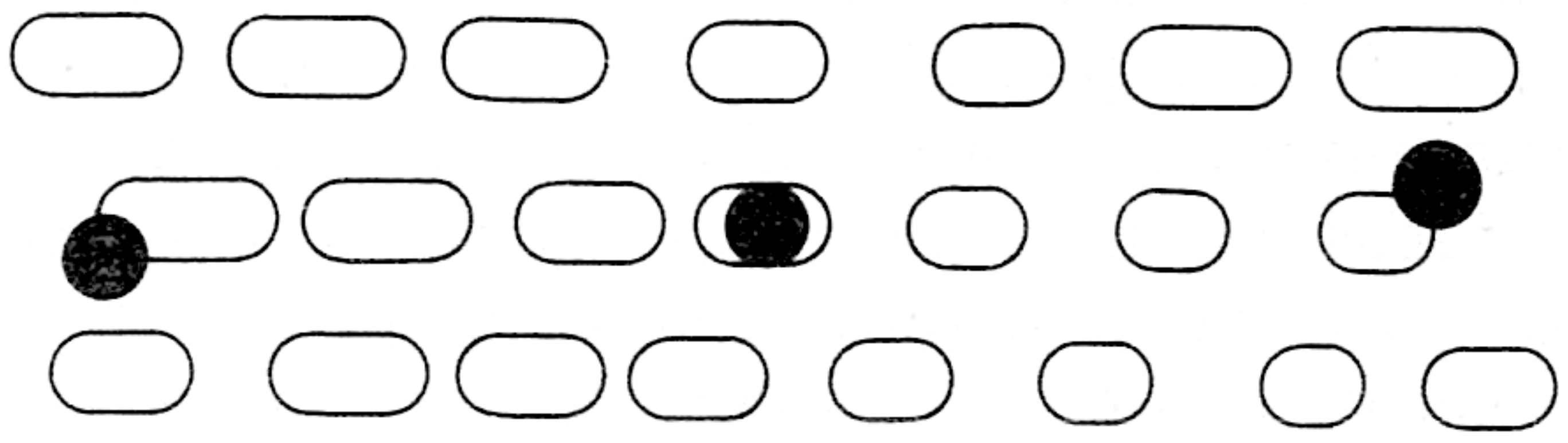


Fig. 6

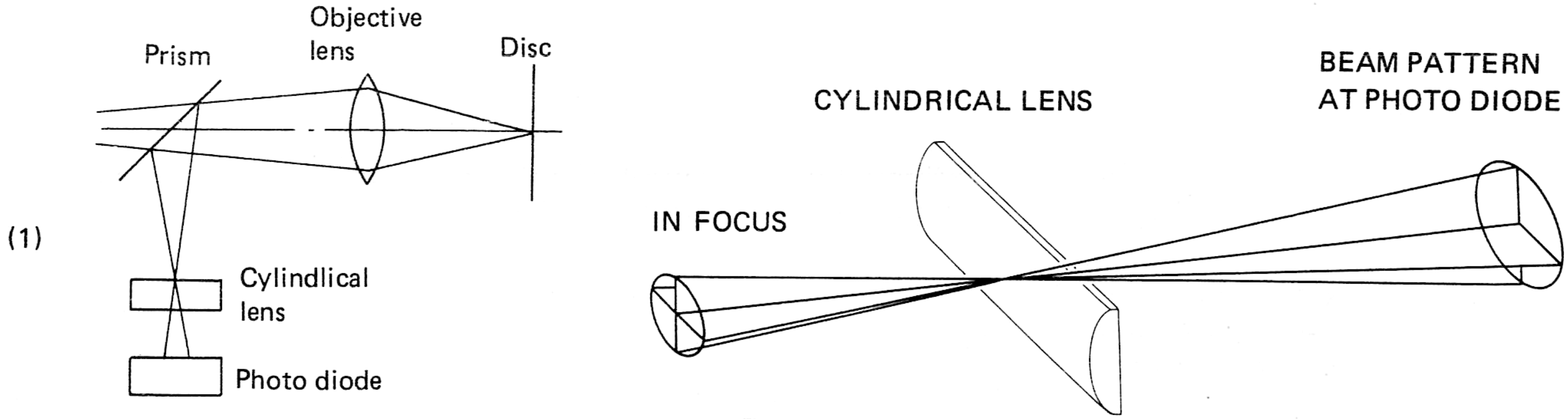


Fig. 7-1

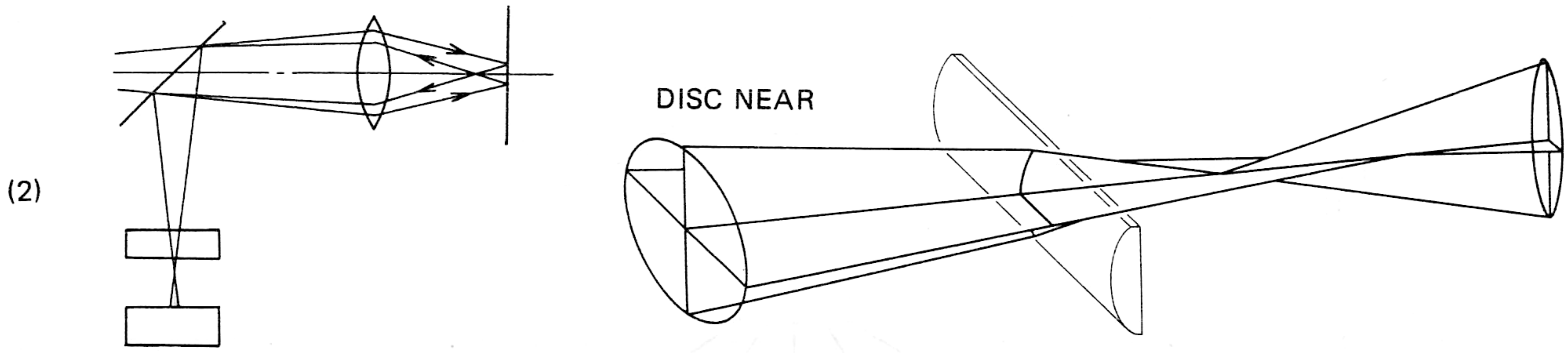


Fig. 7-2

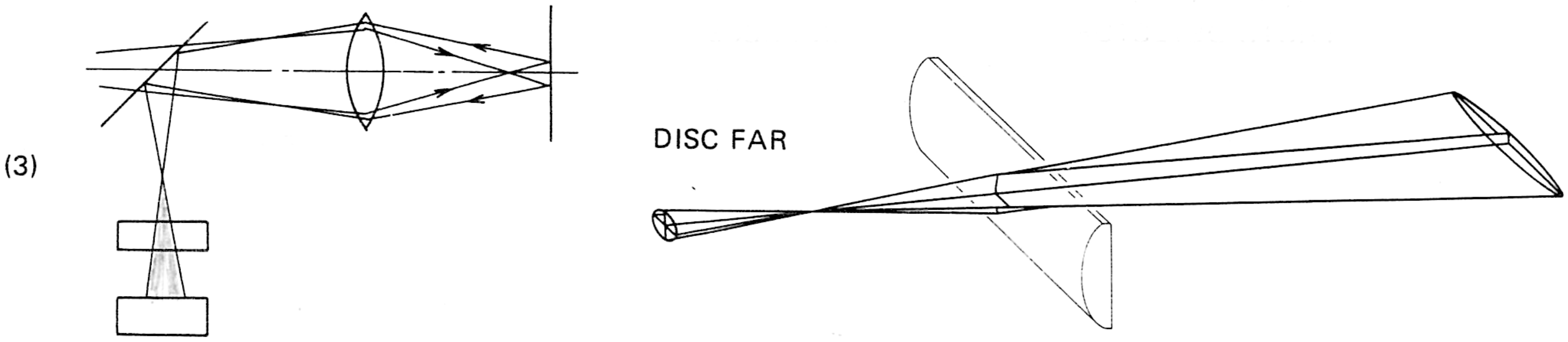


Fig. 7-3

Shape of beam cross section at photo detector, relates the distance between disc and objective lens is shown in Fig. 8.

The 4 separate photo diode output signals are mixed according to the following equation: —

$(B_1 + B_3) - (B_2 + B_4) = V$

where $V = 0$ when the beam is correctly focussed, $V > 0$ when the disc is far from the lens, and $V < 0$ when it is near by the lens.

In other words, the photo diode composite output is only generated when the beam is out of focus, resulting in a current being passed through the focus motor to move the objective lens back and forwards, thereby maintaining the beam correctly focussed at all times.

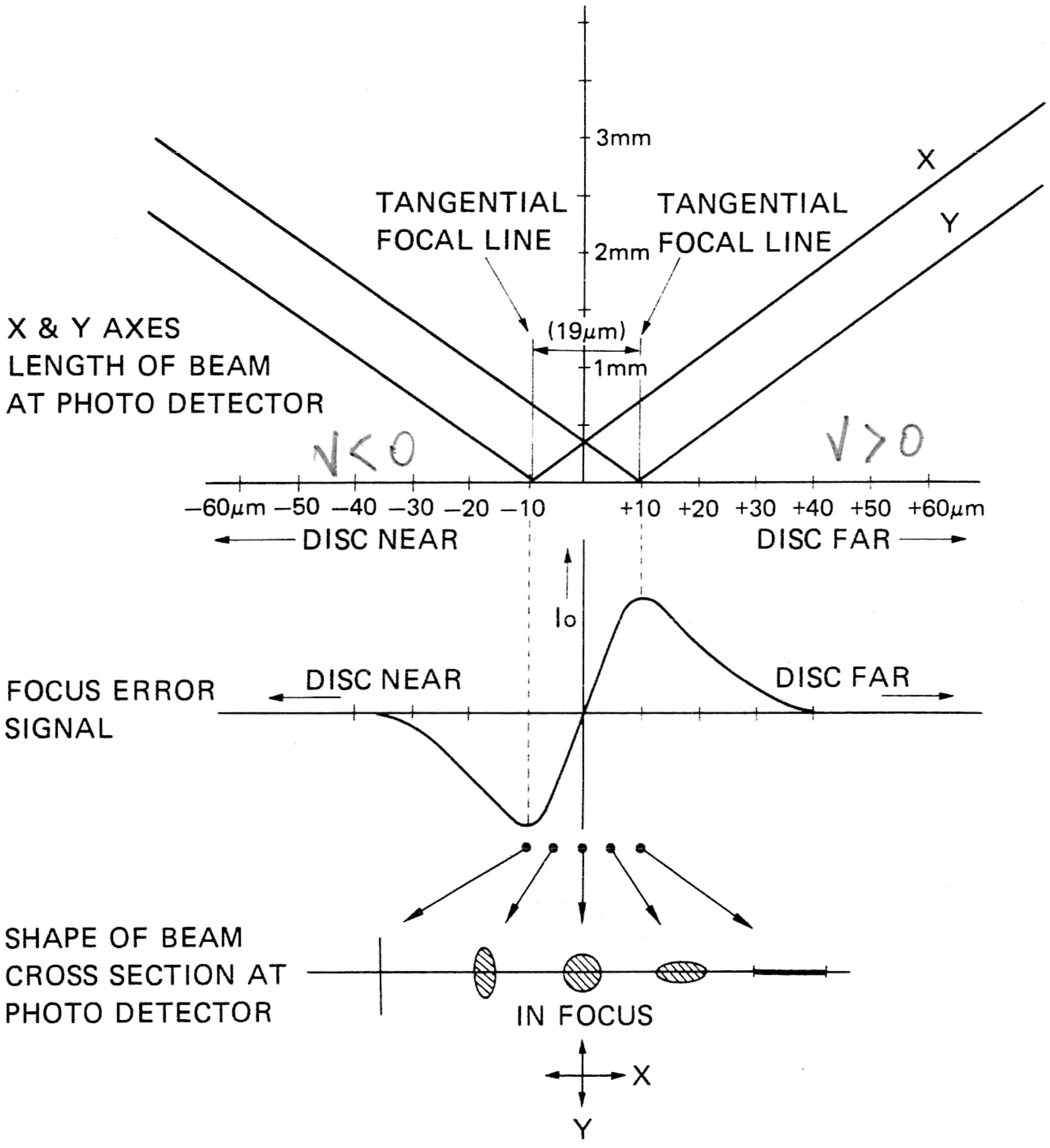

3mm
2mm
1mm
X
Y
TANGENTIAL FOCAL LINE
TANGENTIAL FOCAL LINE
(19μm)
X & Y AXES LENGTH OF BEAM AT PHOTO DETECTOR
V<0
V>0
−60μm −50 −40 −30 −20 −10
+10 +20 +30 +40 +50 +60μm
DISC NEAR
DISC FAR
Io
FOCUS ERROR SIGNAL
DISC NEAR
DISC FAR
SHAPE OF BEAM CROSS SECTION AT PHOTO DETECTOR
IN FOCUS
X
Y

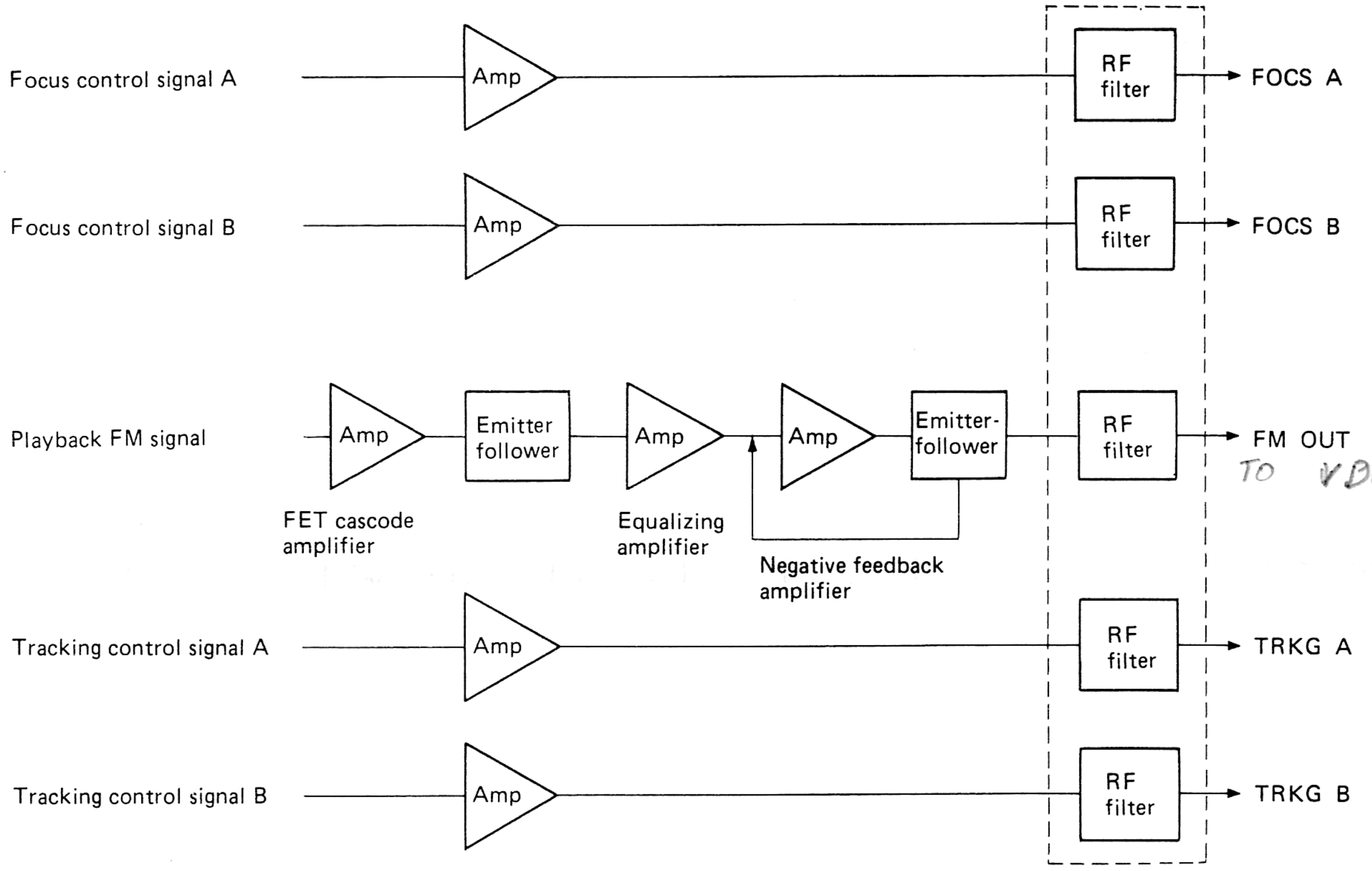
Fig. 8

9. CIRCUIT DESCRIPTIONS

9.1 HEDA

The playback FM signal from the photo detector is applied to the FET cascode amplifier (Q_1, Q_2 and Q_3) where it is amplified by approximately 20dB. The output signal is then passed via the Q_4 emitter-follower to the Q_5 equalizing amplifier where the high frequencies are boosted to improve the overall frequency response, and the cut-off frequency fixed at about 26MHz. Then after being applied to a negative feedback amplifier (Q_6 and Q_7) the signal appears at the output of the Q_7 emitter-follower, an overall gain of about 30dB being obtained. In order to eliminate a 620MHz spurious signal from the laser tube, the output signal is also passed through a low-pass filter.

The focus and tracking control signals are both passed through single amplifier stages (Z_1 and Z_2 respectively) and identical low-pass filters. FOCSA and B and TRKGA and B are the resultant output signals.



TO VDEM BD

Fig. 10 HEAD BLOCK DIAGRAM

9.2 VDEM

Until the photo-diode picks up a signal from the laser, the main signal path demodulator (DEMOD) is kept off by the IN FOCUS signal, and both DOS and DOS are maintained at high level. The switch will thus be open, thereby preventing the appearance of any noise signals at the video output.

After IN FOCUS, the FM signal amplified by the HEAD AMP is distributed to the main signal path, the drop out sensor (DOS) circuit, and the AUDIO circuit board. The main signal path FM signal also contains an audio signal, pilot signal, and other noise components in addition to the video signal. The unwanted signals are removed by filter (2), while VR_1 serves to adjust the FM signal level. After passing through the filter, the signal is sufficiently amplified by the limiter, and amplitude is also made constant. VR_2 is the limiter balance control.

After further amplification by the line receiver, and conversion to TTL level, the FM signal is demodulated into the video signal by the TTL equipped pulse count detector. The linearity of the detector is adjusted by VC_1. Since the demodulated video signal is still a low level pre-emphasized signal containing high frequency components, it is next passed through amplifier and de-emphasis stages and a low-pass filter (fc ≒ 5MHz) before being applied to the drop out compensation switch (9). However, since drop out compensation in the D & CR stage is likely to result in loss of data, a part of the video signal is applied to this stage prior to the drop out compensation stage. Video signal level may be adjusted by VR_3. In summary then, the main signal path in the video demodulator circuit proceeds via (1)—(2)—(3)—(4)—(5)—(9).

The FM signal passed through filter (2) is also applied to the 1H delay line. After a 1H delay (63.5μsec.), the signal is demodulated by the quadrature detector. (The 1H delay makes use of the close similarity between adjacent horizontal scan lines, employing the previous scan line to "fill in", or compensate, any gap left by a drop out). The signal is then passed through a filter which serves as a de-emphasis stage as well as a high-cut filter. Next it is amplified, and finally applied to the drop out compensation switch (9). The VR_4 control is used to adjust the level to the same video level as in the main signal path. Hence, the 1H delay video demodulation route is via (6)—(7)—(8).

Drop outs in the FM signal picked up by the photo-diode are caused by the presence of dust, scratches, and other irregularities in the surface of

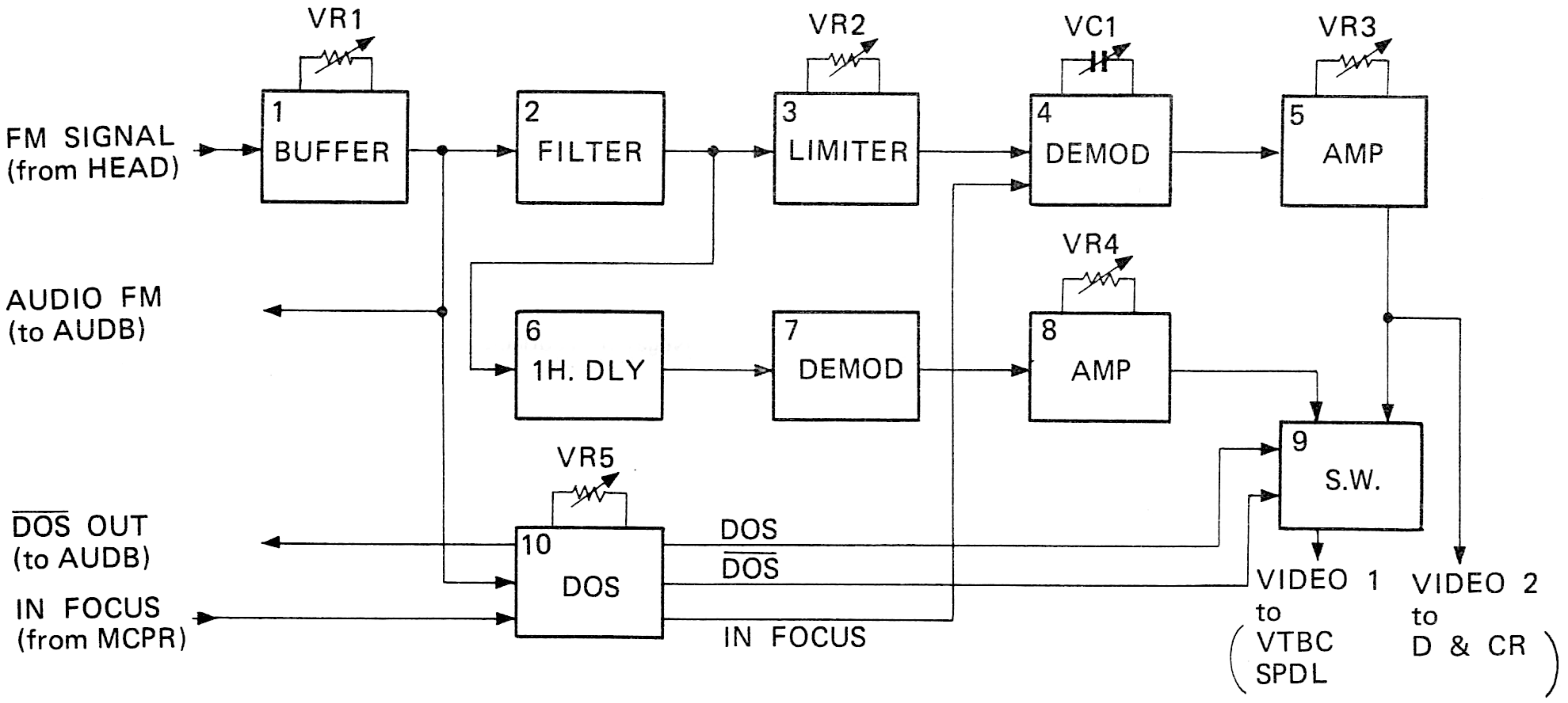


Fig. 11 VDEM BLOCK DIAGRAM

the video disc, and subsequently lead to distortion in the video output signal. Detection of these drop outs and the consequent generation of signal switching pulses occurs in this drop out detection circuit. There are actually 2 forms of the DOS signal — the main DOS signal which passes via the main signal path in the absence of drop outs, but which interrupts the main path when a drop out appears, and the DOS signal (of opposite polarity to the main DOS signal) which connects the 1H delay video signal to the main signal path when a drop out occurs, but leaves the signal unconnected at all other times. Although the TTL level processing results in practically no time delay at all in the DOS signal, the video signal is delayed by several hundred by the two filters it is passed through. This difference is compensated for by inserting a trough in the DOS signal several hundred later, thereby preventing the appearance of any image distortion resulting from drop outs. Hence, the signal path for the drop out detector circuit also includes (10).

The block diagram is outlined in Fig. 11, and the time chart in Fig. 12.

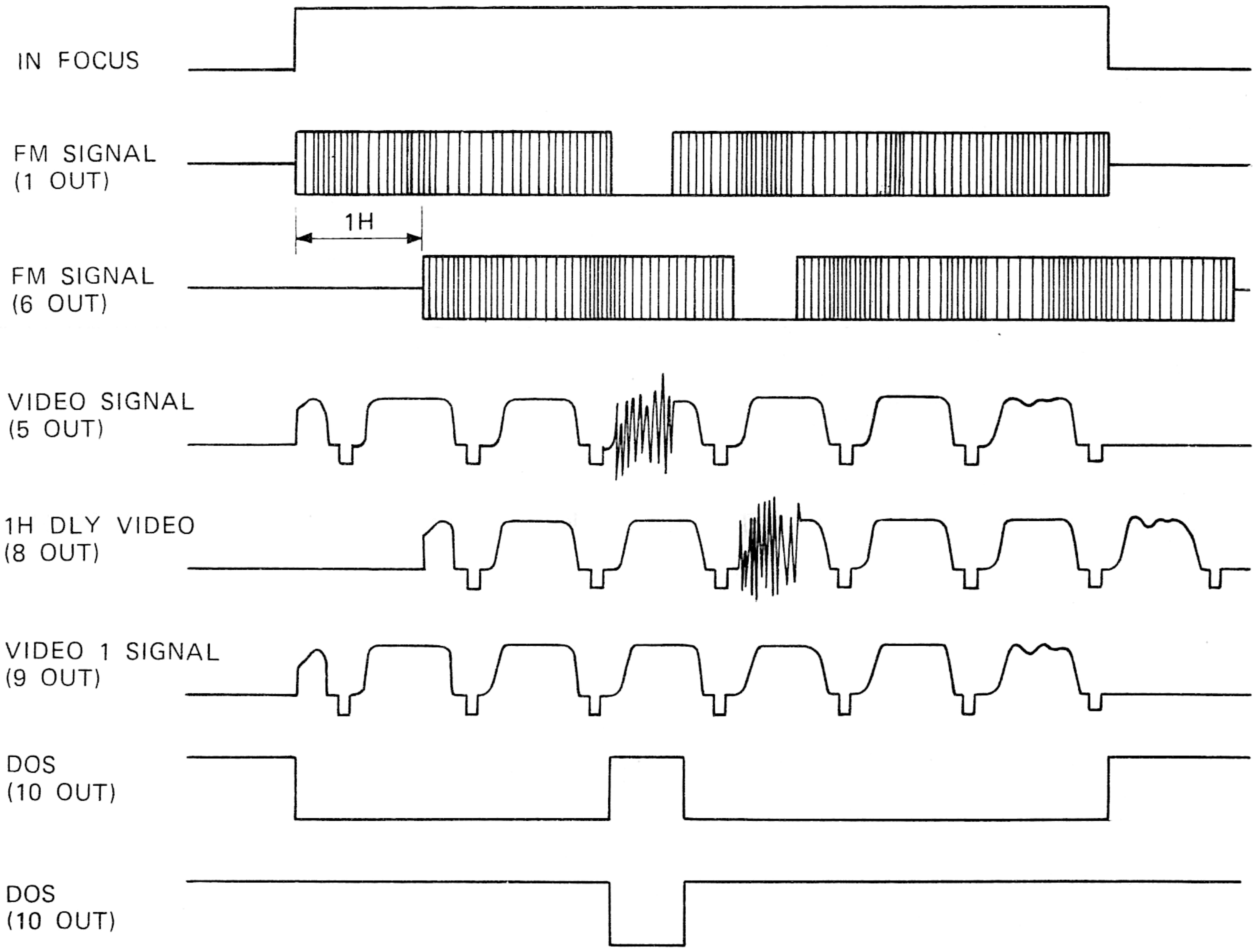


Fig. 12 TIME CHART

9.3 AUDB

The FM signal extracted from the video disc by the photo-diode is passed via the HEDA and VDEM stages to the AUDB circuit. As can be seen from the accompanying spectrum diagram, this FM signal contains unwanted FM video signal components and a 0.4MHz pilot signal, all of which must be removed.

First the FM video signal components are attenuated by a 4MHz low-pass filter, the remaining audio signals being subsequently amplified by a limiter where amplitude variations are also removed.

Since the channel 1 (L) and channel 2 (R) audio signals have been FM modulated on 2.3MHz and 2.8MHz carriers, the unwanted pilot signal, video FM signal, and any other channel audio FM signals are removed by employing 2.3MHz and 2.8MHz band-pass filters.

After passing through these BPF stages, the audio FM signals are further amplified by limiter and detector stages where additional amplitude variations are removed, and the FM signals detected. The FM detector stage is a quadrature detector circuit with VL_1 and VL_2 being used to adjust the linearity of the channel 1 and channel 2 detector circuits.

If the video disc should happen to be slightly off-center, the detected audio signals will also contain eccentricity component signals, the size of the signals being proportional to the degree of disc eccentricity. This eccentricity will also result in a certain amount of flutter, but since this is extremely small, it presents no practical problem.

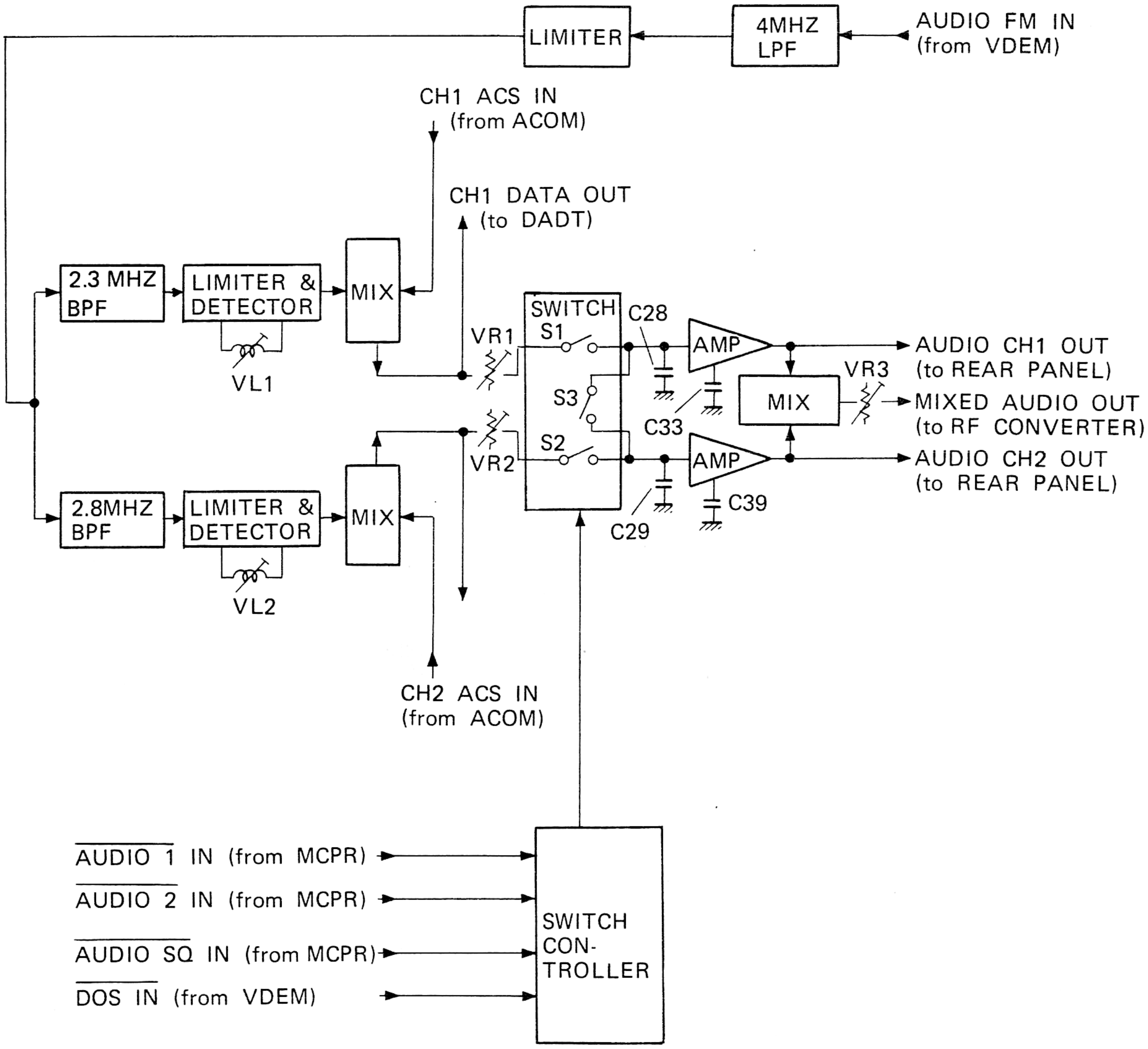


Fig. 13 AUDB BLOCK DIAGRAM

The eccentricity component signals are detected by the ACOM circuit which in turn applies them to the left and right mixer circuits as ACS signals of opposite phase, resulting in the cancellation of the eccentricity component signals in the audio signals.

Besides being applied to the DADT as data dumping signals, the mixer output signals are also passed via VR_1 and VR_2 (audio output level setting controls) to the switching circuit. If $\overline{\text{AUDIO 1}}$ and $\overline{\text{AUDIO 2}}$ are both low level S_1 and S_2 will turn on and S_3 turn off, resulting in the appearance of independent channel 1 and channel 2 output signals. If, however, $\overline{\text{AUDIO 1}}$ is high, and $\overline{\text{AUDIO 2}}$ is low, S_1 will turn off while S_2 and S_3 turn on, resulting in the channel 2 signal being connected to both the CH_1 OUT and CH_2 OUT outputs, and the channel 1 signal will not be connected. If on the other hand, $\overline{\text{AUDIO 1}}$ is low and $\overline{\text{AUDIO 2}}$ is high, the reverse case will be set up, S_2 turning off while S_1 and S_3 turn on. The channel 1 signal will then be connected to the CH_1 OUT and CH_2 OUT outputs and the channel 2 signal will not be connected. If $\overline{\text{AUDIO 1}}$ and $\overline{\text{AUDIO 2}}$ are both high level, S_1 and S_2 will both turn off (and S_3 turn on), resulting in no output signal at all. When $\overline{\text{AUDIO SQ}}$ is low level, all switches (S_1, S_2 and S_3) are turned off, again resulting in no output signal appearing at the outputs.

These 3 switches are also turned off when the $\overline{\text{DOS}}$ signal (drop out detector signal) from the VDEM circuit is at low level. The $\overline{\text{DOS}}$ signal is thus held at the previous value by C_{28} and C_{29}, thereby preventing the output of noise caused by drop outs. The time constant of C_{33} and C_{39} (capacitors employed in the de-emphasis circuit) is 75μsec.

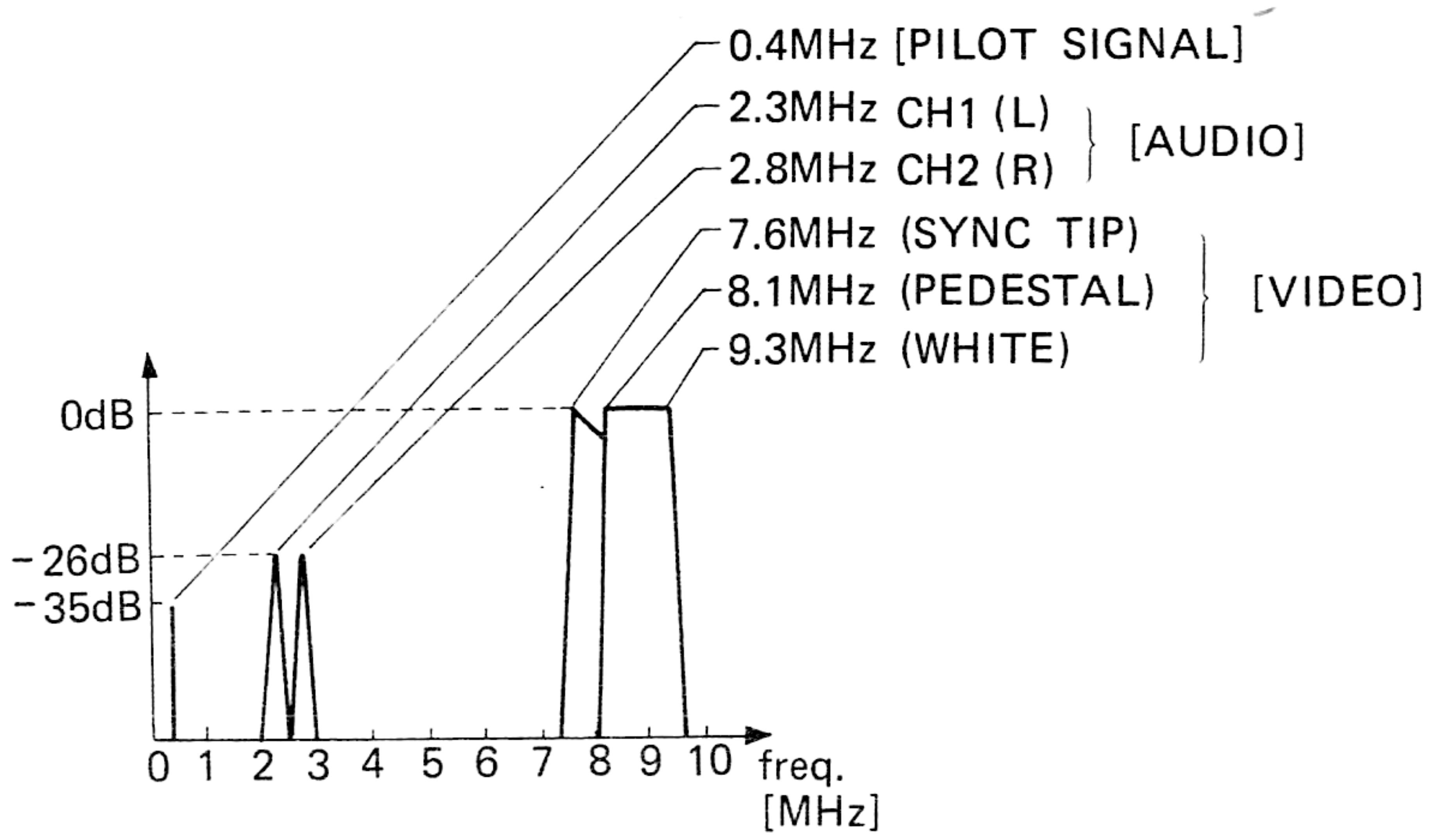


Fig. 14 INPUT FM SIGNAL SPECTRUM

9.4 ACOM

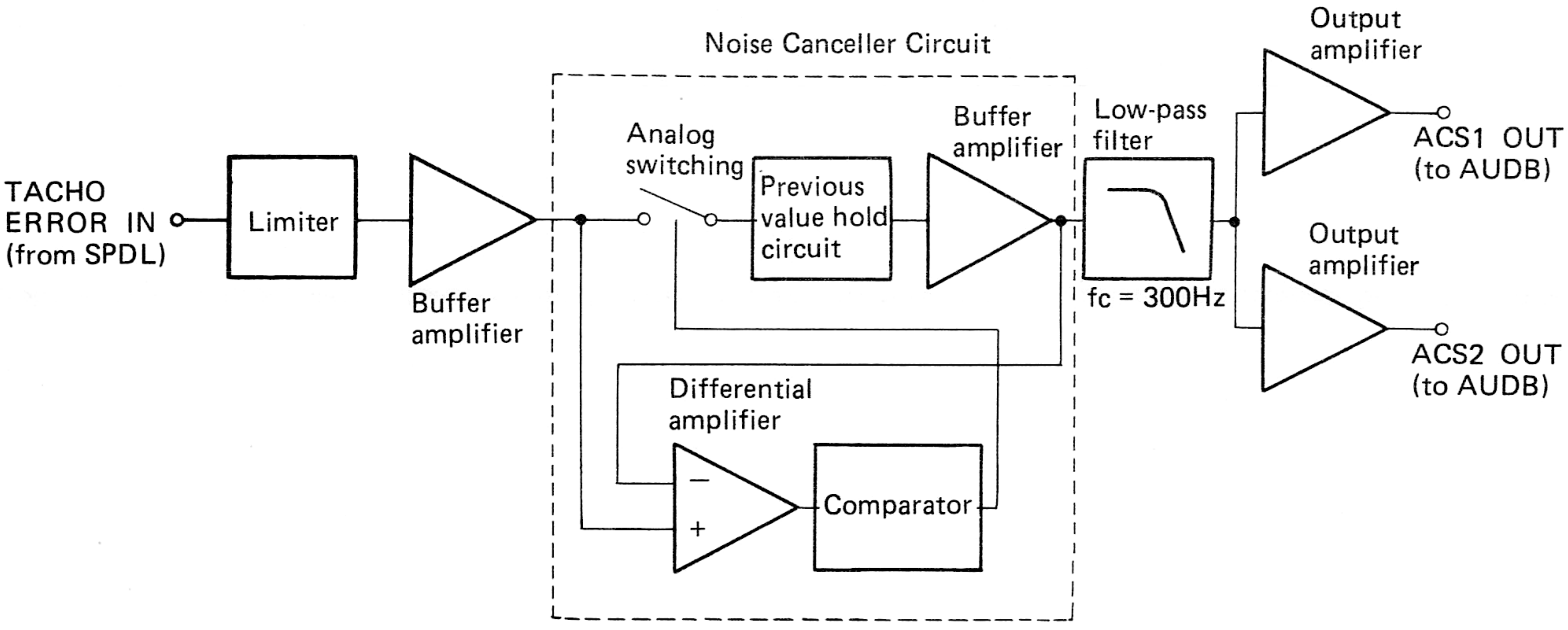
The ACOM (Audio Compensator) circuit has been designed to eliminate any eccentric component signals from the main audio signal when the video disc is not positioned in the exact center.

Since error in the time base caused by disc eccentricity will effect the audio signal, this error is corrected by cancelling the eccentricity components in the audio modulated signal. This is achieved by first rectifying the waveform of a tacho error signal from the spindle (error signal along the time axis), then eliminating the unwanted high frequency components, and then applying the reversed phase signal directly to the audio signal.

The tacho error signal is initially restricted within a ±5V range by a diode limiter to limit the noise components. (The tacho error signal from a 30μsec eccentricity corresponds to a level of 1.2Vp-p). The error signal is then applied to the noise canceller circuit via a buffer amplifier.

In this noise canceller circuit, the tacho error signal forms a step-wise waveform (with step widths of 63.5μsec.). When the step level exceeds the eccentricity error waveform by a certain amount (in either positive or negative direction), the difference is detected by the differential amplifier and comparator stages, and held by the analog switching and previous value hold circuit, thereby further reducing the noise components due to tacho error.

The output signal from the noise canceller circuit is passed via a buffer amplifier to a 300Hz low-pass filter which removes unwanted high frequency components. After then being passed through output amplifiers and undergoing level adjustments to match the levels with the audio signal levels in the mixer circuits (for left and right channels), the output signals are applied as ACS (audio compensation signal) components to the channel 1 and channel 2 audio modulated signals, thereby cancelling the eccentricity component signals contained in the audio signals.



ACOM BLOCK DIAGRAM

Fig. 15

9.5 FOCS

Focus Assembly Circuit Description

The focus servo is a servo circuit designed to maintain the laser beam focussed correctly onto the disc surface at all times. A 4-way splitter photo detector is employed to check that the focusing lens is always in the correct position. Any focus error is applied to the focus assembly differential amplifier, passed through various phase compensation circuits, used to stabilize the servo loop, and then applied to the focus motor from the motor drive amplifier.

During normal operation (as shown in the next page block diagram), any error signal is applied to the differential amplifier and on to the DC servo loop, motor drive amplifier and focus motor. The other parts of the circuit are involved in initial focussing operations, and the raising of the lens assembly when the beam is interrupted.

The sequence of events commences when a "lens down" instruction from MCPR is applied to pin No.6. This results in a voltage being applied to the lens down circuit by the control circuit, forcing the motor to gradually lower the lens in accordance to the time constant. Although the servo circuits are initially inactive due to the absence of focus error input signals, these error signals soon commence to appear. During this early stage the AC servo loop will become active while the lens is being lowered. Once the lens reaches the point of correct focus, the S-shaped curve detector circuit transfers that data to the control circuit, resulting in a switch over to the DC servo loop. The lens thus becomes 'in focus', and an 'in focus out' output signal appears at pin No.13, thereby triggering subsequent operations in other assemblies.

Description of Individual Circuit Components

1. Differential Amplifier

This circuit supplies offset at the point where the input error signal is amplified, and is also involved in phase compensation.

2. DC Servo and AC Servo Loops

The AC servo is applied prior to exact focussing (in focus) while the DC servo is applied after focussing only one circuit operating at any one time. The DC servo loop includes a gain control circuit which permits loop gain to be set to the value of greatest stability and optimum response.

3. Motor Drive Amplifier

This power amplifier stage for driving the focus motor is incorporated in the TA7210P power IC. Additional phase compensation is performed here to further stabilize the loop.

4. S-shaped Curve Detector Stage

This error detector stage has been so called due to the fact that the amount of error on each side the proper focussing position (in focus) varies in accordance to an S-shaped curve. And since the in-focus point is reached just prior to the zero-cross point of the curve, the comparator detects the point just prior to zero-cross, and passes an output signal on to the control circuit.

5. Control Circuit

Comprised of 4 comparators and a NAND flip-flop, this circuit supplies the lens-up command from the MCPR, and the loop switching SW and lens-down signals from the S-shaped curve detector signal.

6. Lens-Down Circuit

This capacitor/resistor circuit controls the gradual lowering of the lens by charging and discharging operations.

7. In Focus Detector and Lens Protection Circuit

Besides indicating that the focus servo in operation, this circuit also forces the focus motor to raise the lens (by applying a positive potential to the servo amplifier) if the laser beam should accidently be interrupted.

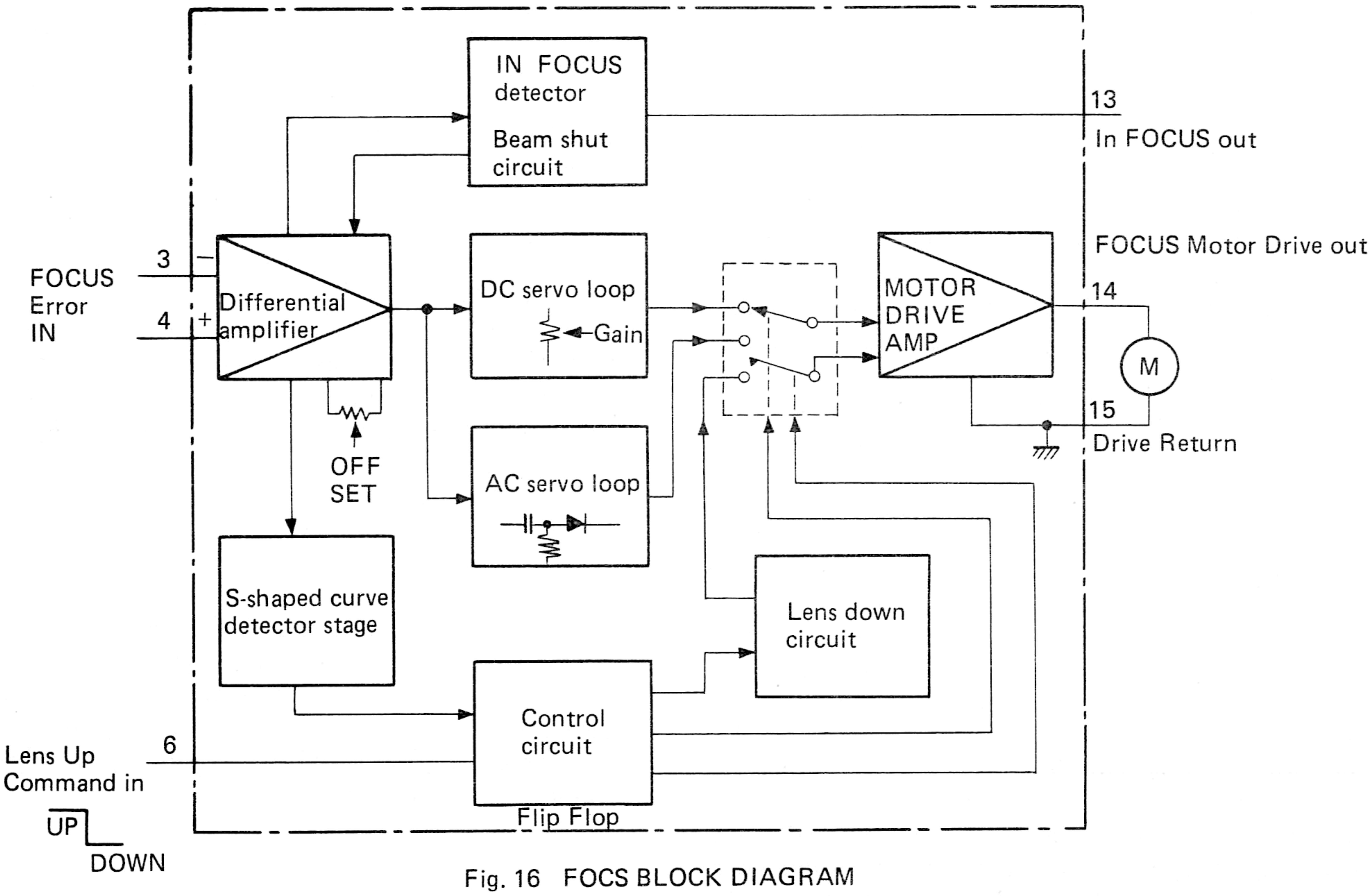


Fig. 16 FOCS BLOCK DIAGRAM

9.6 TRKG

1. Differential Amplifier

The function of this circuit is to provide amplification of the tracking error signal (an error signal proportional in size to tracking and lens position deviations) from the head amplifier (HEDA). This amplifier is also equipped with a detector offset circuit which compensates any differences between the 2 photo detectors.

2. Amplifier/Equalizer and Drive/Equalizer Stages

Both of these amplifier stages are equipped with equalizer circuits for stable servo application (mirror frequency response compensation). The amplifier/equalizer also includes a loop gain control VR, while the drive/equalizer (which corresponds to the power stage of an audio amplifier) is incorporated in a power IC.

3. Zero Crossing Detector and Jump-Back Pulse Generator

During the stop motion mode, a jump-back command from the MCPR applies a DC signal to the tracking mirror. The zero crossing detector subsequently informs the jump-back pulse generator that the jump-back to the adjacent track has been made. This results in the pulse generator applying a DC voltage to the loop, thereby leaving the loop open. This loop is closed again on command from the zero crossing detector.

4. Loop Switching Control Stage

This circuit controls the switch which opens the loop during search and jump-back modes. The loop may also be opened manually by the O/L ↔ L/L switch when making adjustments.

5. Carriage DC Loop Amplifier

This amplifier stage is employed in applying the low frequency components of the TRKG error signal to CARG.

Operating Principle of the TRKG Servo Control Circuit

As the name implies, the TRKG Servo is a servo control circuit used to maintain the laser beam right on the track at all times. As long as the beam remains aimed directly onto the track, the amount of overlap to left or right (onto A and B photo detector elements on both sides of the track) will be more or less equal. Any deviation to the left or right, however, will produce a difference in the amount of overlap in one direction or the other. On the basis of this differential signal, the TRKG servo circuit drives a mirror to change the direction of the laser beam, thereby keeping the beam aimed directly onto the track. In addition, compensation of mirror characteristics via the equalizer ensures stable servo operation.

This TRKG servo control operation may be more easily understood by a description of the stop motion mode. During normal play mode, the spiral track is traced from the inner circumference outwards under the control of the TRKG servo. During stop motion mode, however, the same video image must be displayed while the disc continues to rotate. And since a single video image is stored in one circumference of track, the same image may be displayed by jumping back one track after completing a single cycle. This is achieved by applying a jump-back command signal from the MCPR to the TRKG servo circuit. The TRKG servo loop is subsequently opened temporarily, and a DC voltage is applied to the mirror. Upon detection of completion of stop motion mode, the loop is closed again and the DC voltage cut.

Slow motion modes (SLOW FWD and SLOW REV) are also operated on the same principle, the frequency of jump-back steps being varied.

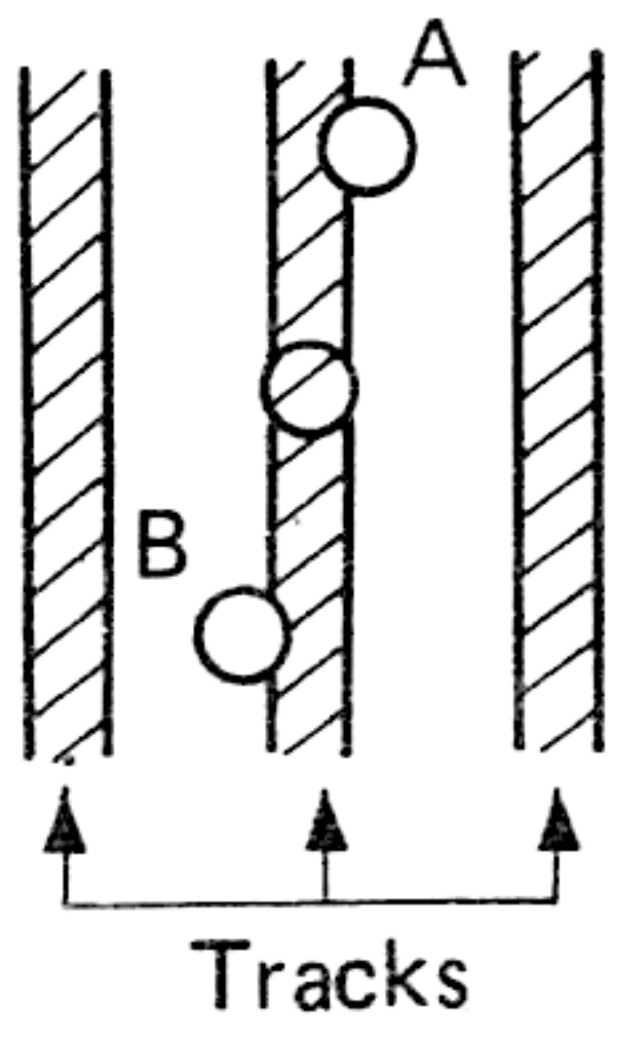


Fig. 17

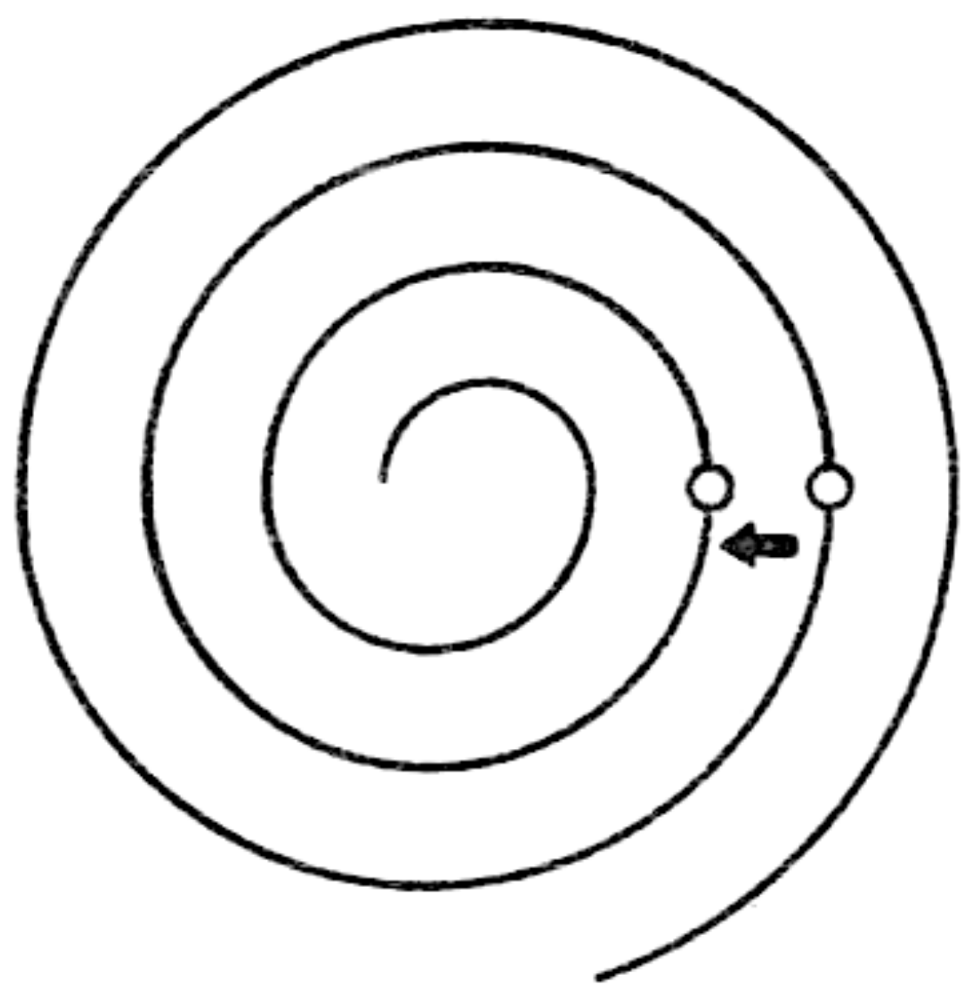


Fig. 18

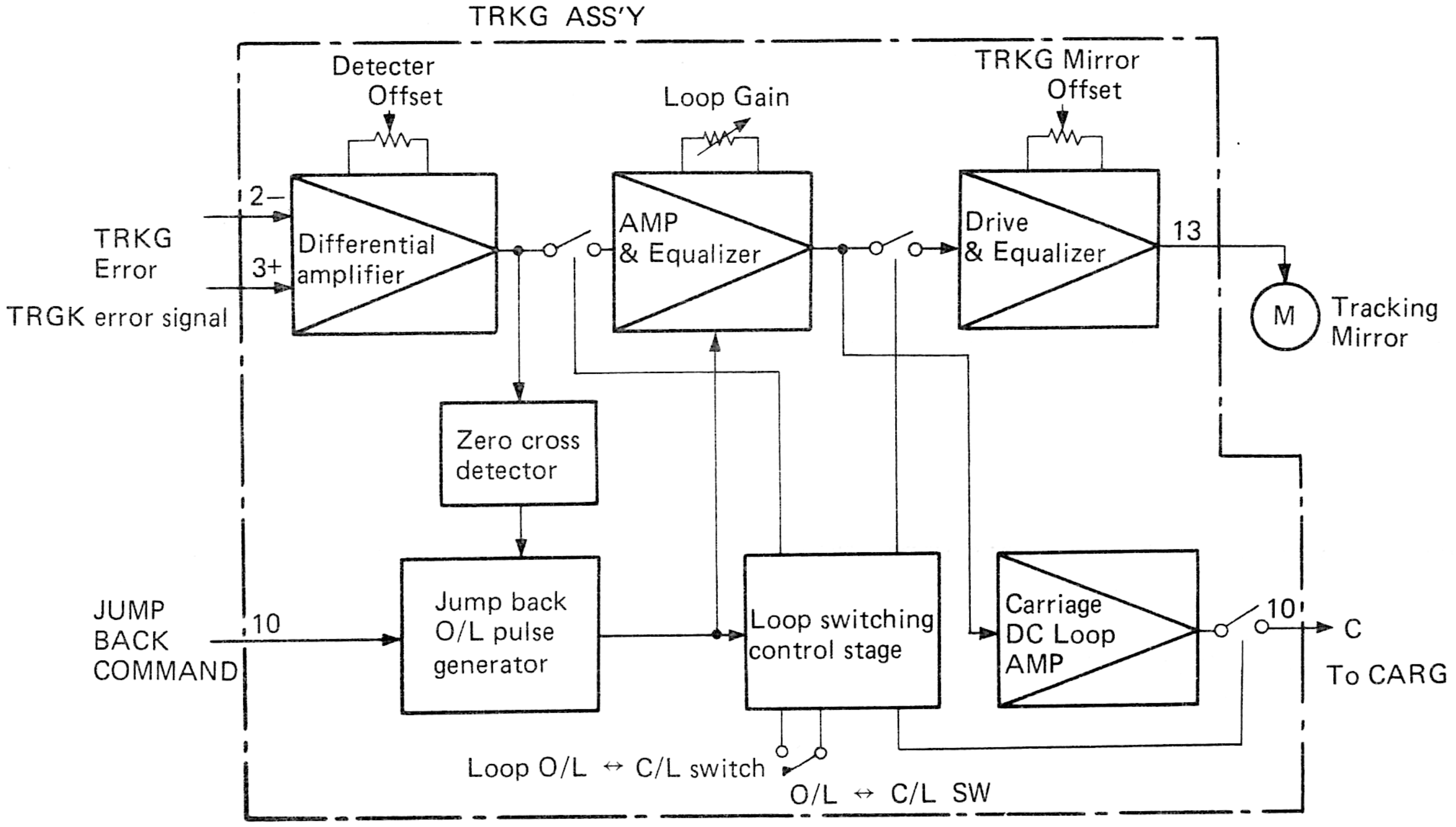


Fig. 19 TRKG BLOCK DIAGRAM

9.7 CARG

CARG Movements

1. When the video disc is in the park position, the CARG mechanism closes SW_4, reduces the loop gain, and prevents the carriage motor from operating.
2. For high speed transport of the CARG mechanism during search and scan modes, speed and direction instructions are received from the microprocessor, resulting in the required signals being transferred to the carriage motor.
3. When the TRKG loop is closed during play and stop modes, the tracking error DC components shift the CARG mechanism to trace the disc track.

CARG Operation

1. When in the park position, SW_4 is closed by a RUN command ($SW_1 \sim_3$ will be open at this time), and the tracking servo loop will be open (not shown in the TRKG circuit board diagram). The drive amplifier output will then be fed back to the amplifier input (negative feedback), the loop gain will drop, and the motor will remain inactive. In any other position (apart from PARK), the run input signal will become "H", thereby turning SW_4 off to permit the motor to rotate.
2. When tracking error is off:
   CARG mechanism transport to either the inside or outside position will be determined by the rotational direction of the carriage motor, which in turn is determined by whether a (+) or (−) voltage is applied to the drive output (DRIVE OUT). Transport speed will be determined by the motor rotational speed, which in turn is determined by the voltage applied to DRIVE OUT.
   For transport to INSIDE (REV), the REV input is switched to "H" by command from the microprocessor, resulting in only SW_3 being turned on, and a (−) voltage being applied to DRIVE OUT. For transport to OUTSIDE (FWD), the FWD input signal is made "H", resulting in only SW_2 being turned on, and a (+) voltage being applied to DRIVE OUT.
   Transport speed is determined by selection of a speed command (fast, mid, slow, play, variable) and the subsequent changing of the D-A converter analog output.
   For fast speed transport to REV (INSIDE), for example, $SW_{1,\,2}$ and $_4$ are turned off, and SW_3 turned on; $\overline{\text{FAST}}$ INPUT becomes "L", and $\overline{\text{MID}}\sim\overline{\text{PLAY}}$ become "H". The D-A converter output is thus passed via SW_3 to the adder (+), the applied voltage then serving as a reference voltage for operation of the speed loop, and subsequent rotation of the motor.
3. When tracking servo loop is closed (play, stop, slow motion modes):
   Tracking error DC components from the TRKG circuit board are compensated (for loop characteristics) by the equalizer circuit and applied to the adder (+), thereby activating the speed loop. The CARG mechanism is consequently shifted to a position where it can operate at the center point of the TRKG mirror. During play mode, the tracking DC error signal is applied to the adder (+) together with an "L" $\overline{\text{PLAY}}$ command and "H" FWD command from the microprocessor. The D-A converter output is consequently passed via SW_2 only and applied to the adder (+) to activate the speed loop.
   During slow motion mode, SW_1 is turned on, thereby cutting the D-A converter output to result in the DC voltage from VARIABLE being applied to the adder (+).
4. The speed loop includes the adder, amplifier, carriage motor, motor tacho generator, and the notch filter. The output of the tacho generator which detects changes in the rotational speed of the motor is fed back (as negative feedback) and compared with a reference voltage. The loop is activated in a way that will reduce this difference to zero in order to obtain a constant motor rotational speed proportional to the reference voltage. The purpose of the notch filter is to attenuate the motor's mechanical resonance output.

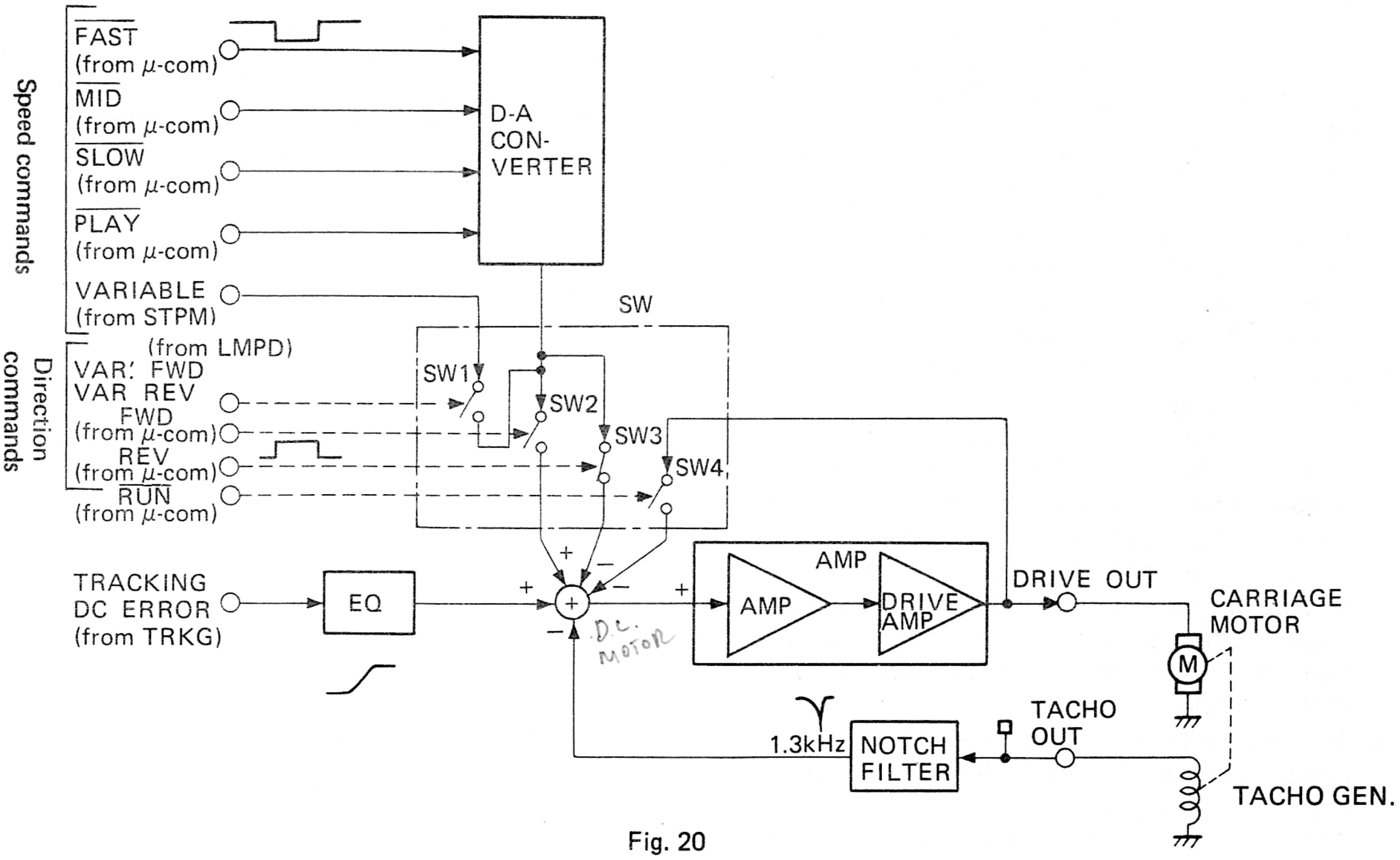

Speed commands
FAST (from μ-com)
MID (from μ-com)
SLOW (from μ-com)
PLAY (from μ-com)
VARIABLE (from STPM)
Direction commands
(from LMPD)
VAR' FWD
VAR REV
FWD (from μ-com)
REV (from μ-com)
RUN (from μ-com)
D-A CONVERTER
SW
SW1
SW2
SW3
SW4
TRACKING DC ERROR (from TRKG)
EQ
+
−
D.C. MOTOR
AMP
AMP
DRIVE AMP
DRIVE OUT
CARRIAGE MOTOR
M
1.3kHz
NOTCH FILTER
TACHO OUT
TACHO GEN.

Fig. 20

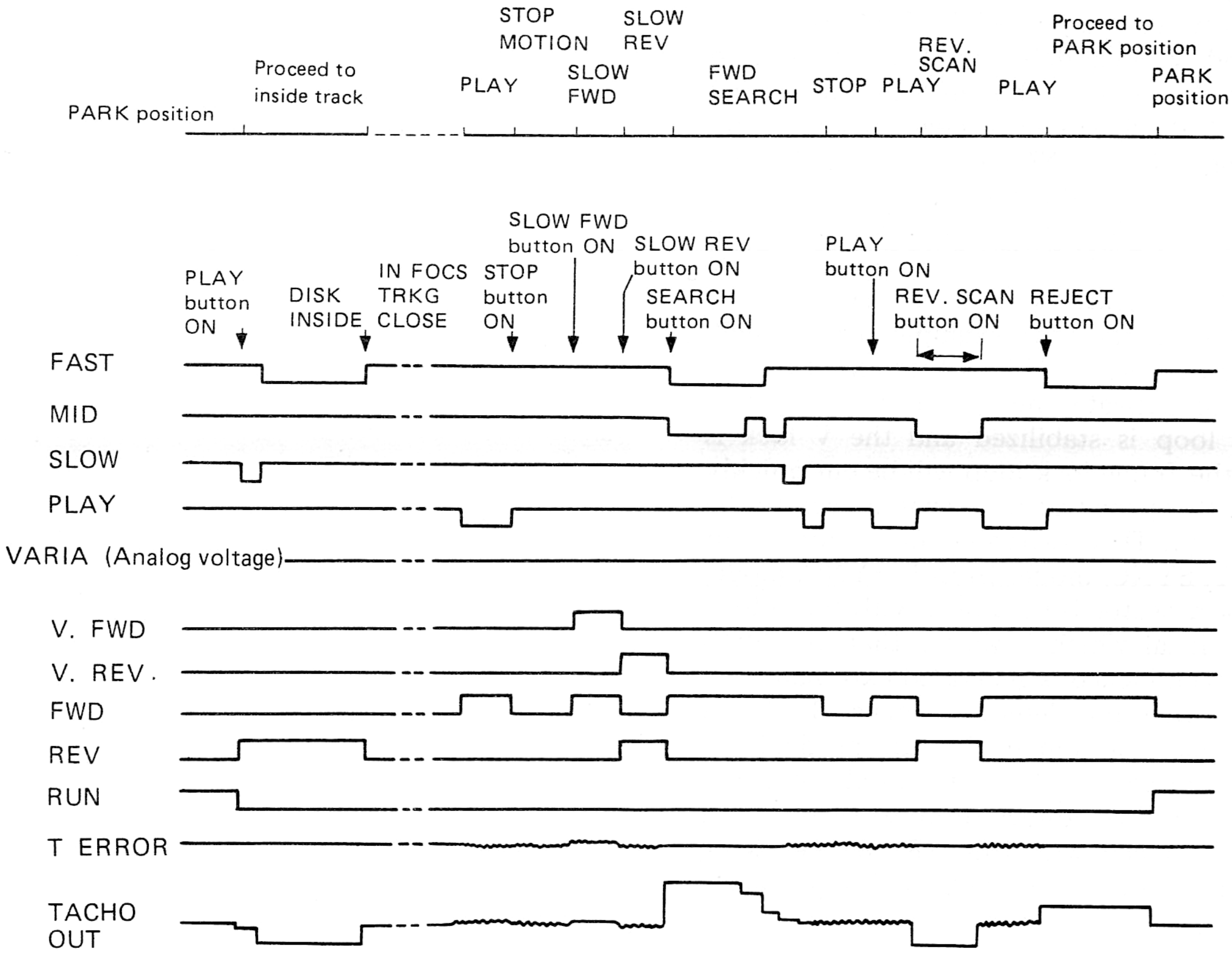

PARK position
Proceed to inside track
STOP MOTION
PLAY
SLOW FWD
SLOW REV
FWD SEARCH
STOP
REV. SCAN PLAY
PLAY
Proceed to PARK position
PARK position
PLAY button ON
DISK INSIDE
IN FOCS TRKG CLOSE
STOP button ON
SLOW FWD button ON
SLOW REV button ON
SEARCH button ON
PLAY button ON
REV. SCAN button ON
REJECT button ON
FAST
MID
SLOW
PLAY
VARIA (Analog voltage)
V. FWD
V. REV.
FWD
REV
RUN
T ERROR
TACHO OUT

Fig. 21

9.8 SPDL

1. The SPDL servo circuit consists of (1) a frame lock loop, (2) H lock loop, (3) tacho loop, (4) H and V lock detectors and free-run detector, plus a reference signal generator (REF. SYNC. GEN.).
2. This REF. SYNC. GEN. generates the horizontal synchronizing signal (reference signal for the SPDL servo circuit) and a sub-carrier signal. The output signal is applied to the rear panel synchronization selector switch used to select INT or EXT reference signal.
3. The frame lock loop prepares the vertical synchronizing signal (V) from the REF. SYNC., and compares it with the REF. SYNC. horizontal synchronizing signal (H) to produce frame pulse signals. These pulse signals are then compared (phase comparison) with P.B frame pulse signals obtained (as described earlier) from the P.B SYNC. prepared by separate synchronization of video playback signals, thereby forming a servo loop. Note that this loop is not used during INT. SYNC. mode.
4. The H lock loop (2) forms a servo loop by phase comparison of the REF. SYNC. H signal and P.B SYNC. H signal.
5. The tacho loop (3) on the other hand, forms a servo loop by frequency comparison of the intervals between successive P.B SYNC. H signals.
6. The H and V lock detectors (4) are used to check that the phase of the reference (REF) and playback (P.B) signals have been locked. Note that during INT. SYNC. mode or CLV disc playback, or when the tracking servo loop is open, the V lock detector is reset, and will supply lock signals even if there is no vertical lock. Before vertical lock is achieved during EXT. SYNC. mode, for example, the V lock detector interrupts the H lock loop (2) at S_4 and opens S_3 to activate the frame lock loop (1). Once the loop is stabilized and the V lock is checked, the frame lock loop will be cut quickly at S_3, and S_4 opened again to switch back to the H lock loop. This switching does not occur during INT. SYNC. mode. In INT. SYNC. mode, the H lock detector is used only with the H lock loop; the signal which indicates that the SPDL servo has been locked is generated externally.
7. When the free-run detector opens S_1 by a "RUN" signal, and applies the run speed adjustment VR voltage to the differential amplifier, the motor terminal voltage (proportional to rpm speed) is balanced with this VR voltage. Note that S_2 will be open. During CLV disc playback, S_5 is opened by a "CLV" signal, and the inner to outer circumference free-run rpm speed is varied continuously by the carriage potentiometer voltage. When the in focus signal is applied, S_2 is closed to include the motor drive amplifier in the H lock loop described earlier, thereby muting the free-run loop.

DISC SPINNING AT 1800 RPM

SPDL BLOCK DIAGRAM

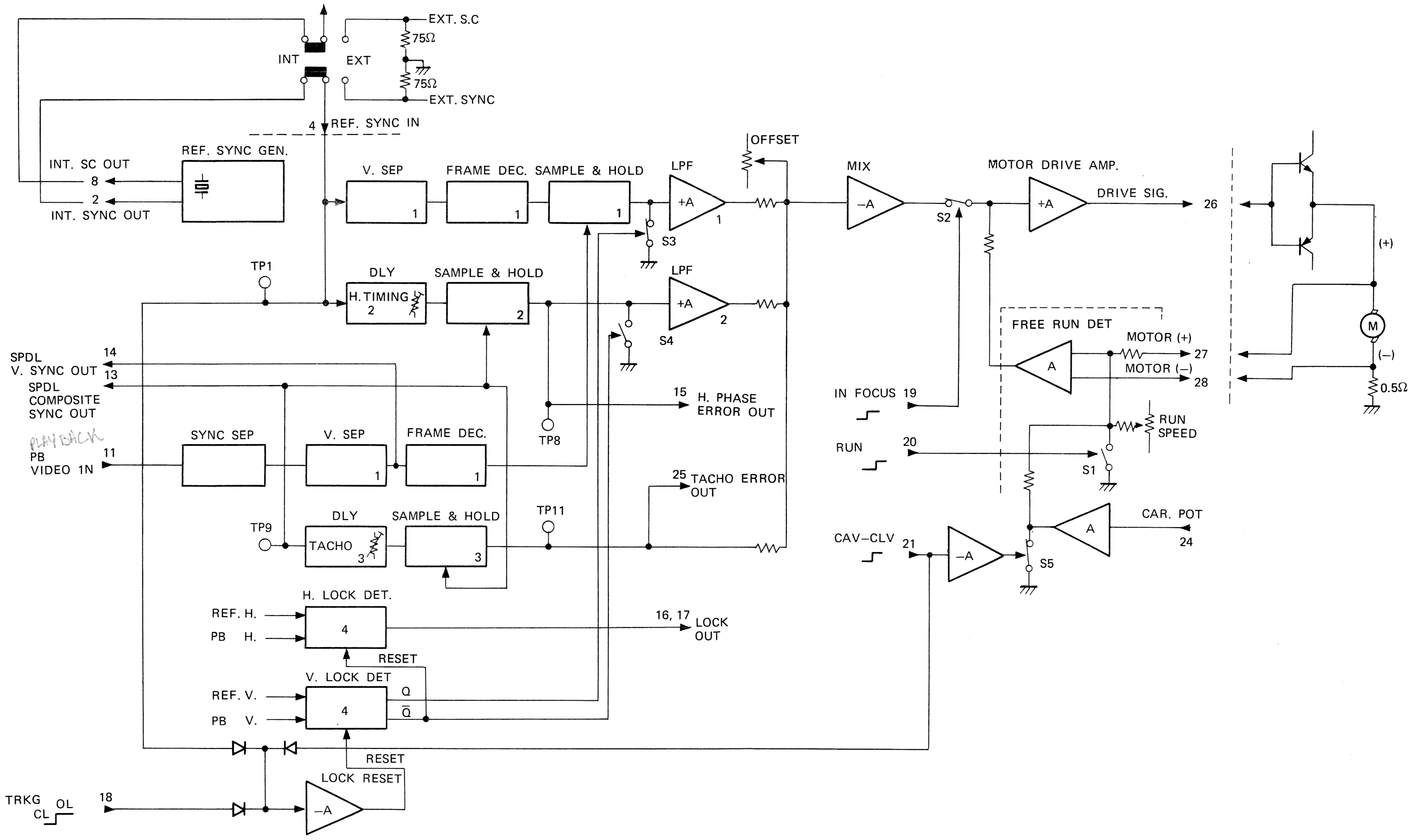


Fig. 22

9.9 VTBC

1. Purpose of the VTBC Circuit

The VTBC circuit (which corresponds to the tangential servo circuit in conventional mirror systems) is used to compensate time base errors contained in the playback video signal in order to obtain a normal playback color image. In order to achieve this objective, the VTBC circuit features a charge-coupled device (CCD) in a pure electronic circuit board which offers far greater stability than the conventional mirror systems containing mechanically movable parts. Furthermore, the range in which time base error may be compensated is far wider than any conventional system.

2. Basic Composition of the VTBC Circuit

The major component parts of the VTBC (video time base corrector) circuit include the general adjustment circuit for the open loop control system which operates in proportion to the amount of phase difference in the horizontal synchronizing signal obtained from the spindle servo system, and the video signal time base error compensation circuit which also includes the fine adjustment circuit for the closed loop servo system controlled by the phase difference signal formed upon detection of a phase difference in the output signal burst. In other words, the basis for VTBC circuit operation involves the input horizontal synchronizing signal being compared (phase comparison) with a reference horizontal synchronizing signal to obtain an error signal (in the SPDL circuit) which is then added as the open loop error signal to the error signal of the main loop consisting of the closed loop servo system controlled by the phase difference in the output burst signal. The eccentric error components (large amplitude components) are thereby cancelled.

At the present, this system is capable of compensating for up to 30μsec. of time base error. The time base error compensation element employed in this VTBC circuit is a variable delay circuit equipped with the charge-coupled device (CCD), and is capable of varying the delay time of the video signal passing through it (by purely electronic circuitry) according to changes in the frequency of the CCD drive clock.

As can be seen from Fig. 23 (basic composition which outlines the fundamental VTBC operating principles), the basic VTBC structure is a PLL circuit with an input reference signal of 3.58MHz, and the VDL corresponding to the VCO employed in normal PLL circuits. In other words, the time base error contained in the input video signal applied to the video input may be considered corresponding to the external interference applied to the PLL circuit, and the VDL as a VCO circuit responding to phase differences in the burst signal. Consequently, the time base error components in the input video signal (external interference) will be contracted in accordance to the PLL circuit response characteristics to obtain a compensated output video signal at the output, although in this case residual phase error in respect to the 3.58MHz reference signal will exist.

The error signal obtained by compressing the horizontal synchronizing signal applied to the other input of the adder circuit (the signal formed by detecting time base error in the input video signal) does not belong to the basic PLL circuitry (since no closed loop is formed). It does, however, have the capacity to detect large amplitude time base error components (which cannot be corrected by this kind of PLL system), and to compress them by proportional control within the correctable dynamic range of the closed loop system.

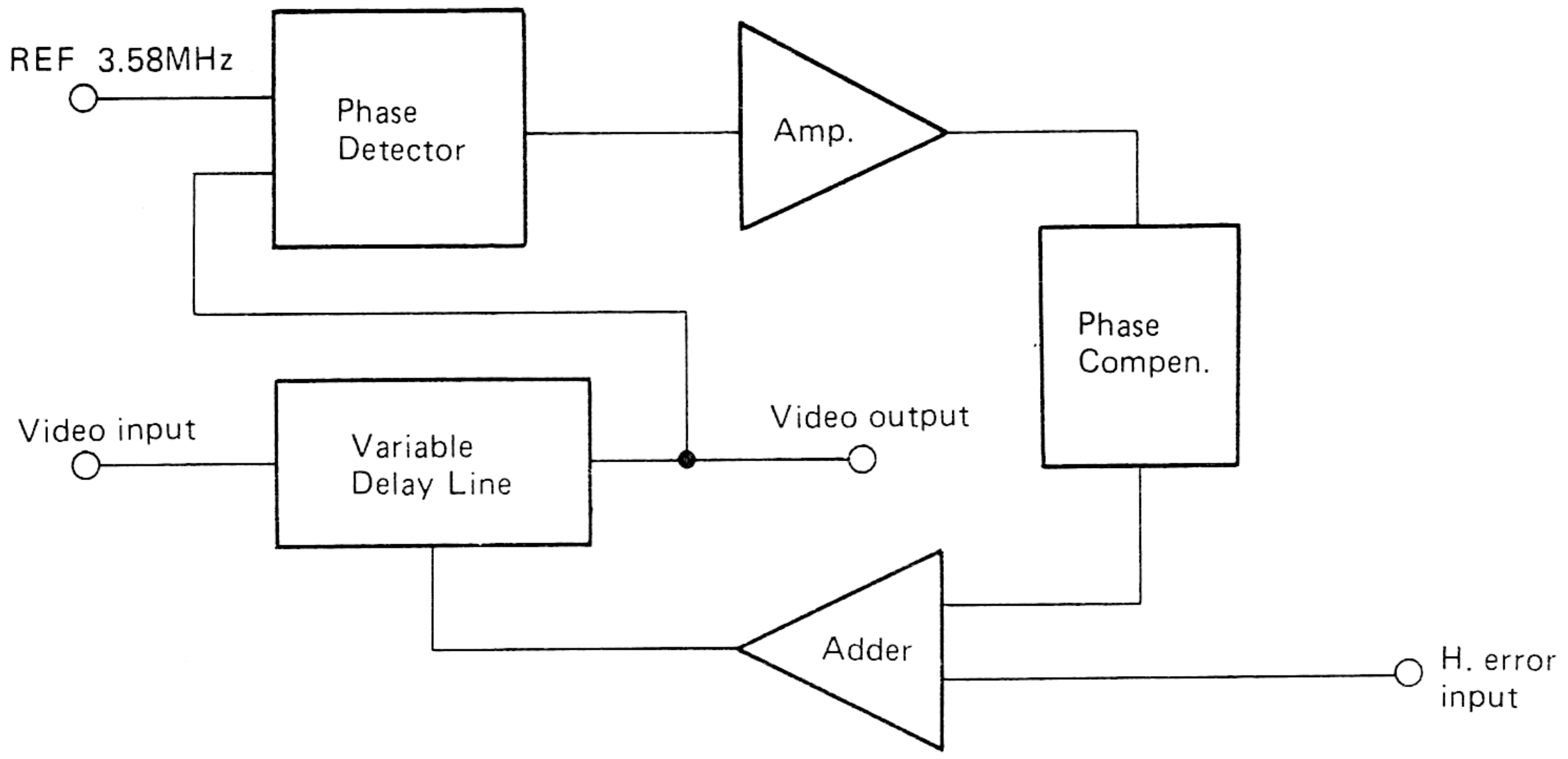


Fig. 23

3. VTBC Structure and Operation

The overall block diagram for the VTBC circuit is outlined in the appendix diagram Fig. 24. As has already been described, this circuit contains a horizontal synchronizing signal phase difference open loop compensation circuit which serves as a general adjustment circuit (and centered around the CCD equipped variable delay circuit), and a burst signal phase difference closed loop servo circuit which serves as a fine adjustment circuit. The operation of this basic structure will be described in accordance to the block diagram shown in appendix Fig. 24, and followed by an outline of the composition, purpose, and operation of individual blocks.

The video signal obtained from the VDEM prior to compensation undergoes synchronizing pulse separation in the SPDL, and is then compared (phase comparison) with a reference horizontal synchronizing signal to obtain a horizontal synchronizing phase difference signal. The reference signal employed here is obtained by dividing a signal from the same oscillating source as the 3.58MHz reference signal (to be described later), and which has been synchronized with this reference signal. The error signal applied to the VTBC H error input from the SPDL circuit is level adjusted by VR_5, passed through an amplifier (27) and applied to the 15.75kHz notch filter (28). The purpose of this notch filter is to eliminate noise components which are synchronous with the horizontal synchronizing signal. If it was not included in the circuit, the variable delay elements would be also activated by the 15.75kHz pattern noise components, resulting in a peculiar form of color irregularity in the playback video image.

The amplifier (27) output is also applied to the drop out detector circuit (31). The presence of any drop-outs in the separated playback synchronizing signal would result in the generation of very sharp spike noise in the error signal after the phase comparator stage. This would consequently cause loss of stability in the playback image, and deterioration in color. In order to avoid the effect of drop outs, a pre-value hold circuit (29) driven by output signals from the drop out detector (31) and passed via an interface circuit (32), holds on to the previous value whenever a drop out is detected. The pre-value hold circuit (29) output is then passed via a low-pass filter (30) to remove unwanted high frequency components before being applied to the adding amplifier (22) together with the closed loop error signal. Note that the cancellation level may be adjusted by VR_5.

In order to prevent mutual interference (at DC level) between the horizontal synchronizing phase error signal and the closed loop signal, a coupling capacitor (C_{38} in the circuit diagram) is employed to permit the passage of AC components only. The adding amplifier (22) output is passed via an open/close switching circuit (23) to the control voltage input of the VCO (24). The output clock of this VCO serves as the main oscillator used to drive the CCD, and is capable of oscillating at frequencies ranging from 7.5MHz to 15MHz, the center frequency being 10MHz. The VCO output clock is divided into a 4-phase clock by the clock timing generator (25) and then passed via a driver (26) to drive the CCD. Hence, the adding amplifier (22) output corrects the time base error in the input signal by varying the amount of delay in the variable delay line in such a way so as to cancel out the time base error in the input signal.

By itself the above open-loop compensation circuit (horizontal synchronizing phase error signal) can only achieve an error compensatory accuracy equal to the precision of the horizontal synchronizing signal, no matter how much circuit adjustment is performed. To achieve greater accuracy, a closed loop fine adjustment circuit with signal burst phase compensation accuracy is required. However, the open loop compensation circuit is particularly effective in correcting the time base errors of large amplitude, and compresses these error signals to within the dynamic range of the closed loop compensation circuit.

Two of the variable delay line (2) outputs are added in the adder & video filter (3) where unwanted clock components (added in the variable delay line stage) are removed. The combined output is then passed via VR_{10} to the video amplifier (4) where an output level of 2Vp-p is obtained. Part of this output is reduced to a 1Vp-p level by a buffer amplifier (8) before being applied to the STPM circuit where it undergoes synchronizing separation, the resultant compound and vertical sync. signals being returned to the VTBC circuit. While the main video amplifier output is applied to the clamp/buffer circuit (5), and 3rd part of the output is also applied to a burst gate circuit (12) to form the signal for the burst-oriented closed loop system. The comp. sync. signal returned from the STPM circuit generates a gate pulse signal in the burst gate pulse generator (11) according to the timing of the burst signal present in the video signal, and a color burst signal is extracted from the video signal by the burst gate (12). This color burst signal is then applied to a comparator (13)

VTBC BLOCK DIAGRAM

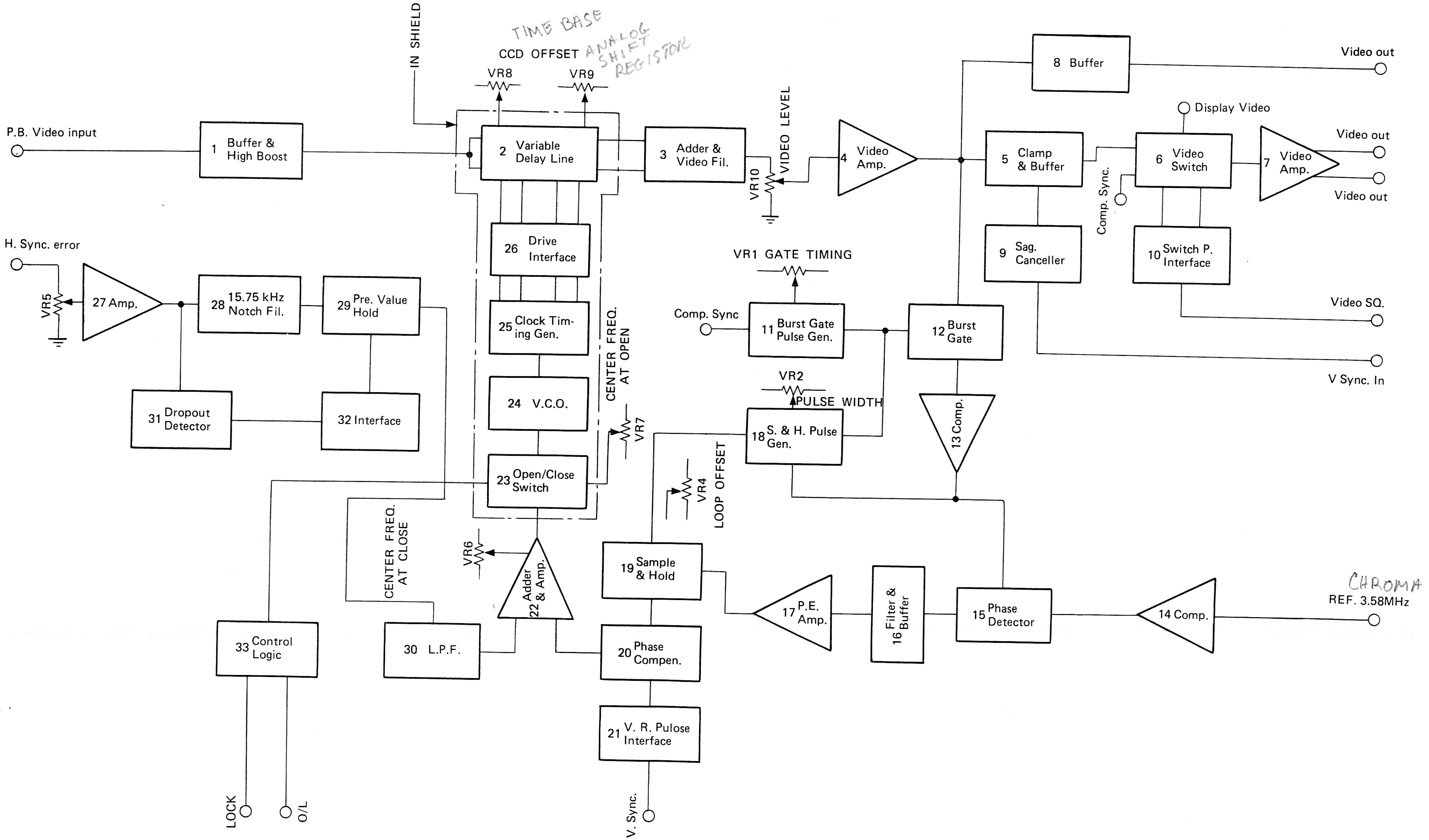


Fig. 24

where it is converted to TTL level, and is subsequently applied to the comparator input of a phase detector (15). The 3.58MHz reference signal, on the other hand, is applied to another comparator (14) where it also undergoes TTL level conversion before being applied to the reference input of the phase detector (15). The two signals are compared with each other in a digital phase comparison mode.

The phase detector (15) output is obtained as a pulse-width modulated signal which has been modulated in accordance to the 3.58MHz clock phase error. This output is consequently integrated in respect to 3.58MHz in the filter/buffer circuit (16), thereby converting the pulse width modulation to analog level. The filter/buffer (16) output is then amplified by the following amplifier (17) in a way that increases the level to about 8Vp-p after a 360° phase inversion, the resultant output being applied to a sample/hold circuit (19). Driven by a sample/hold pulse generator (18), the purpose of this sample/hold circuit is hold burst phase error signals within the horizontal synchronizing intervals. By applying burst gate pulse signals and integrated output signals form comparator (13) to an AND circuit in the sample/hold pulse generator (18), sampling pulse signals will only be generated during the period when burst phase error signals are present.

The sample/hold circuit (19) output is applied to the servo system phase compensation circuit (20), basically an integrating circuit which integrates phase error components within vertical zones, thereby enabling correction of time base errors of at least 0.28μsec. (that is, a single 3.58MHz cycle). Hence, the frequency response of this circuit is a very critical factor in the stability and quality of the playback video image.

The purpose of the V. reset interface circuit (21) is to discharge the integrating capacitor located in the phase compensation circuit (20) during the V blanking interval. Without this V reset circuit, unwanted DC components would accumulate on the integrating capacitor as a result of lack of error signal V zone, DC drift, and other forms of noise. This would lead to a drift in the phase compensator output DC level, thereby resulting in loss of stability of the central frequency for the servo system. The servo system would consequently deteriorate now and again, resulting in a very unstable playback video image. This is avoided, however, by periodically discharging the integrating capacitor so that the circuit will continue to operate at a central fixed frequency free of drift.

The phase compensator output is applied to the adding amplifier (22) to form a closed loop servo system via the open/close switch, VCO, clock timing generator, and drive interface circuit, thereby constituting a burst phase error compensatory circuit. Since the phase comparison in this closed loop system is oriented towards phase changes in the burst signals, the accuracy of this compensatory circuit is as high as the phase precision of the burst signals. The quality of the video signal after compensation, therefore, is sufficiently high enough for playback via normal color TV sets (the residual phase error being suppressed by a sufficiently high enough degree).

4. Composition and Operation of Individual Blocks

Composition and operation are described below in reference to the VTBC circuit diagram.

(1) Buffer and High Boost

Component parts:— Q_{47}, Q_{48}, $R_{200} \sim R_{206}$, R_{147}, R_{148}, $C_{73} \sim C_{75}$.

The purpose of this circuit is to pre-emphasize the high frequency components (of the 1Vp-p input video signal from the VDEM) due to be attenuated by the frequency response of the CCD circuit, and to attenuate the signal to the optimum level (0.4Vp-p) for passage through the CCD. It also applies the prescribed DC level (approx. 4V) to the CCD input, and serves as a buffer circuit which separates the playback video input from the CCD input signal.

(2) Variable Delay Line

Component parts:— Z_{19}, $R_{134} \sim R_{146}$, C_{55}, C_{56}, $C_{59} \sim C_{61}$, VR_8, VR_9.

This circuit is responsible for time base compensation of video signals passed through the CCD upon reception of modulated clock signals from the driver interface circuit (26), the CCD component employed being the Fairchild CCD321A-3. The CCD drive system involves applying in-phase input signals to 2 CCD delay lines, and driving each delay line by clock signals of mutually opposite phase, this being equivalent to doubling the sampling ratio. The V_{RA} and V_{RB} voltages determine the center value of the charge transferred within the CCD, the transfer charge in turn being determined by the difference between these voltages and the input voltage. Although VR_8 and VR_9 are used to adjust the V_{RA} and V_{RB} voltages, changes in these voltage levels can result in serious deterioration in the quality (DG, DP) of the output signal. For this reason, the maximum output level is taken as the optimum level.

(3) Adder and Video Filter

Component parts:— Q_{49}, Q_{50}, R_{149}, R_{150}, $L_8 \sim L_{10}$, $C_{62} \sim C_{66}$, VR_{10}.

This circuit adds the outputs of the two CCD delay lines, and cancels the clock signal of opposite phase. Any residual clock components are removed by a video filter, the filter cut-off frequency being 4.8MHz.

(4) Video Amplifier

Component parts:— $Q_{51} \sim Q_{53}$, $R_{151} \sim R_{157}$, C_{67}, C_{69}, C_{90}.

Following level adjustment by VR_{10}, the video signal is amplified by approximately 20dB by this amplifier circuit. The circuitry consists of a normal 3-stage direct-coupled amplifier plus two feedback loops (a DC feedback loop via R_{156}, and an AC feedback loop via C_{68} and R_{157}). Output level is adjusted to 2Vp-p.

(5) Clamp and Buffer

Component parts:— Q_{54}, Q_{55}, D_{30}, D_{31}, $R_{159} \sim R_{161}$, C_{69}.

A feature of CCD transfer is the fluctuation in output DC level with changes in clock frequency. Consequently, when the large amplitude time base error signals are corrected, DC level fluctuations of mainly 30Hz components are added to the video signals. The purpose of this circuit is to remove these fluctuations by "hard clamp" action.

(6) Video Switch

Component parts:— Z_{16}, ¼Z_{18}, R_{162}, R_{163}, R_{181}, R_{182}, R_{215}, $C_{70} \sim C_{72}$, C_{76}, L_{11}.

This circuit switches the main video signal to comp. sync. when a video squelch signal is received during squelch operations. DISPLY VIDEO addition is performed here through R_{163}, the video level at the addition point being 1Vp-p. The filter positioned prior to this is an 8MHz low-pass filter designed to further attenuate components not removed by the video filter.

(7) Video Amplifier

Component parts:— $Q_{59} \sim Q_{63}$, Q_{67}, $D_{36} \sim D_{39}$, D_{46}, D_{47}, $R_{185} \sim R_{199}$, R_{211}, R_{212}, C_{77}, $C_{94} \sim C_{97}$.

This is the output video amplifier stage with a fixed gain of 6dB (achieved by the R_{185} and R_{186} feedback loop). In terms of circuit composition, this is an operational amplifier with the Q_{62} current mirror coupled to the Q_{59}/Q_{60} differential pair. The Q_{67}, D_{46} and D_{47} circuit is used to limit the compound sync. during squelch operations in order to prevent leakage of the video signal. R_{192} and C_{77} form a phase compensation circuit with a value which influences the frequency response of the output signal. The video level when the output is terminated by a 25 ohm resistance through R_{198} and R_{199} is 1Vp-p.

(8) Buffer

Component parts:— Q_{58}, $R_{166} \sim R_{168}$.

This buffer circuit is an emitter-follower circuit used to attenuate the output of the video amplifier (4) to 1Vp-p, and apply the video signal to the STPM circuit.

(9) Sag Canceller

Component parts:— Q_{56}, Q_{57}, $R_{169} \sim R_{173}$, R_{158}, D_{29}.

The hard clamp performed in the clamp/buffer circuit also results in the generation of a strong sag. This sag may be largely diminished by shifting the clamp level in the minus direction in the V zone only. To achieve this objective this circuit makes use of the V. sync., shifting the clamp level for the V zone only by D_{29} after passing through the Q_{56}/Q_{57} interface circuit.

(10) Switch Pulse Interface

Component parts:— ½Z_{17}, $R_{176} \sim R_{180}$, R_{183}, R_{184}, $D_{32} \sim D_{35}$.

This is the interface circuit used to drive Z_{16} upon reception of the video squelch signal.

(11) Burst Gate Pulse Generator

Component parts:— Z_1, R_{13}, R_{14}, C_{91}, C_{92}, VR_1.

The purpose of this circuit is to delay the comp. sync. by about 6μsec., and to apply the gate pulse signals during the period when burst signals are present in the video signal. Circuit composition includes a pulse delay circuit with two one-shot multiples. The degree of delay may be varied by VR_1, and the output pulse width is set to 2μsec.

(12) Burst Gate

Component parts:— $Q_1 \sim Q_4$, $R_1 \sim R_{12}$, $C_1 \sim C_3$, L_1, L_2, D_1.

This circuit extracts burst signals from the output video signal by switching operations. The balanced output obtained by differential-pair switching is readily matched with the comparator input in the following stage. L_1, C_1 and R_1 form a low-Q 3.58MHz series resonance circuit, while L_2 and C_3 form a high-Q series resonance circuit, thereby determining the band-pass characteristics for the burst signals.

(13) (14) Comparators

Component parts:— Z_2, R_{40}, R_{41}, C_{108}, C_{101}.

In these two circuits, the burst signal applied to the gate, and the 3.58MHz reference signal from the SPDL circuit undergo TTL level conversion in order to match the outputs with the following phase detector. The maximum TTL level conversion attainable with the burst gate circuit (12) plus comparator (13) is −9dB in respect to the standard burst signal level.

(15) Phase Detector

Component parts:— Z_5, Z_6.

This circuit is designed to detect the phase difference between the comparator input and reference input in purely digital form. The output signal is a 3.58MHz PWM (pulse width modulation) signal modulated according to the phase difference.

(16) Filter and Buffer

Component parts:— Q_{12}, Q_{13}, R_{42}~R_{47}, L_4~L_7, C_{16}~C_{18}.

The PWM output signal from the phase detector may be converted to an analog signal by integration. This circuit employs a 3.58MHz integrating filter and processes the balanced phase detector output directly in order to effectively remove the carrier portion. The Q_{12}/Q_{13} emitter-follower serves as the impedance conversion circuit which enables the following amplifier stage to be used as a differential amplifier.

(17) Phase Error Amplifier

Component parts:— Q_{14}~Q_{19}, D_5~D_8, R_{48}~R_{62}, R_{213}, R_{214}, C_{19}, C_{79}~C_{81}.

Although the circuit composition is the same as the output video amplifier, the differential amplifier gain is set to 9.4dB. And since a differential gain of 6dB may be obtained, the apparent gain from input to output is 15.4dB.

(18) Sample/Hold Puse Generator

Component parts:— Z_3, Q_9~Q_{11}, R_{34}~R_{39}, L_{16}, C_{13}, C_{14}, VR_2.

The burst gate pulse signal and TTL level converted burst signal are applied to an AND circuit in order that sampling pulse signals be generated only during the presence of a burst signal. L_{16} and C_{13} form a burst signal integrating circuit, and levels exceeding the threshold level (set by VR_2) only during the presence of burst signals will appear at one of the Z_3 input terminals. Consequently, the sampling pulse rise point will be determined by the VR_2 setting level, while the drop point will coincide with the gate pulse rise point. Q_{10} and Q_{11} constitute the interface circuit used to drive the Q_{20} gate. The sampling pulse width is adjusted to 0.8μsec. by VR_2.

(19) Sample and Hold

Component parts:— Z_7, Q_{20}, R_{63}~R_{68}, C_{20}, C_{98}, VR_4.

This circuit samples and holds the output of the phase error amplifier (17) during the presence of a burst signal, C_{20} serving as the sampling capacitor. Since the feedback loop of this circuit is closed when the Q_{20} switch is closed, C_{20} will be charged up by the Z_7 output. When the Q_{20} switch is opened, thereby opening the feedback loop, a voltage follower will be set up across the terminals of C_{20}, thereby holding the voltage during sampling. In order to prevent the discharge of C_{20}, Z_7 is connected to an operational amplifier with an FET input.

(20) Phase Compensator

Component parts:— Q_{21}, Q_{22}, Q_{24}, Q_{25}, R_{69}~R_{73}, R_{80}~R_{84}, C_{21}~C_{26}.

C_{21}, R_{69} and R_{70} form a phase advancer circuit which compensates phase in the high frequency region, while C_{22} and C_{23} form an integrating capacitor stage which is discharged by Q_{21} and Q_{22} during the V blanking interval. Since this discharge is in respect to ground level, the DC level will be modulated by the V reset stage when the Z_7 output DC level is not exactly at ground level, resulting in a peculiar flicker in the top of the playback image. Note that the Z_7 output DC level is adjusted by VR_4.

(21) V Reset Pulse Interface

Component parts:— ½Z_8, Q_{23}, R_{76}~R_{79}, D_{11}, C_{27}, C_{28}.

This interface circuit drives the Q_{21}/Q_{22} switch by the vertical sync. signal.

(22) Adding Amplifier

Component parts:— ½Z_4, R_{106}~R_{108}, R_{110}~R_{112}, C_{38}, C_{57}, VR_6.

This is the amplifier stage which adds the closed loop error signal to the open loop error signal, using the minus input to the inversion amplifier as the adding point. The output DC level of this amplifier may be adjusted by VR_6, thereby designating the center frequency for VCO operation.

(23) Open/Close Switch

Component parts:— Q_{31}~Q_{34}, R_{113}~R_{120}, VR_7, D_{26}~D_{28}, C_{99}.

This switching circuit is used to open and close the servo system circuit. When the switch is closed, the adding amplifier output servo error signal appears on the emitter of Q_{34}, but when it is opened, a DC voltage set by VR_7 will appear on the emitter instead. When the Q_{31}/Q_{33} switching FET is closed, a low impedance signal from the emitter of Q_{34} is applied to the base of Q_{34}. Consequently, the voltage of the high impedance coupled VR_7 will not effect the signal. When the FET switch is open, however, the VR_7 setting voltage will become the controlling voltage since the R_{118} impedance is very much lower than the impedance when Q_{33} has been turned off. When the switch is open, the VCO center frequency may be set by VR_7.

(24) Voltage-Controlled Oscillator

Component parts:— Z_{10}, $Q_{35}\sim Q_{38}$, $R_{121}\sim R_{128}$, $C_{39}\sim C_{43}$, D_{48}.

Unlike regular VCO components where the oscillating frequency is varied in direct proportion to changes in the input voltage, the VCO employed in this circuit has been designed with a linear relation between the cycle time of the oscillation waveform and the input voltage. The reason for using this kind of VCO lies in the fact that the CCD delay time varies in proportion to the inverse of the clock frequency, and is indispensable if the control dynamic range is to be expanded while maintaining servo system linearity. Q_{35} and Q_{36} form a constant current circuit which applies a constant charging current to C_{40}. If the voltage across C_{40} exceeds the control voltage applied via R_{126}, a comparator will be activated, resulting in Q_{37} being turned on after a fixed delay time, and subsequently discharging C_{40} immediately. C_{40} is then charged up again, and the same sequence of events repeated, thereby maintaining an oscillating operation. Since the C_{40} voltage level is linear in respect to time, the change in cycle time will also be linear in respect to the input control voltage, resulting in a sawtooth waveform being generated at C_{40}. This sawtooth signal is then applied to another comparator where it is divided and compared with the input control voltage to obtain an output clock signal of 50% duty cycle.

(25) Clock Timing Generator

Component parts:— $Z_{11}\sim Z_{13}$.

This circuit generates the 4 types of clock signals required to drive the CCD. By making use of the Z_{11} and Z_{12} pulse delay times, clock signals of required timing and pulse widths may be prepared by the AND gate.

(26) Drive Interface

Component parts:— $Q_{39}\sim Q_{46}$, $D_{13}\sim D_{25}$, $R_{129}\sim R_{133}$, R_{220}, $C_{45}\sim C_{52}$, C_{58}.

While a 15Vp-p clock signal is required to drive the CCD, there is also a certain amount of idle capacitance (about 10pF to 30pF) on the CCD input terminal. This drive interface circuit is the circuit used to convert the TTL level signal to a 15Vp-p drive signal under these conditions. In order to drive the capacitance load, a push-pull circuit with a coupling capacitor in the input stage and a diode clamped switching transistor in the output stage is employed.

(27) Amplifier

Component parts:— ½Z_{9}, $R_{85}\sim R_{88}$, C_{29}, VR_{5}.

This circuit is an inverting amplifier stage designed to ensure flat amplication of the horizontal synchronizing phase error signal from the SPDL. Gain is 6dB. It also serves as an impedance matching buffer amplifier, the input level being adjusted by VR_{5}.

(28) 15.75kHz Notch Amplifier

Component parts:— Q_{26}, $R_{90}\sim R_{92}$, $C_{31}\sim C_{33}$, R_{209}.

This twin-T type 15.75kHz CR filter removes unwanted 15.75kHz components contained in the error signal.

(29) Pre-Value Hold

Component parts:— ½Z_{9}, Q_{27}, R_{93}, C_{34}.

When a drop-out occurs, this circuit holds the previous value by means of a hold pulse signal from the drop-out detector circuit. C_{34} is the hold capacitor, while Z_{9} is used as a voltage follower, thereby maintaining a very high input impedance.

(30) Low-Pass Filter

Component parts:— Q_{30}, $R_{103}\sim R_{109}$, $C_{35}\sim C_{37}$.

The purpose of this filter is to eliminate high frequency noise components from the error signal, and further improve the stability of the servo system. The filter used here is a Bessel filter with a 500Hz cut-off frequency.

(31) Drop Out Detector

Component parts:— Z_{14}, Z_{15}, ½Z_{8}, R_{89}, $R_{97}\sim R_{102}$, C_{30}, C_{44}.

The high frequency components of the drop-outs included in the error signal are filtered out by the C_{30}/R_{89} differentiating circuit, and the signal then converted to TTL level by the window comparator consisting or Z_{14} and Z_{15}. The pulse width is expanded by Z_{8}, thereby enabling drop-outs to be completely masked during the drop out interval.

(32) Interface

Component parts:— Q_{28}, Q_{29}, $R_{94}\sim R_{96}$, D_{12}, C_{93}.

This circuit is employed in TTL level conversion and Q_{27} drive.

(33) Control Logic

Component parts:— Z_{18}, ¼Z_{17}, R_{175}, circuit board switch.

This circuit drives the open/close switch (23) upon reception of signals from the SPDL and TRKG circuits. The open/close switching circuit may also be controlled by the circuit board switch.

MEMO

9.10 CONTROL SYSTEM

The control system consists of a number of different assemblies (described below) where the signals employed are mainly TTL level logic signals. The major functions of the control system may be summarized as follows:—

- Reception of operation command signals (from front panel push-buttons, remote control, and external control input).
- Control of servo circuits.
- FRAM# read out and display.

9.10.1 MCPR circuit board

(Refer to the Control System Block Diagram)

The MCPR circuit comprises the F8 microprocessor (3850, 3861 and 3853), a Read Only Memory and Display RAM. The microprocessor is connected to other control and servo circuit boards, the polarity of the signals employed being boutlined in the Control Signal Chart.

The only parameter requiring adjustment in this circuit board is the clock frequency. This is set to 2.025MHz (at 25°C room temperature) by the VC_1 control.

9.10.2 RAMB circuit board

(Again refer to the Control System Block Diagram)

This RAMB circuit is a 1k byte CMOS RAM equipped with a Nickel-Cadmium Rechargeable Battery to hold the memory contents after the normal power supply has been disconnected, or if the power is interrupted.

This assembly is connected directly to the MCPR circuit by means of flat cable and connector.

During test mode, this assembly is tested by self-diagnosis (see Program A).

9.10.3 DSPL circuit

(Refer to Control System Block Diagram)

The DSPL circuit is divided into the following 3 blocks.

a. Character Display

When the contents of the MCPR circuit Display RAM are applied to the Character Generator IC (DM8678), a character output is generated synchronized with the TV signal. This operation is performed by the Display Counter activated by the 0CLOCK.

b. Carriage Position Sensor

Carriage position is indicated by the potentiometer output voltage. The comparator is used to detect the INSIDE LIMIT and OUTSIDE LIMIT (the disc signal starting and finishing positions). Note that these 2 position output signals also contain forewarning output signals, viz. ANTICIPATE INSIDE and ANTICIPATE OUTSIDE.

c. Command Input

The function push-button data is transferred from the Transmitter IC in the LMPD circuit in serial form, and converted into 8-bit button data (command code, BIN A~D SEL A~D) by the Receiver/Decoder IC in the DSPL circuit.

External command code (DIO 0~7) is received after switching the INT/EXT signal.

9.10.4 DADT circuit

The DADT circuit (amplifier and comparator composition) converts the dump signal applied to AUDIO CH_2 into TTL level.

"0" level 2.5kHz

"1" level 5kHz

This dumping operation is described later under the Program C operational example.

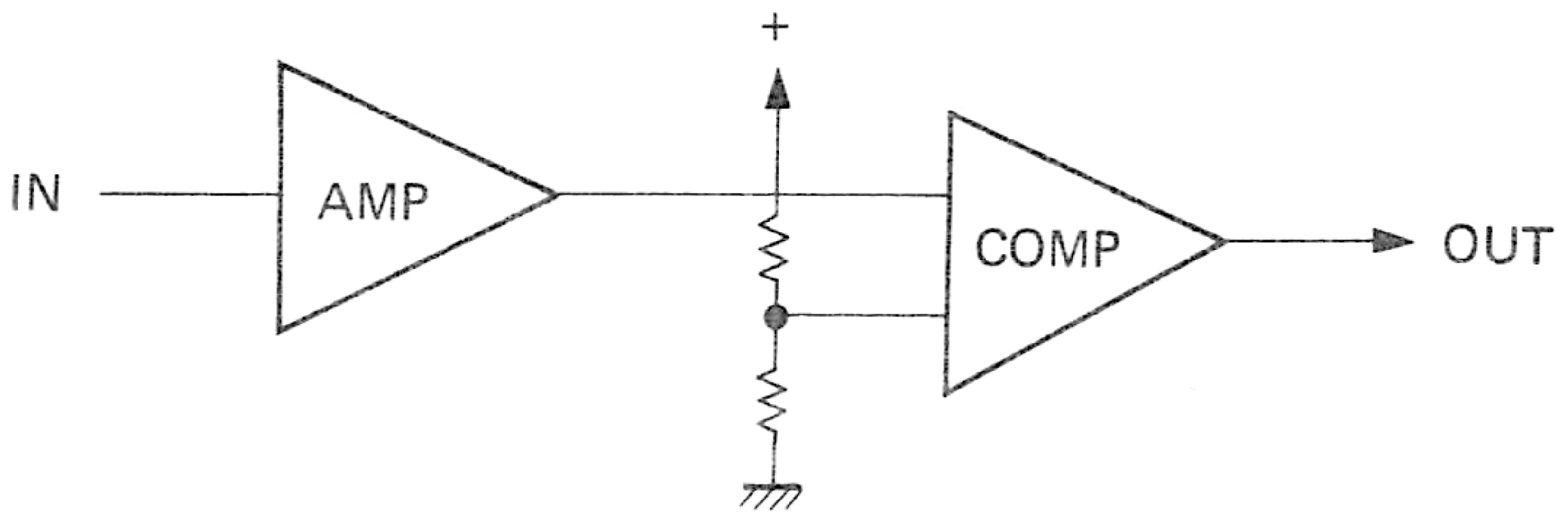


Fig. 25

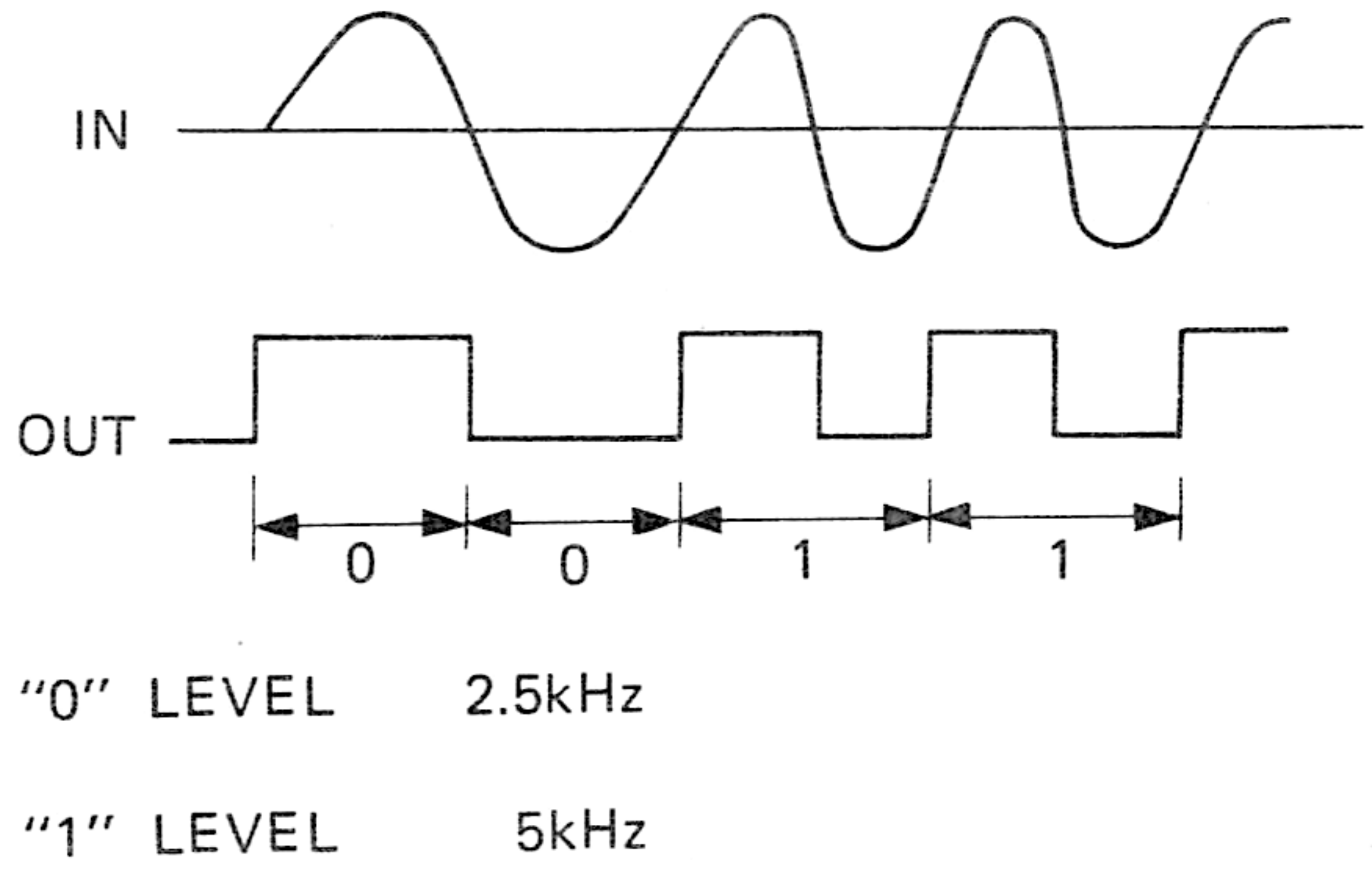
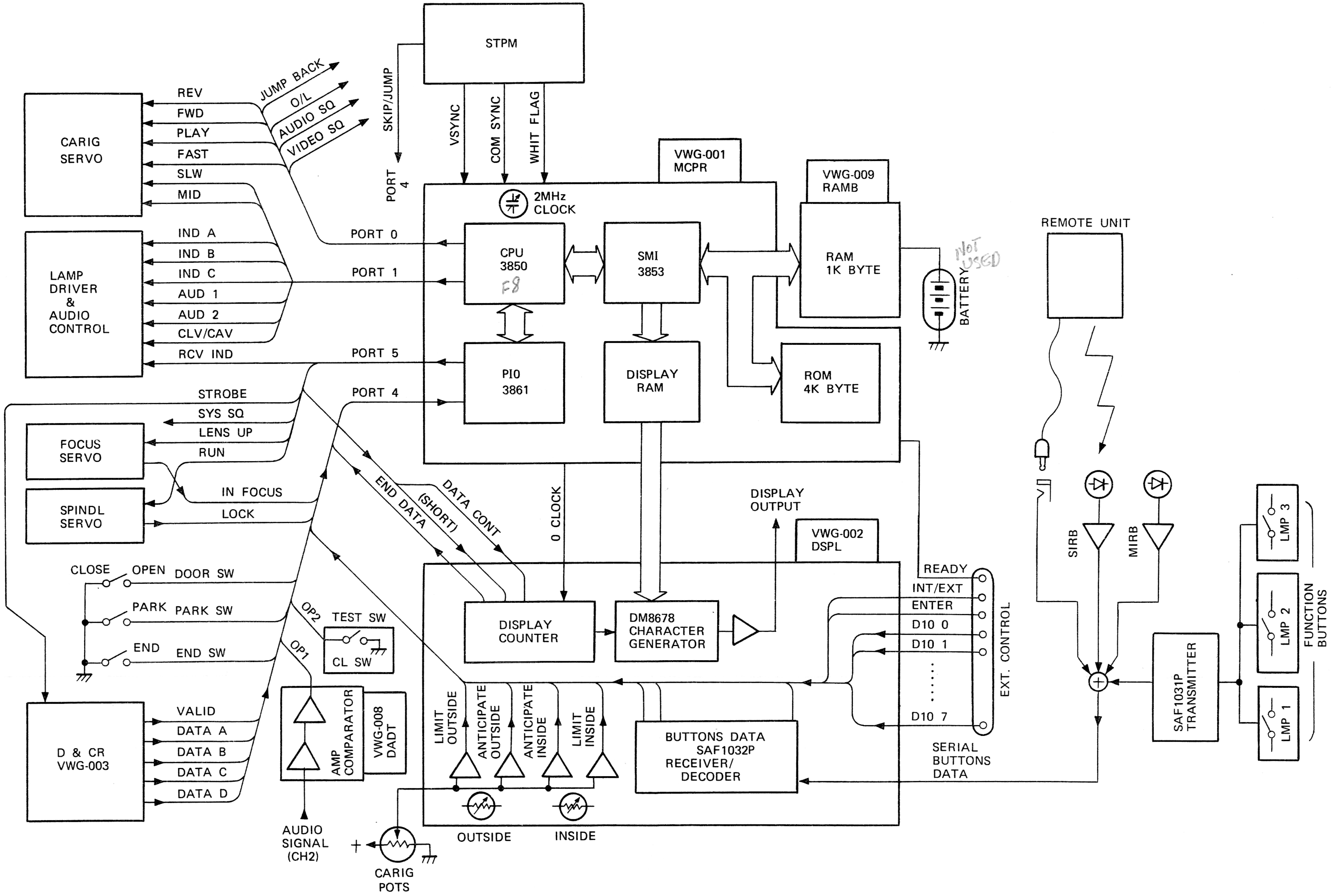


Fig. 26

CPU 3850 — F8- STATIC SENSITIVE

9.10.5 Control system diagram



9.10.6 Control system signal table

PORT 0

OUTPUTS

00	JUMP BACK
01	O/L CLOSE LOOP OPEN LOOP
02	AUDIO SQ SQ
03	VIDEO SQ SQ
04	REV *
05	FWD *
06	PLAY *
07	FAST *

PORT 1

OUTPUTS

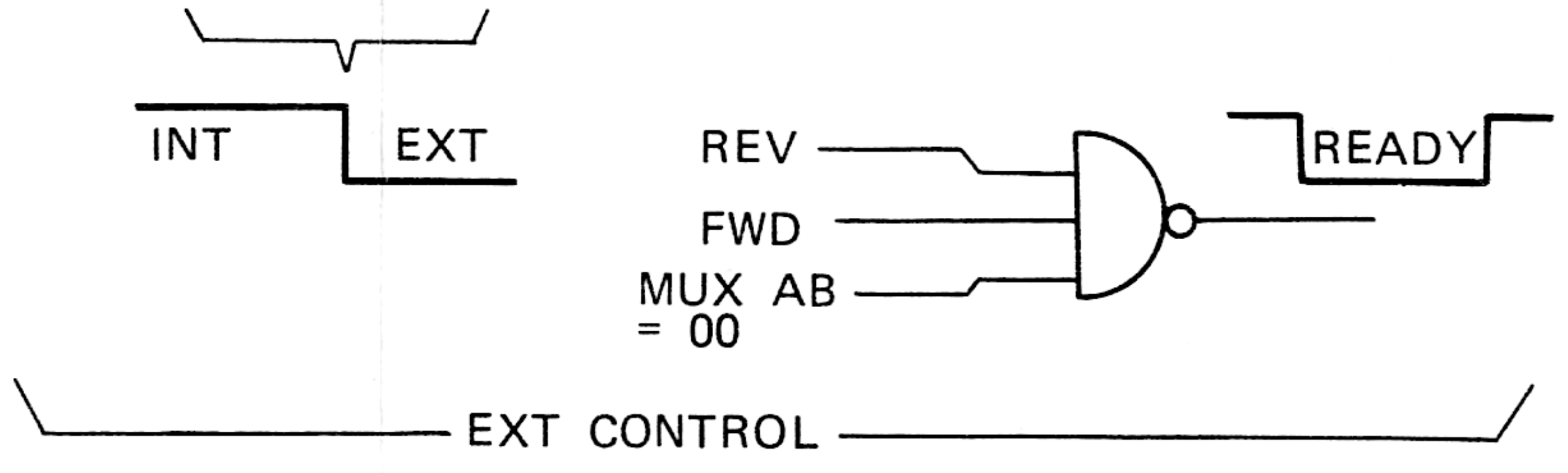
10	IND A
11	IND B
12	IND C
13	AUD 1 SELECT
14	AUD 2 SELECT
15	CLV/CAV CLV CAV
16	SLW *
17	MID *

NOTES: 1. ALL SIGNALS ARE TTL LEVEL HIGH "1" LOW "0"

INPUTS

PORT 4

	MUX AB = 0·0		MUX AB = 01	MUX AB = 10	MUX AB = 11
40	SEL D	DIO 0	INFOCUS FOCUS	END SW END	NC
41	SEL C	DIO 1	NC	PARK SW PARK	NC
42	SEL B	DIO 2	LOCK LOCK	END DATA END	NC
43	SEL A	DIO 3	NC	VALID DATA VALID	NC
44	BIN D	DIO 4	LIMIT OUTSIDE	DATA A	SKIP/JUMP
45	BIN C	DIO 5	ANTICIPATE OUTSIDE	DATA B	OP 2 RAM CLEAR
46	BIN B	DIO 6	ANTICIPATE INSIDE	DATA C	DOOR SW OPEN CLOSE
47	BIN A	DIO 7	LIMIT INSIDE	DATA D	OP1 DUMP DATA
	INT BUTTONS	EXT DATA			



INDICATOR

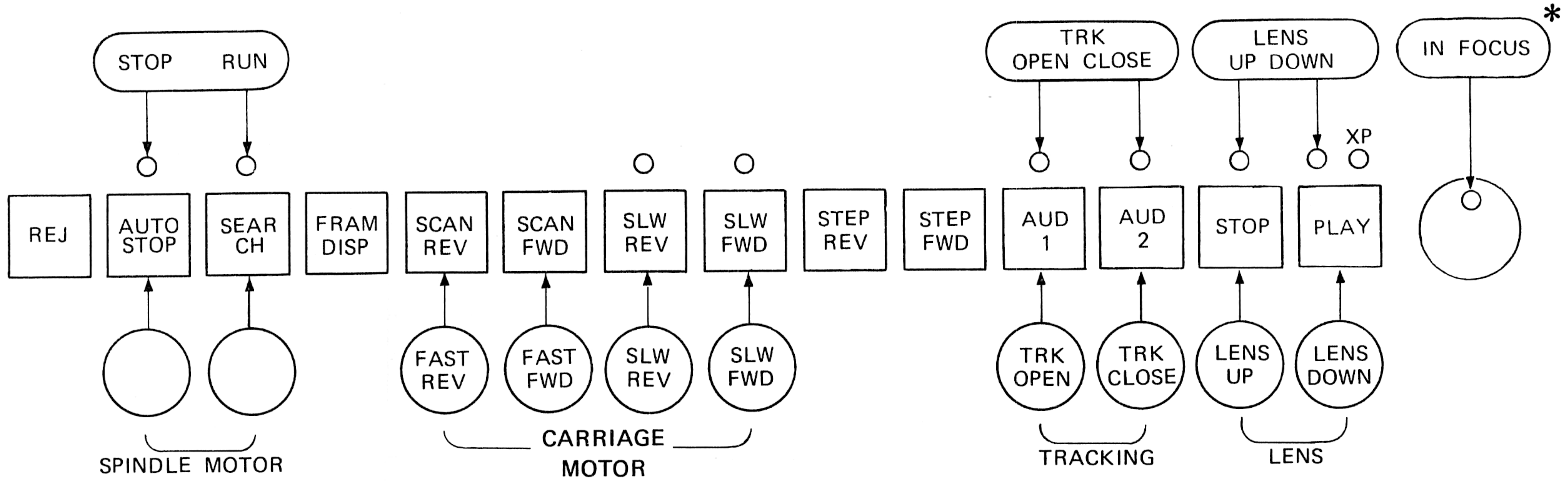
C	B	A	LAMP
0	0	0	VAR FWD
0	0	1	VAR REV
0	1	0	SEARCH
0	1	1	AUTO STOP
1	0	0	PLAY
1	0	1	STOP
1	1	0	
1	1	1	BLK

PORT 5

OUTPUTS

50	MUX B
51	MUX A
52	DATA CONT DISP
53	SYSTEM SQ SQ
54	RCV IND RCV
55	STROBE (SHORT DATA)
56	LENS UP DOWN UP
57	RUN RUN

TEST MODE



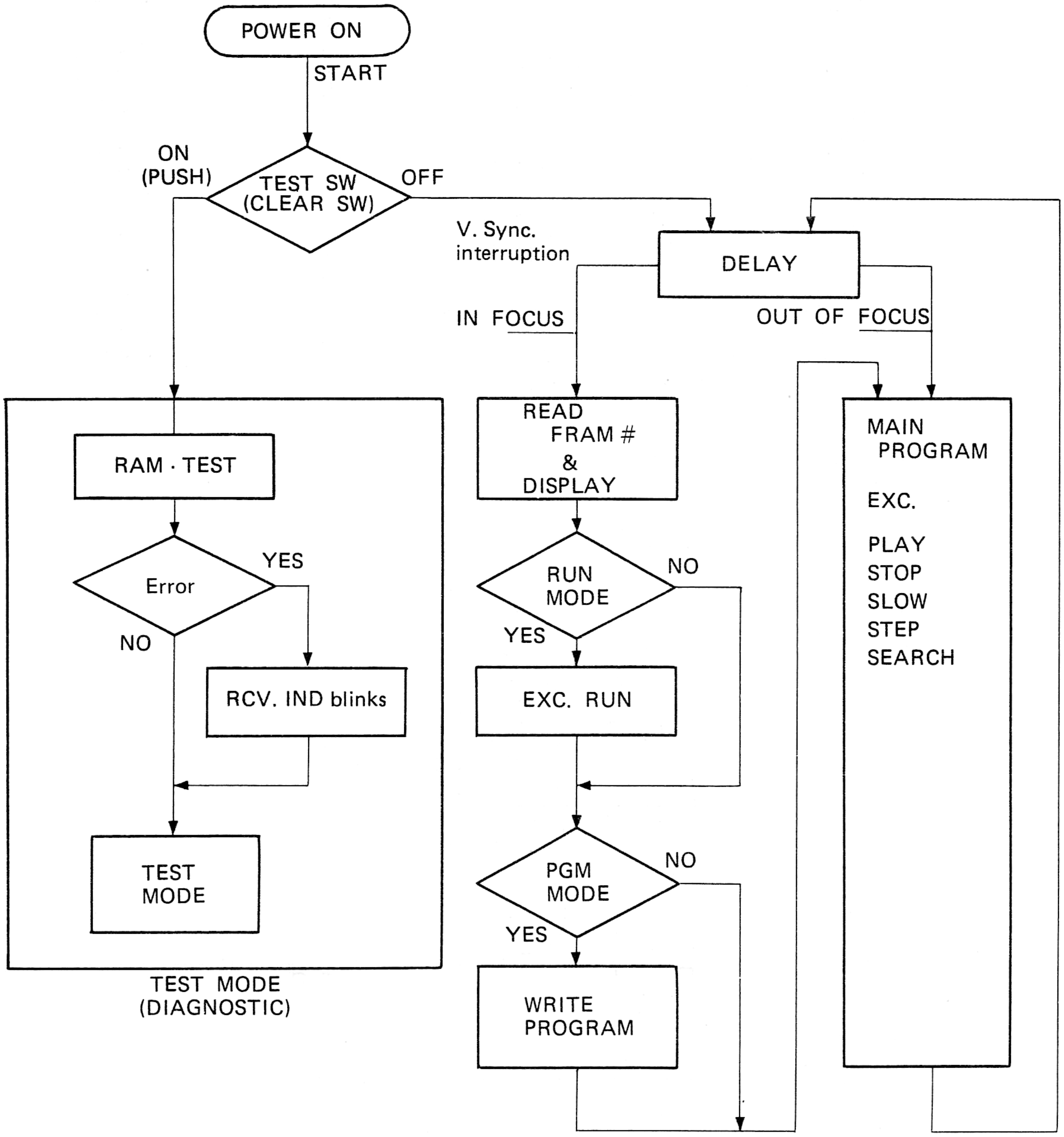
OTHER SIGNALS

SYS SQ : NOT SQ
VID SQ : NOT SQ
AUDIO SQ : SQ

✱ This lamp will blink on and off when a RAM error is detected.

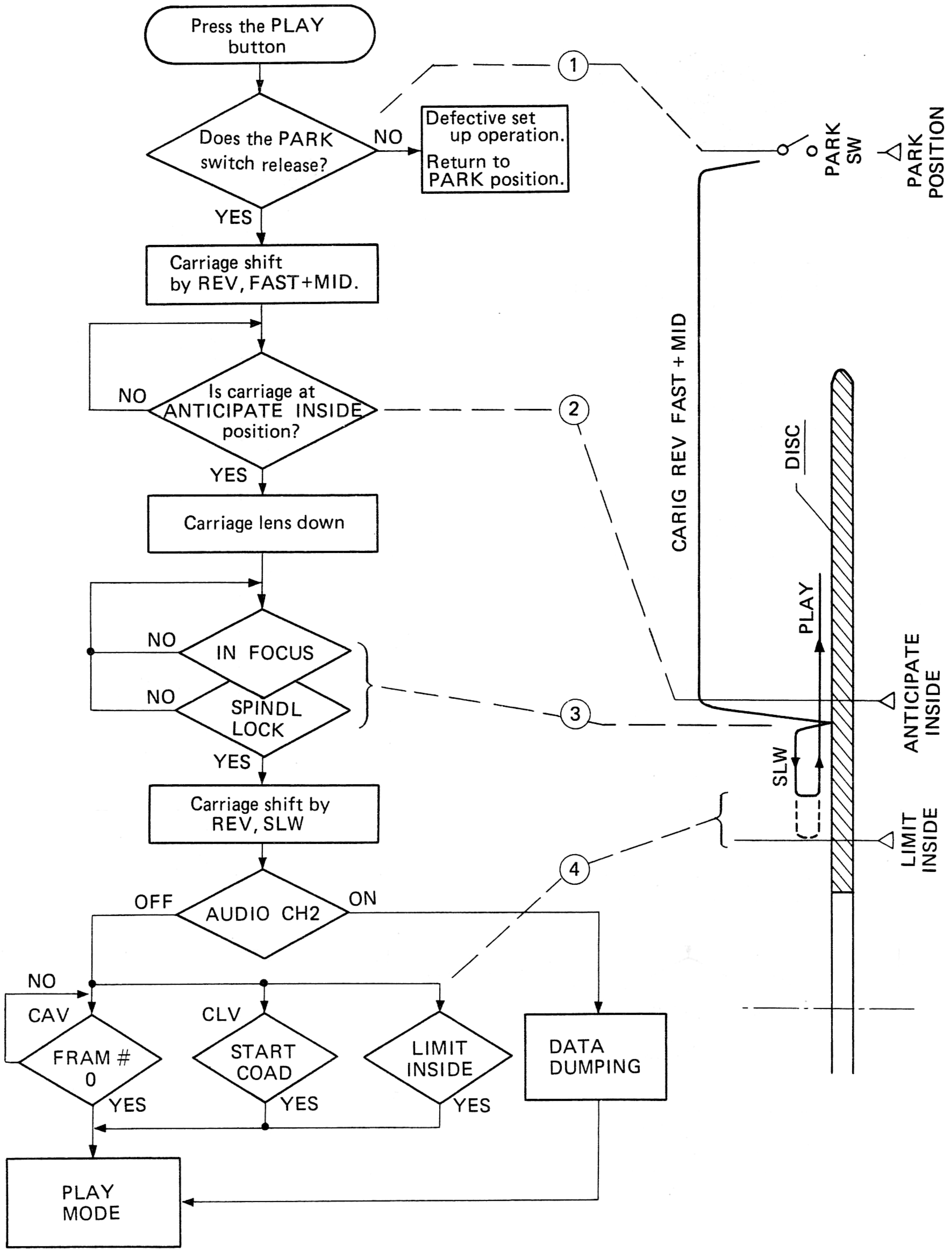
NOTE:
Test mode may be activated by turning the power switch on while pressing the RAM CLEAR switch (rear panel). In this case, the front panel push-buttons will switch to the operating modes indicated above.

a. Program A Main Program and Test Mode Operations

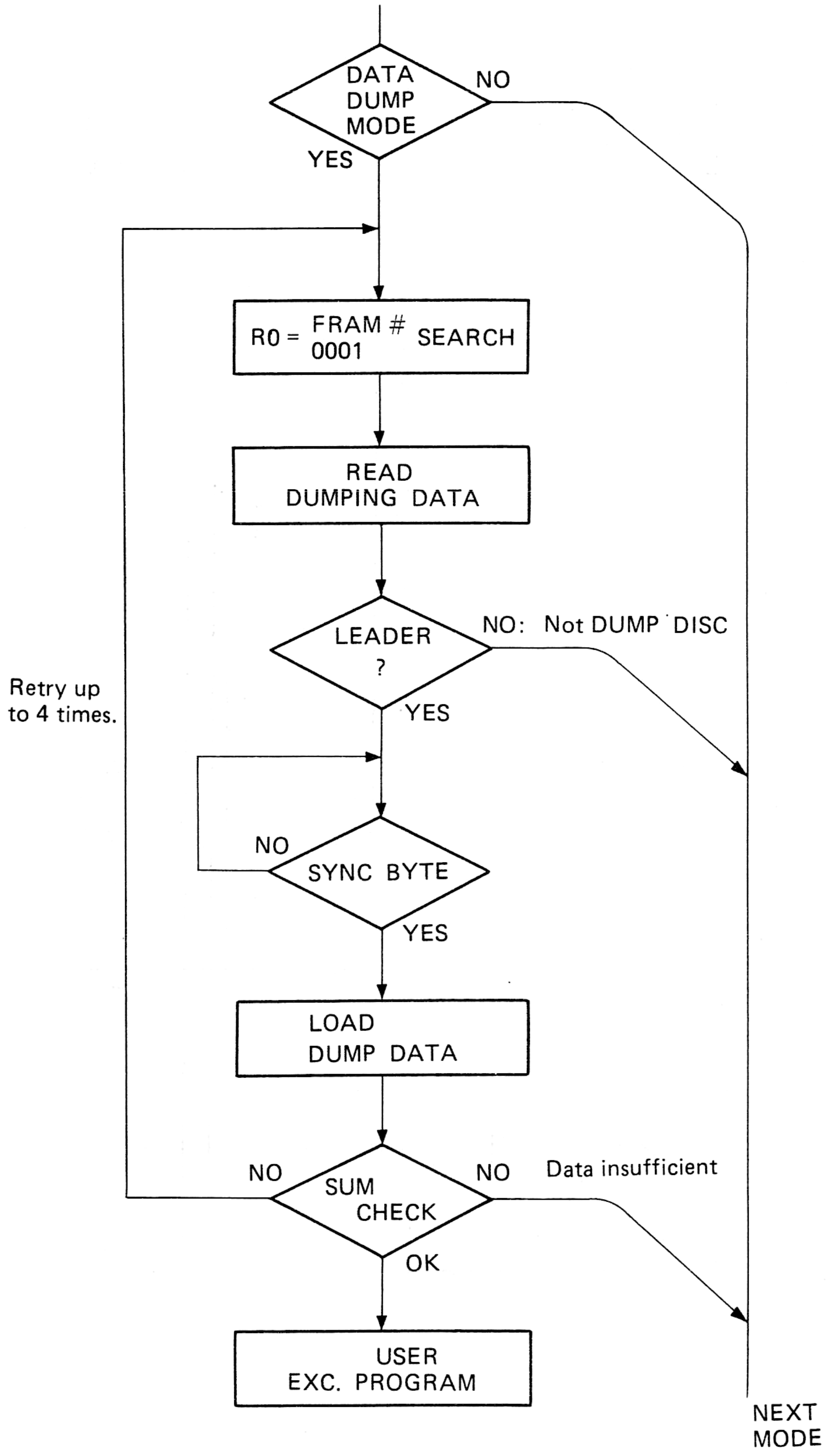


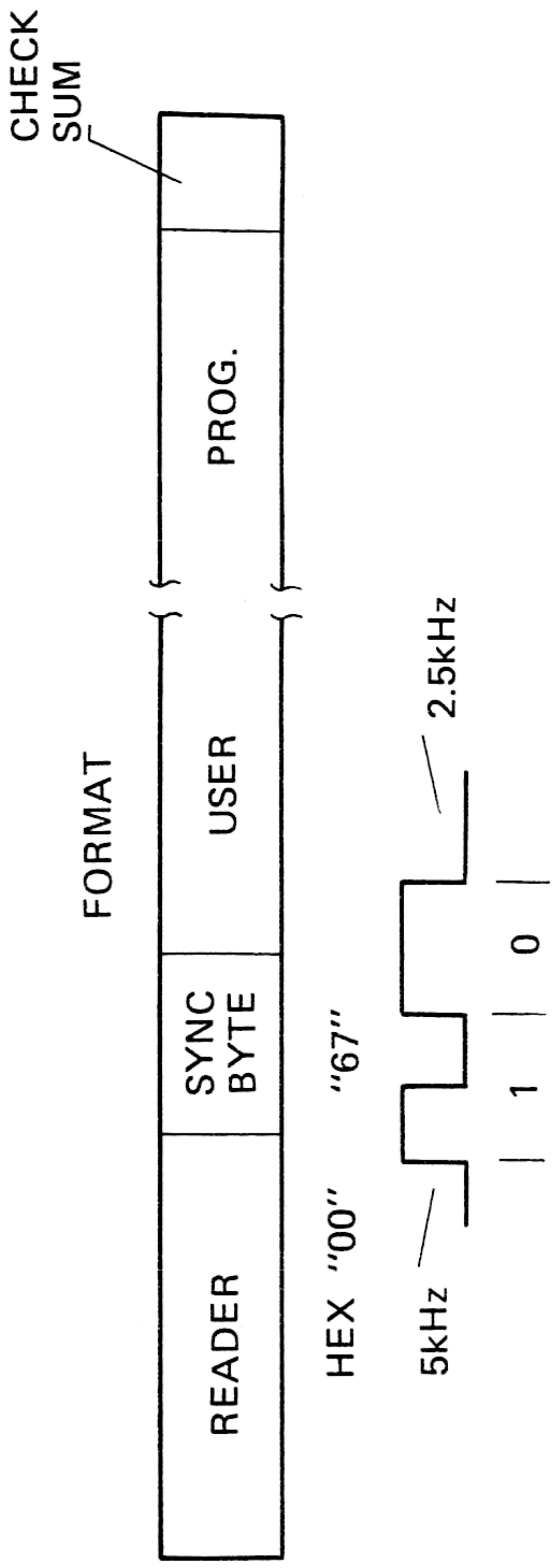
General overall program is organized in this manner.

b. Program B Set Up Operation

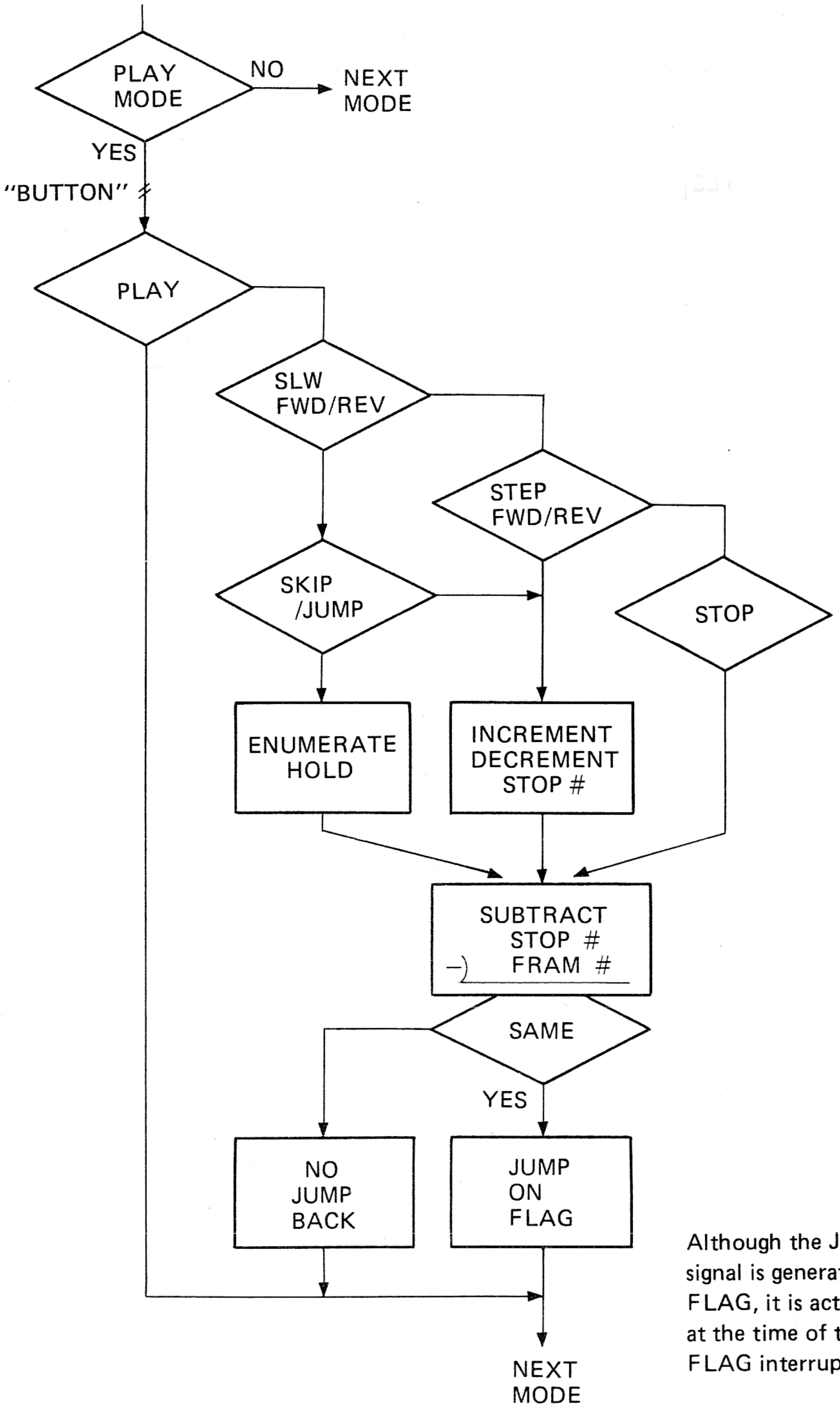


c. Program C Data Dumping Operation





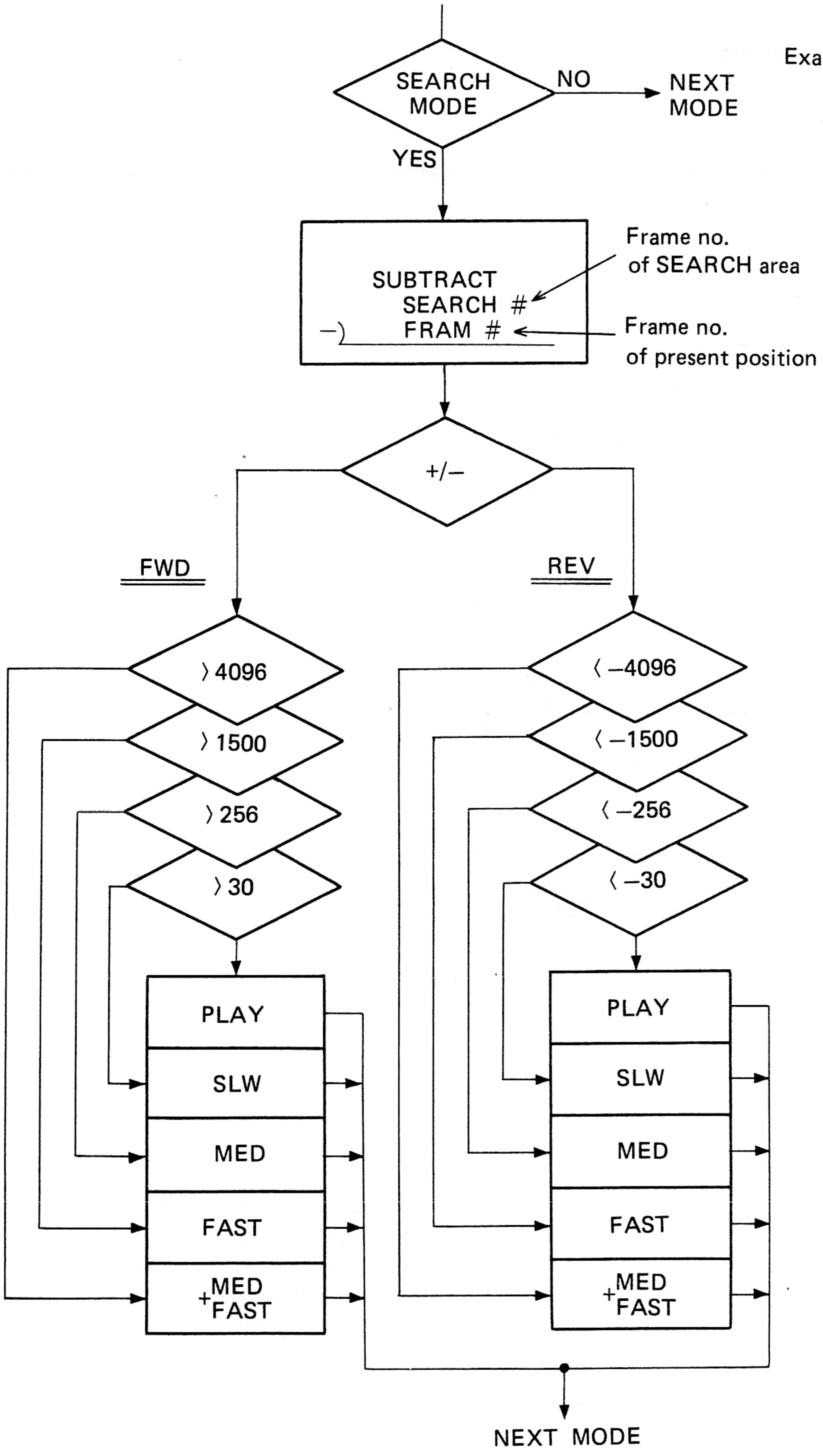
. Program D Play Mode Operation



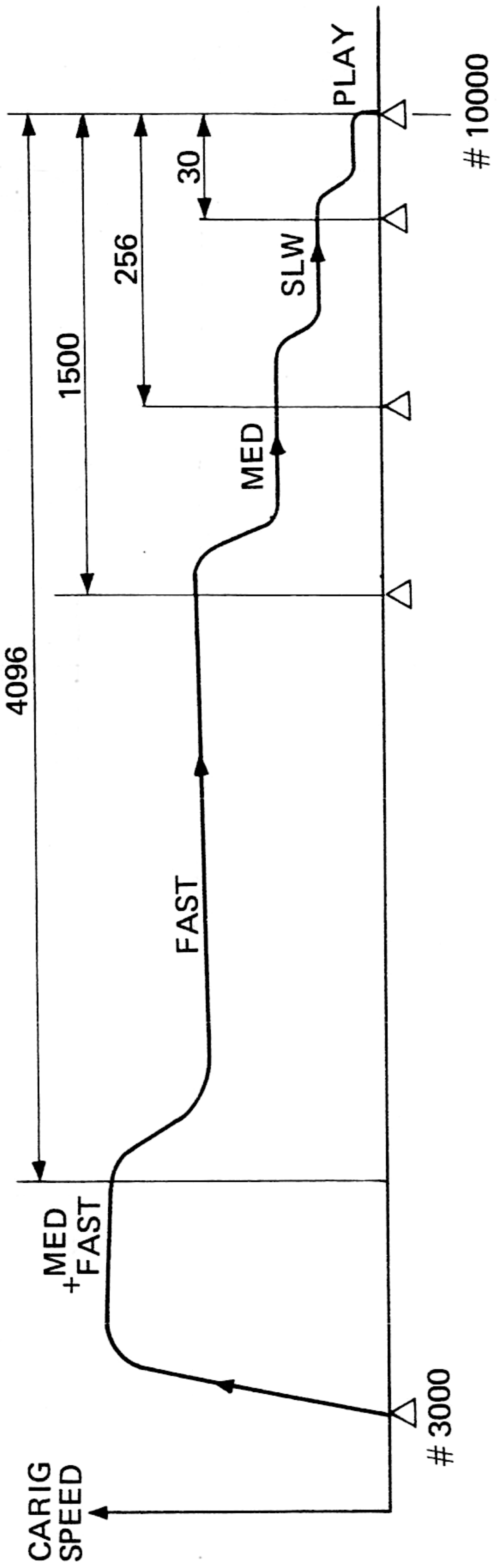
Although the JUMP BACK signal is generated by this FLAG, it is actually generated at the time of the WHITE FLAG interruption.

STOP #: Frame no. at which disc is to stop
FRAM #: Present frame no.

e. **Program E Search Operation**



Example: Sequence followed during search from present position # 3000 to # 5000.



PhiLLips CODE

MCA CODE -OLD

9.11 D & CR

- Outline

The D & CR circuit samples frame number and clock data from the video signal, converts the signal from serial to parallel which is TTL level, and feeds it to the microprocessor.

- Data signal format

As can be seen in Fig. 28, the frame number is inserted within V-blanking intervals. The data signal format is outlined in Fig. 29 (a) and (b). This 40-bit frequency modulated serial signal is first demodulated, converted into a parallel signal, and then transferred to the microprocessor. Detailed operation is described below with the use of the Fig. 30 block diagram.

9.11.1 Circuit composition

a. Clamp circuit

The DC level of the capacitor-coupled video signal is "clamped" to a particular value in order to simplify the operation of the following frame number sampling circuit.

b. Frame number sampling circuit

In order to extract the frame number code, the clamped video signal is converted to a TTL level signal by the voltage comparator, and at the same time, also applied to the time gate, thereby blocking any other unwanted signals. Both comparator and time gate are incorporated in the SN75107 IC.

VR1 is used to adjust the comparator slice level in order to cope with video signal variations, and must consequently be readjusted whenever the VDEM circuit board is exchanged due to change in the video signal level.

c. Data signal demodulator

The frequency modulated signal is demodulated into NRZ signal format.

d. Clock reproduction circuit

This circuit reproduces the clock signals which set the signal read-in timing for the NRZ signals.

e. Serial to parallel converter

Since the microprocessor input is a parallel input, this circuit employs a shift register to obtain parallel outputs from the NRZ and clock signals.

f. Data check circuit

If the bit pattern of the frame number code leading data and trailing data is correct, the frame number code is accepted as being valid, and the subsequent output signal become VALID DATA.

g. Output circuit

Since the microprocessor input can only accept single digit portions of data, the 5-digit frame number is divided into 5 parts (outlined in Fig. 27 below) before being transferred to the microprocessor.

h. $VR_1 \sim VR_4$

VR_1 has already been described above in section b. $VR_2 \sim VR_4$ are used to absorb variations in IC output levels, delay lines, and filters, and will not require further readjusting after the initial setting.

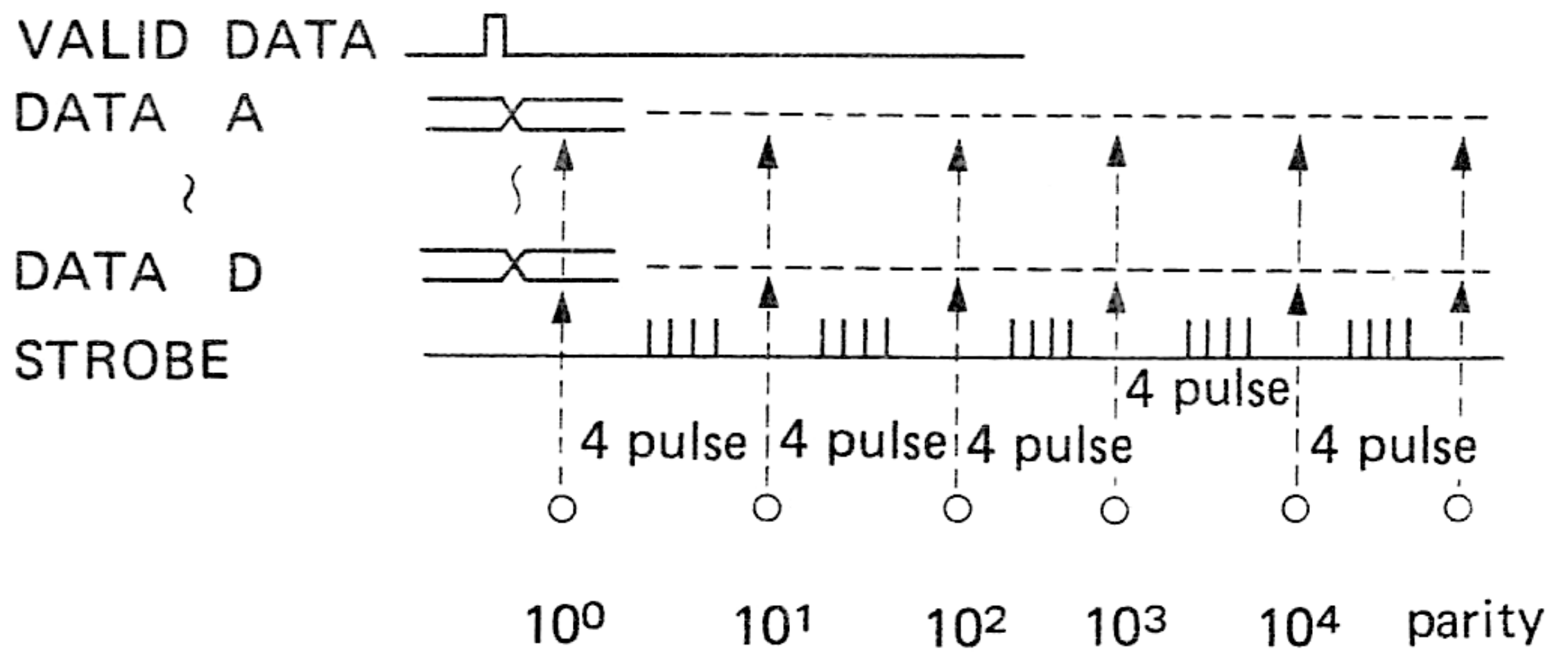


Fig. 27

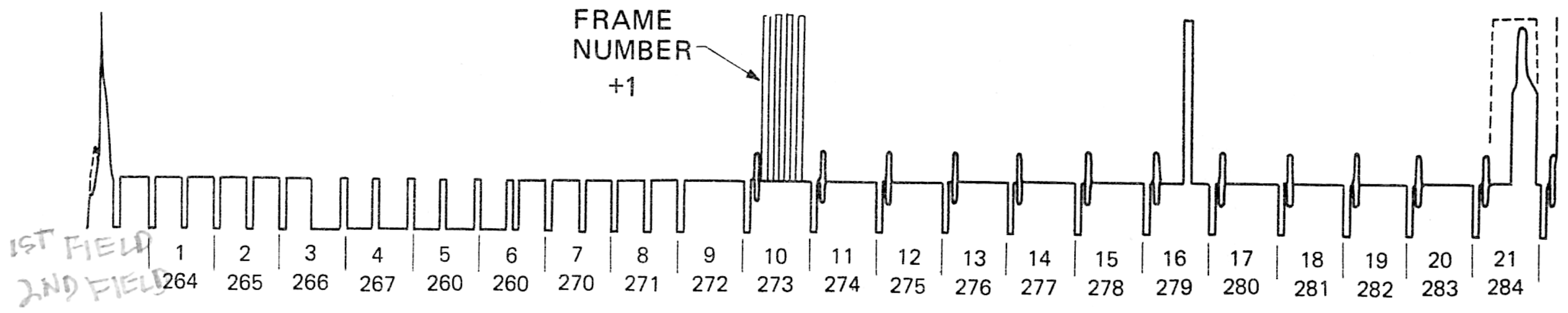


Fig. 28-a

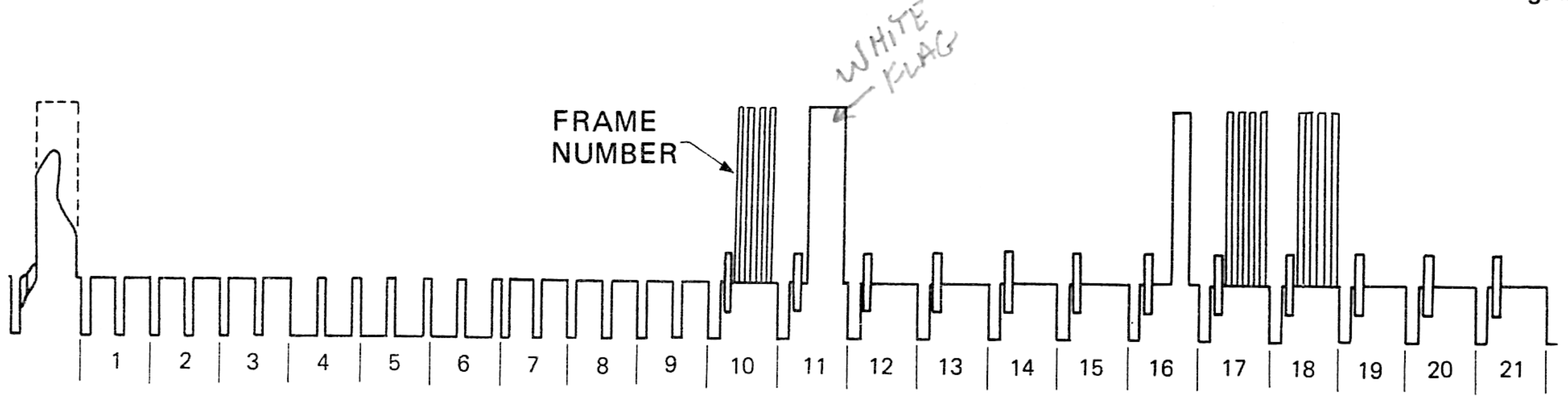
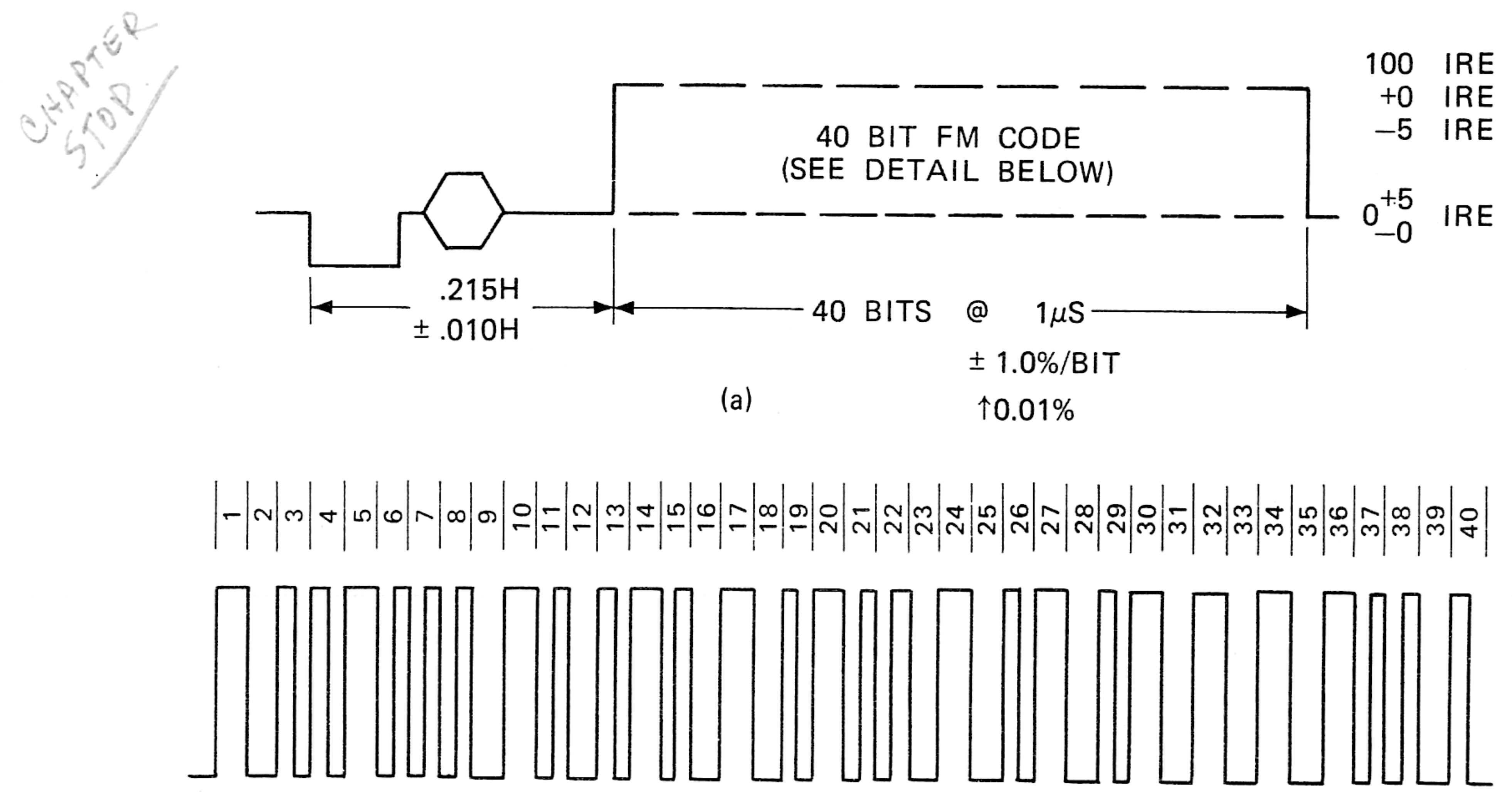


Fig. 28-b



(a)

40 BIT FM CODE
(VIDEO FIELD 2, FRAME #12,345 SHOWN)

(b)

Fig. 29

Transitions in center of bit cell represent logical "1"s.
Rise and Fall Times = 135ns ± 15ns. (10 – 90%)

Bit (s)	Remarks
1 – 4	Receiver clock synchronizing bits – "0011"
5	Video field indicator bit (Logic "1" = Video field one)
6 – 12	Leading, data recognition bits – "1110010"
13 – 16	Data – X5 – Bit 13 = LSB
17 – 20	Data – X4 – Bit 17 = LSB
21 – 24	Data – X3 – Bit 21 = LSB
25 – 28	Data – X2 – Bit 25 = LSB
29 – 32	Data – X1 – Bit 29 = LSB
33	Data Parity Bit (Odd Parity)
34 – 40	Trailing, data recognition bits – "0001101"

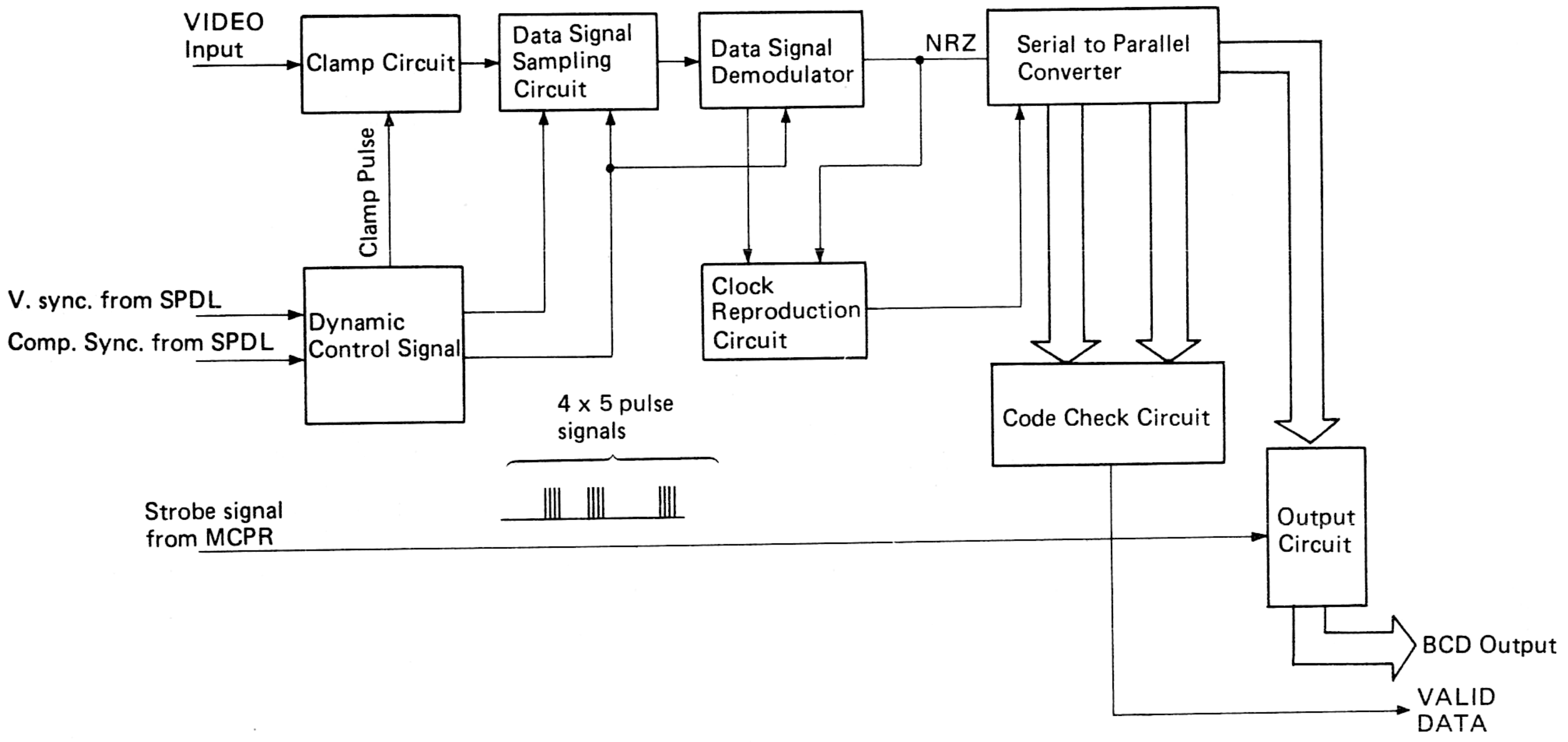


Fig. 30

9.12 STPM

a. VIDEO AMP, VIDEO CLAMP

This circuit amplifies the playback video signal, and by clamping, removes the DC fluctuation in the video signal. In this way, a constant sync. chip level is obtained.

b. COMP SYNC SEPARATION

This circuit separates the composite sync from the playback video signal, and subsequently applies the video signal to the comparator where a constant DC level signal is added to the reverse phase input for "slice comparison" at that level.

c. VERT SYNC SEPARATION

With a circuit composition the same as the above composite sync separation circuit, this circuit integrates the composite sync received from the above circuit in order to extract the vertical sync component.

d. WHITE FLAG SEPARATION

This circuit extracts the white flag signal inserted in the vertical interval blanking zone in the playback video signal. This white flag signal is used in stop, slow motion, and step playback modes.

e. GATE PULSE GEN.

Pulse signals of requisite pulse widths (obtained via time constant circuit) are prepared from the vertical sync in order to synchronize the white flag insertion zone with the gate.

f. SKIP/JUMP PULSE GEN.

This circuits generates pulse signals with a pulse width controlled by the DC voltage generated by the slow motion speed control on the front panel. The pulse train is transferred to the microprocessor where the signal duty cycle is determined for setting the playback speed.

The STPM circuit (VWG-004) may be divided into 2 major stages — the synchronizing signal separation circuit, and the slow motion speed control circuit. The former employs a comparator in order to separate the white flag signal and the composite and vertical sync from the playback video signal picked up from the video disc. The basic operation of this circuit involves applying the video signal to the inverse phase input of the comparator, and subsequently separating the desired signal by slice comparison at a prescribed DC level.

The latter stage, on the other hand, applies DC voltage data (from the front panel slide potentiometer) to the timer IC where it is converted to a pulse train with a duty cycle corresponding to the voltage level. The microprocessor then measures the pulse train duty cycle and subsequently sets the slow motion speed.

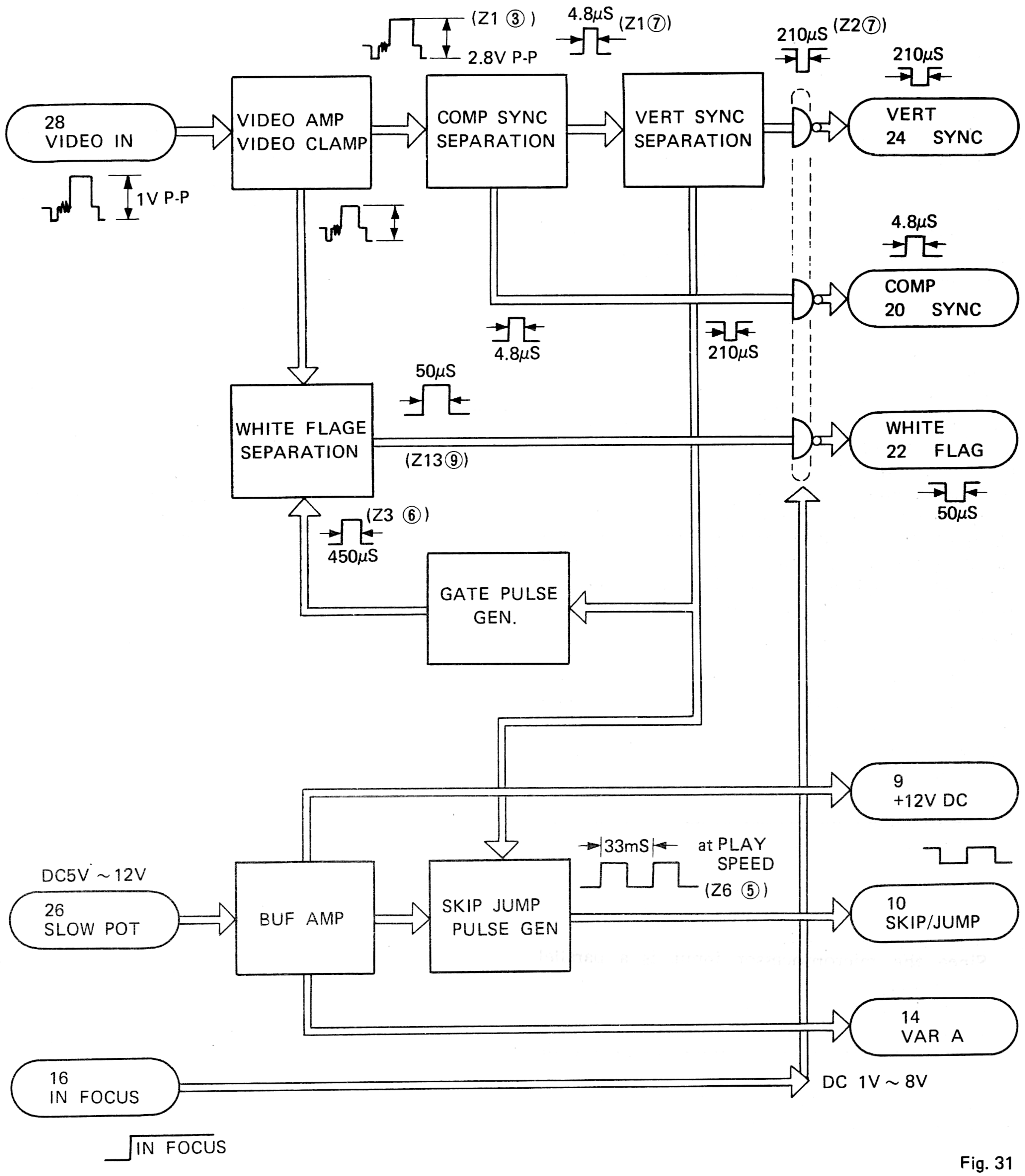


Fig. 31

NOTE:

The white flag signal and the composite and vertical sync are enabled only after the "in focus" status has been attained.

VWG-004 STPM Block Diagram

- Input and output signals without level designations are TTL level signals.

9.13 LMP 1, 2, 3

$LMP_1 \sim _3$ Description

The LMP_1, LMP_2 and LMP_3 circuit boards located inside of the front panel serve as function selector switch and mode indicator lamps.

As the bellow diagram shows, the LEDs are anode common connected, and will light up the LMPD LED driver terminal is switched to "L" level.

These switches are located in the X-Y matrix, the function selector operation being completed by short circuiting the LMPD encoder X_i-Y_j.

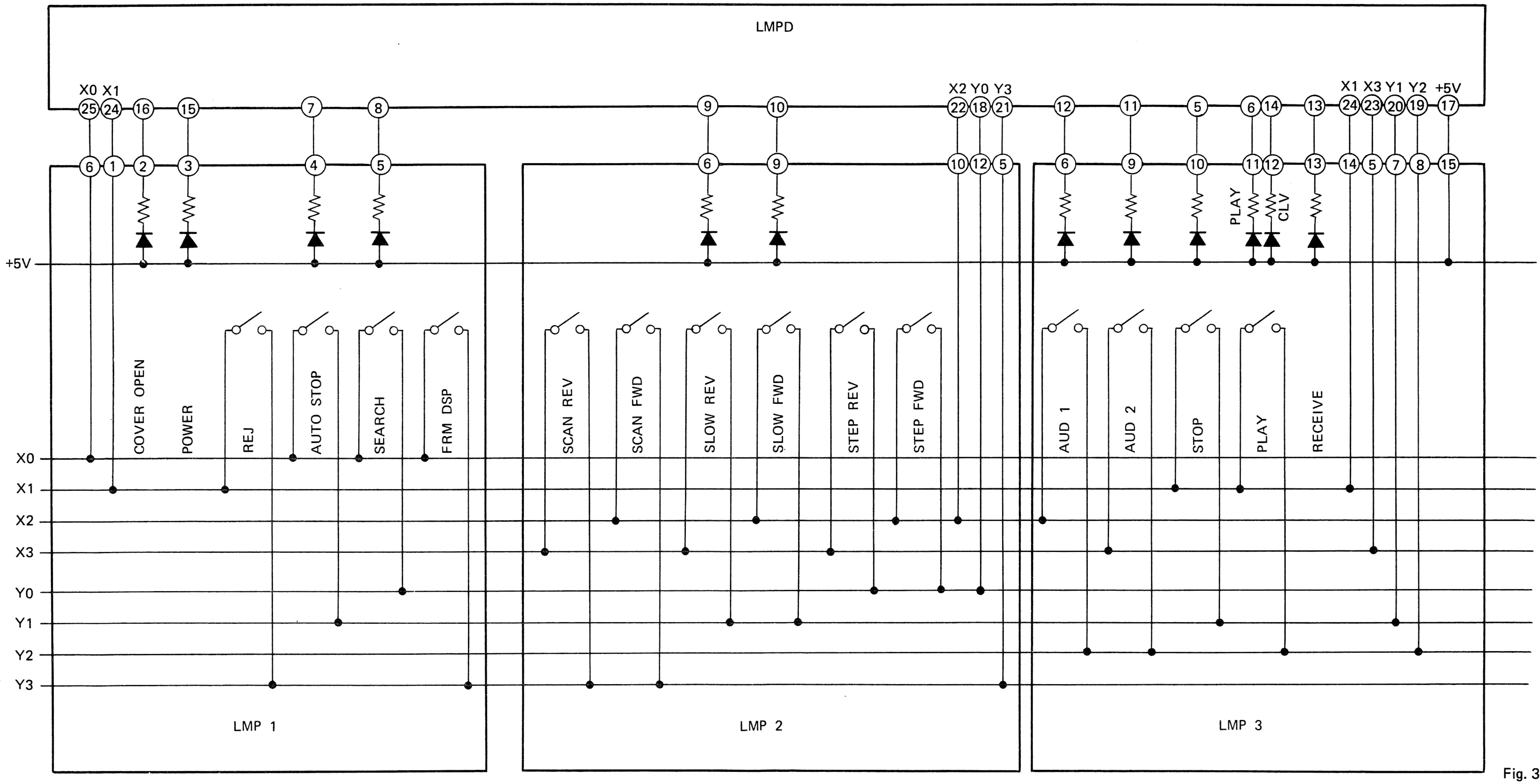


Fig. 32

9.14 RU-8 REMOTE CONTROL UNIT

Function

Transfer of 30 different commands to the disc player unit by means of the wireless (or wired) remote control unit.

Composition

a. Keyboard (see Fig. 33)

Consists of 30 push-button keys (1 line per contact switch) in a matrix format which is connected to the code pulse generator by 12 leads).

b. Code Pulse Generator

Generates different serial signals according to the inputs received via 12 input leads. The generator employed here generates a 200kHz signal only when a push-button key is pressed, and this may be checked via pin No.7 of Z_1.

c. LED Driver

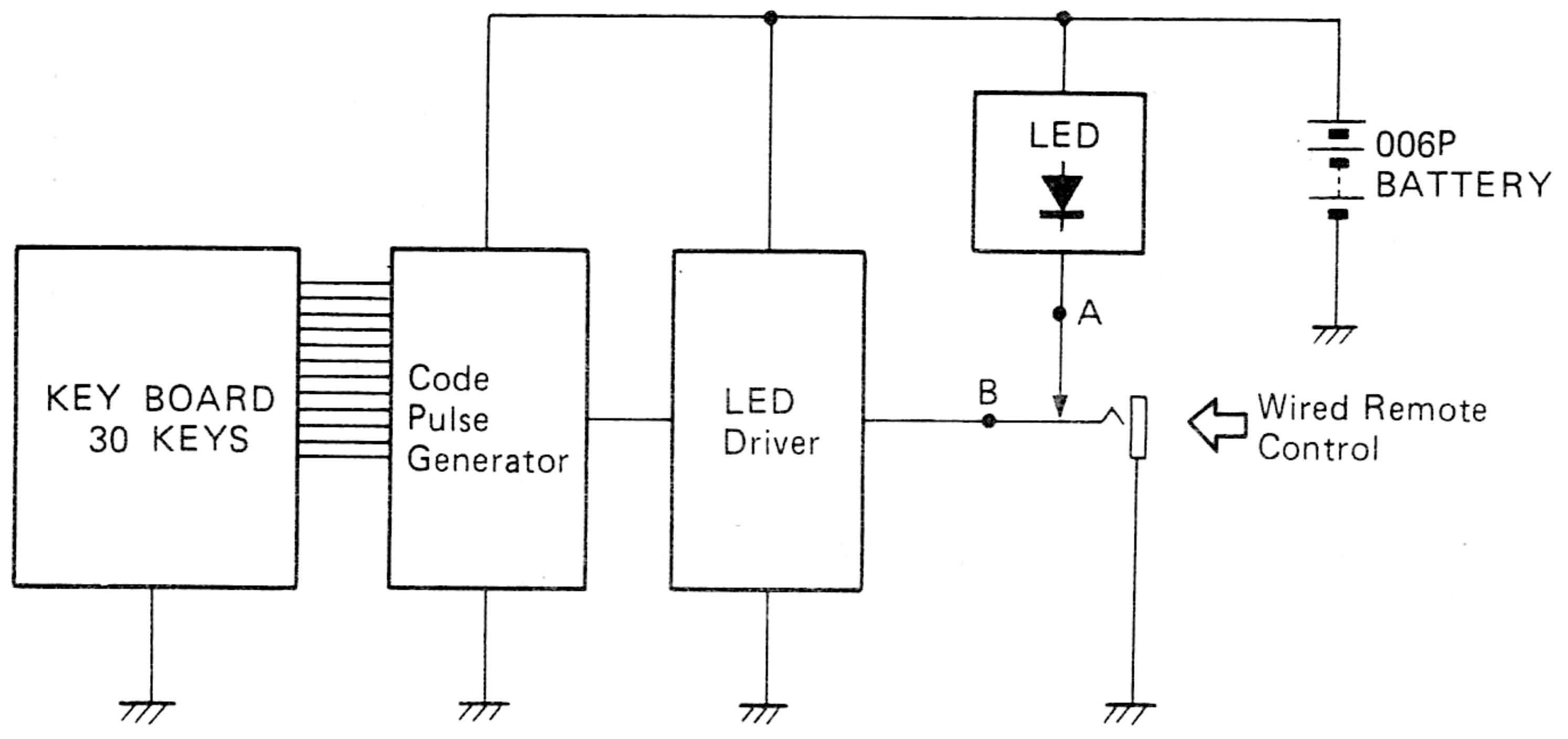
This Darlington connection transistor driver circuit applies a peak current of 2.5A to the LED, but since the wave length of the LED emission is 9400A° (infra red) the emission is not visible to the human eye.

d. Wired Remote Control

When the remote control unit is connected to the disc player unit by cable, the LED is disconnected from the driver stage. And since the power supply for the driver is received from the player unit via the cable, battery consumption may be economized.

e. Serial Signal

The serial signal outlined in the above diagram is generated at pin No.5 of Z_1. By various combinations of $D_0 \sim D_4$, a maximum of 32 different data signals may be generated.



	Wireless Remote Control	Wired Remote Control
A - B switch	ON	OFF

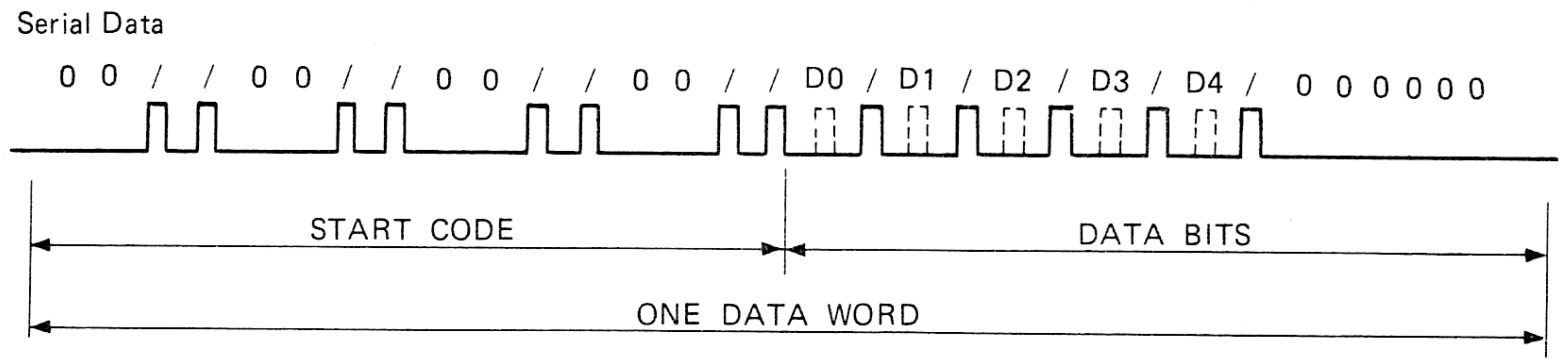

Serial Data
0 0 / / 0 0 / / 0 0 / / 0 0 / / D0 / D1 / D2 / D3 / D4 / 0 0 0 0 0 0
START CODE
DATA BITS
ONE DATA WORD

Fig. 33

9.15 MIRB

Mounted in the front panel of the disc player unit, the MIRB circuit receives infra-red control signals from the remote control unit (max. distance of 7 meters), and converts them into electrical signals to be transferred to the LMPD circuit.

The infra-red signals are picked up by the photo-sensitive diode D_1 (covered with an infra-red filter), and passed on to amplifier and switching stages before appearing at pin No.2 output terminal.

The power supply is a 9V power supply regulated in the LMPD circuit.

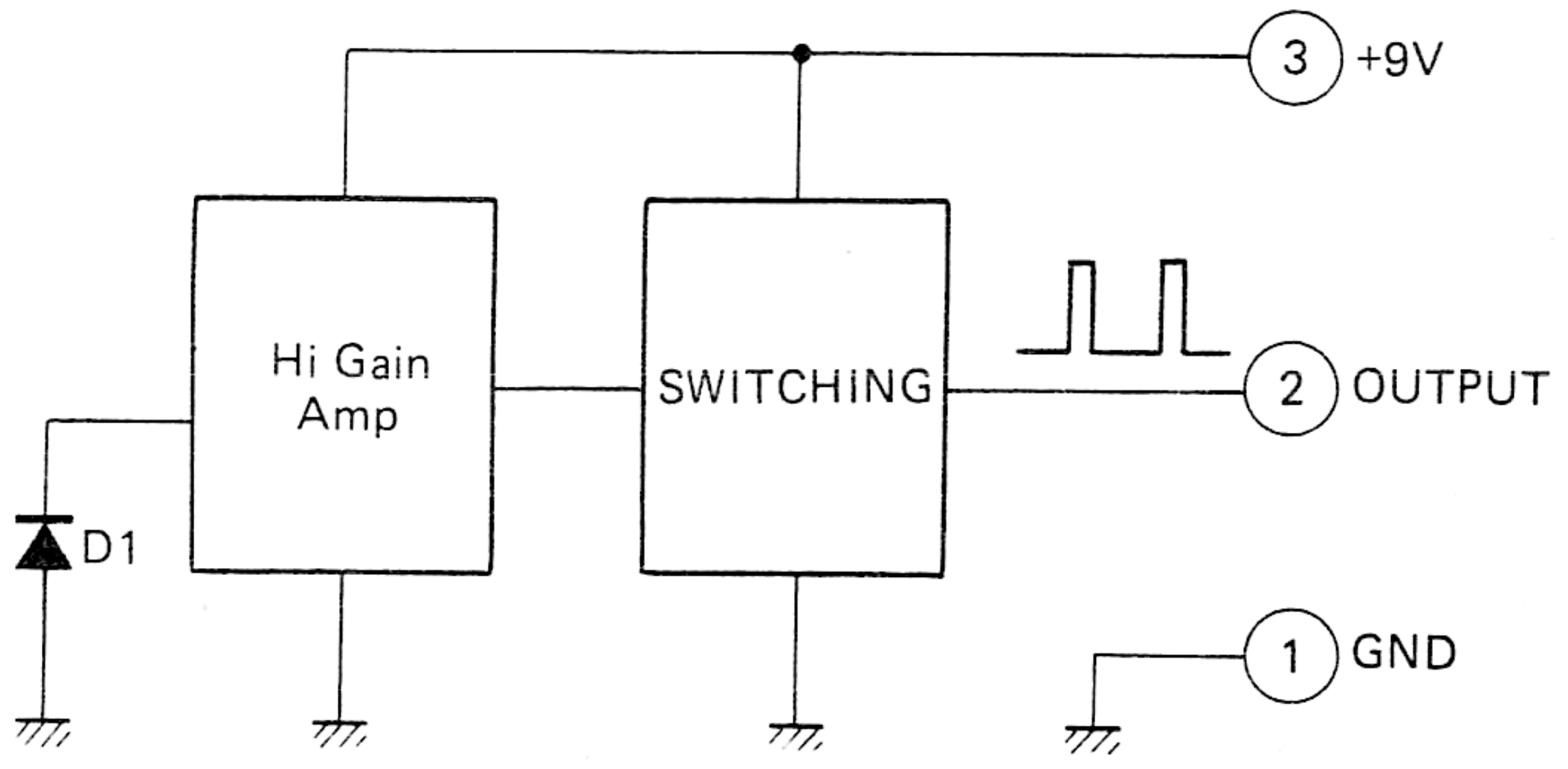


Fig. 34

9.16 SIRB

Infra-red signals received from the remote control unit mounted in the top of the player unit are converted into electrical signals which are passed on to the LMPD circuit.

Infra-red signals beamed via an acrylic resin reflector built into the top cover of the player unit are picked up by the photo-sensitive diode D_1, and then passed via amplifier and switching stages to pin No.3 output terminal.

The power supply again is the 9V supply regulated in the LMPD circuit.

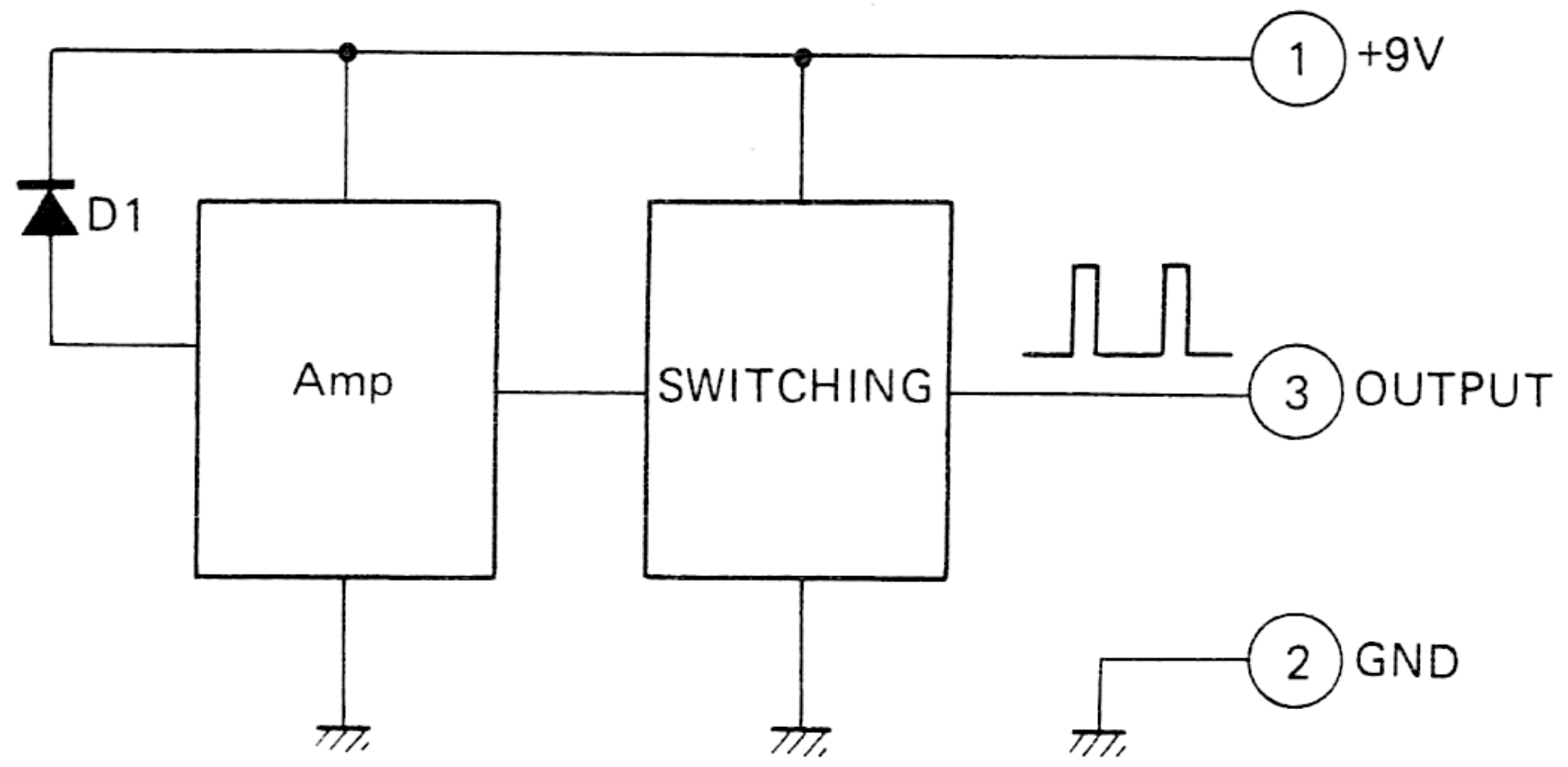


Fig. 35

9.17 SYPS

1. 15V Regulated Constant Voltage Circuit

As can be seen from the block diagram, this circuit is employed to provide a variety of different power supply voltages. The fundamental voltage is the ±15V (pin Nos.18 and 22) prepared by the voltage regulator ICs. An over load protector circuit is also incorporated within these ICs.

2. 5V Regulated Constant Voltage Circuit

The constant voltage on each of the 3 terminals is prepared by independent transistors. The 6.3V ±2% fundamental voltage is prepared by a zener diode.

3. SPDL Drive Power Supply and SPDL Motor Drive Circuit

Because of the considerable amount of current required to drive the SPDL motor, the power is supplied from a separate transformer winding. The SPDL drive circuit amplifies the current of the drive signal from the SPDL assembly. Furthermore, since this is a SEPP circuit, the (+) side transistor is equipped with a separate heat sink (mounted externally) to dissipate the extra heat generated. And in order to compensate for the power transistor V_{BE} loss (V_{BE} of 1.2V due to the Darlington connection), a PNP transistor and 2 diodes are employed to shift the drive signal DC level in the positive direction.

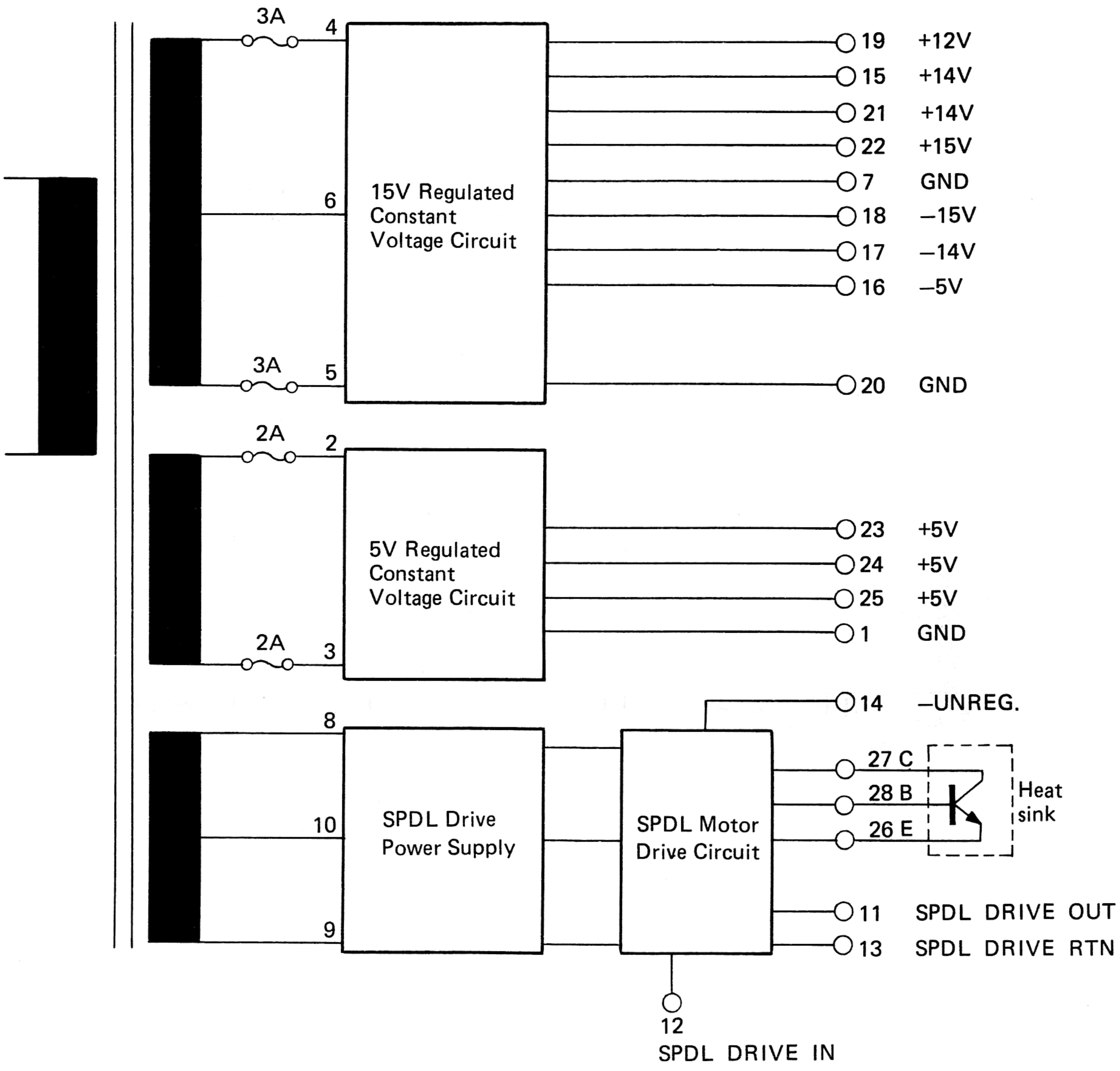


Fig. 36 SYPS (SYSTEM POWER SUPPLY) CIRCUIT DIAGRAM

9.18 LSPS

Outline of Operation

The LSPS and CUST circuits are used to activate the laser tube. The LSPS first applies AC 800V to the voltage doubler rectifier, and then on to the H.V. Block where the voltage is multiplied by 9 and the signal further rectified to provide a starter voltage high enough to light up the laser tube. Once the laser tube begins to oscillate, the impedance of tube drops and the DC current starts to flow through the high voltage block and laser tube. From then on, the high voltage block stops multiplying its input. The CUST is also then employed to maintain a constant flow of current through the laser tube.

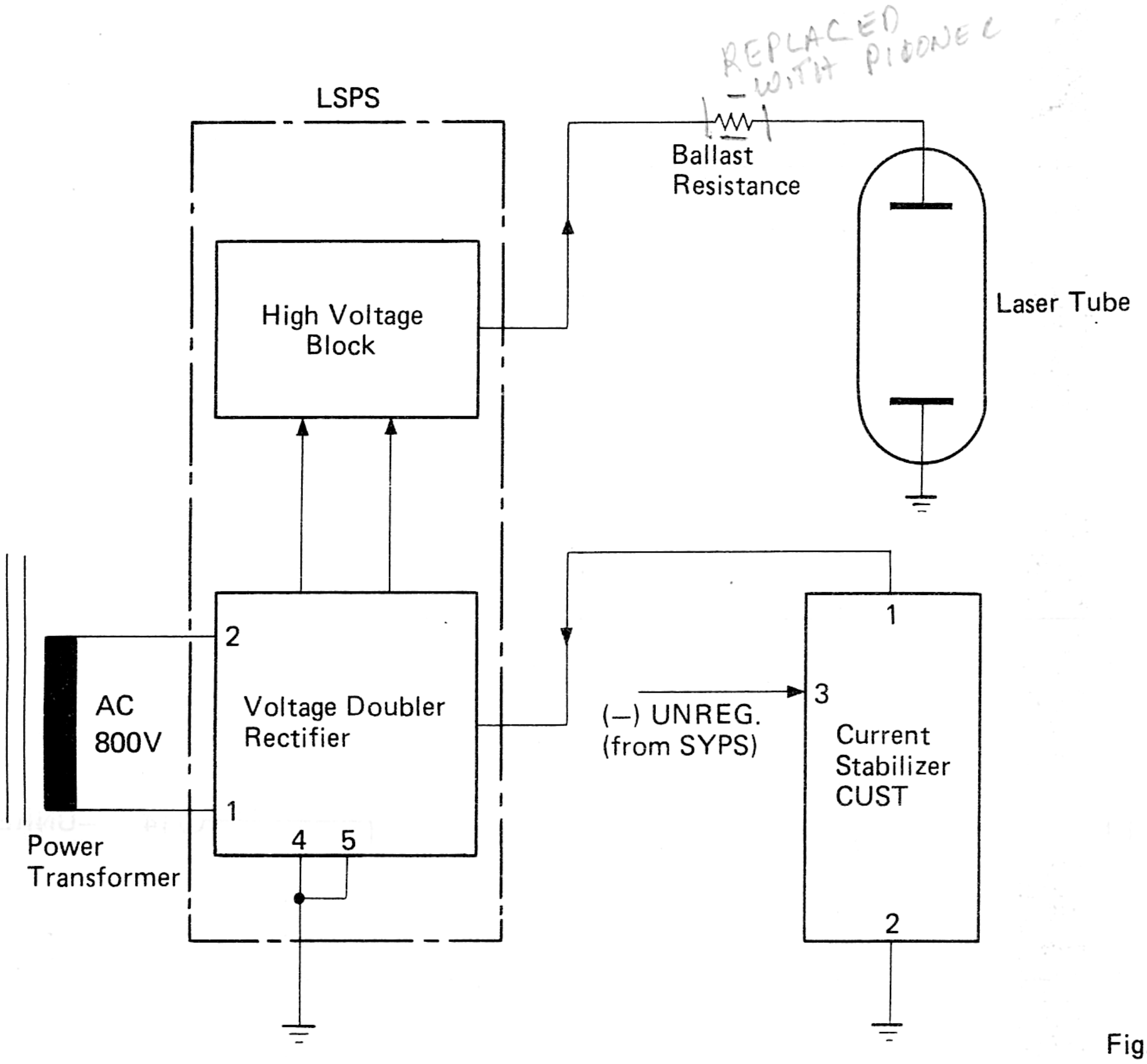


Fig. 37

9.19 RF MODULATOR

The synchronizing signal portion of the video signal applied to the VIDEO IN terminal is clamped by the clamper before being applied to the video modulator.

The video carrier signal is generated by the X_1 or X_2 quartz oscillator circuit, multiplied by the frequency multiplier, and then applied to the video modulator and mixer stages.

The video signal modulated by the video modulator is passed to the RF OUT via high-pass and low-pass filters.

The audio signal applied to the AUDIO IN terminal is first passed through a 75μsec. pre-emphasis preamplifier stage.

The audio signal is then modulated into an FM signal by the 4.5MHz oscillator before being passed onto the mixer.

This 4.5MHz signal is mixed with the video carrier signal from the frequency multiplier, and passed to the RF OUT terminal as the audio carrier.

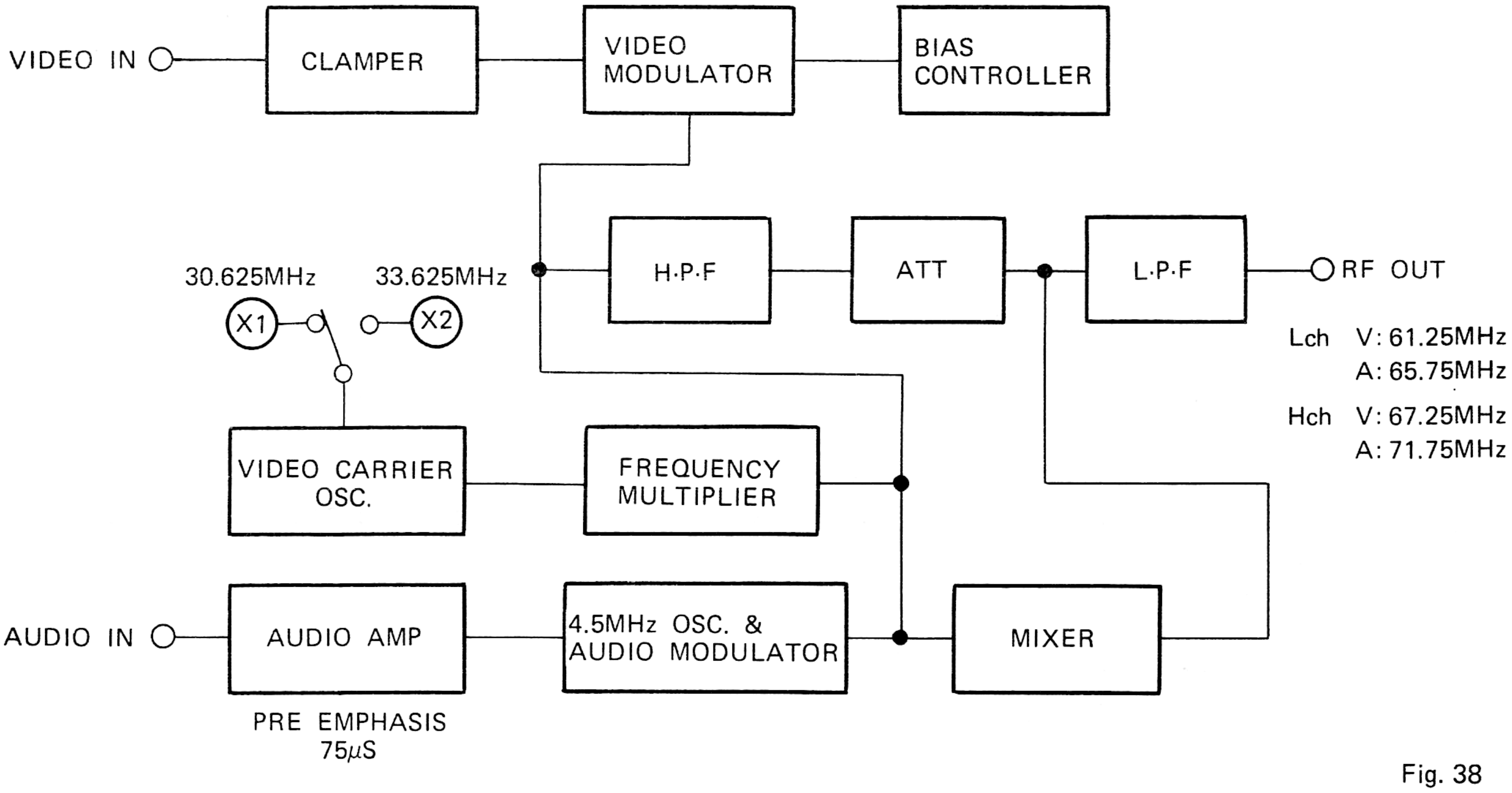


Fig. 38

9.20 LMPD

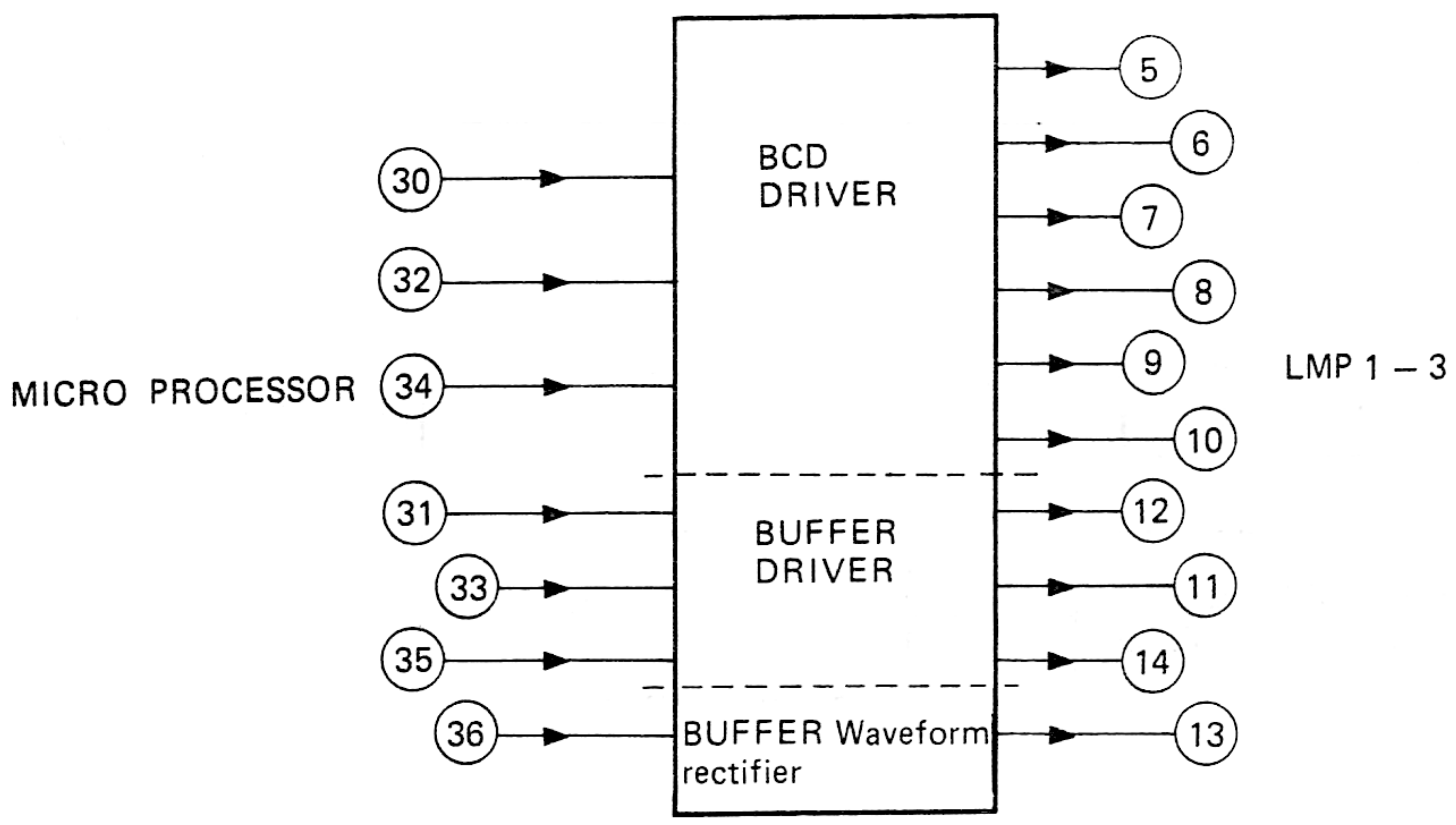
This circuit consists of an Indicator Driver stage for the indicator LEDs above $LMP_1 \sim _3$, and a Function Selector Code (serial data) Transfer stage for transfer of data to the decoder in the DSPL circuit.

The Indicator Driver decodes input signal applied from the MCPR circuit, thereby obtaining output signals (to be applied to $LMP_1 \sim _3$) in accordance to the accompanying chart. A +5V power supply for $LMP_1 \sim _3$ is obtained from pin No.17.

In the Selector Code Transfer stage (outlined in the accompanying diagram), the CODE SELECT priority is determined by NAND gates A and B.

1. When one of the push-button SW (corresponding to $LMP_1 \sim _3$) on the front panel is pressed, one of the (18)~(21) terminals and one of the (22)~(25) terminals will be short circuited (depending on the selected mode), resulting in a serial data output appearing on pin No.37. The oscillating frequency at this time will be set to 200kHz, and will appear at pin No.7 of Z_3. Together with the data output, the Code Pulse Generator also issues an "L" level output at C. Resulting in the separation of all stages behind the dotted line (1).
2. During wired remote control mode when the remote control unit is connected by cable, the wire SW (44) is switched to "L" level mechanically. Since this disconnects the stage behind dotted line (2), infrared (wireless) remote control signals will not be accepted during this mode.
3. Wireless remote control outputs from MIRB and SIRB are rectified before appearing at the output terminal (pin No.37).
   The +9V power supply for MIRB and SIRB is obtained from pin No.29.
   In addition, 3 relay terminals are also made available, pin Nos.2 and 3 for SLOW VR, and pin No.16 for the cover open indicator.

INDICATOR DRIVER PART



IN			OUT					
34	30	32	5	6	7	8	9	10
L	L	L	H	H	H	H	H	L
L	L	H	H	H	H	H	L	H
L	H	L	H	H	H	L	H	H
L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H
H	L	H	L	H	H	H	H	H
H	H	L	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H

31	12
L	L
H	H

33	11
L	L
H	H

35	14
L	H
H	L

36	13
L	H
H	L

Fig. 39

o FUNCTION SELECT CODE TRANSFER PART

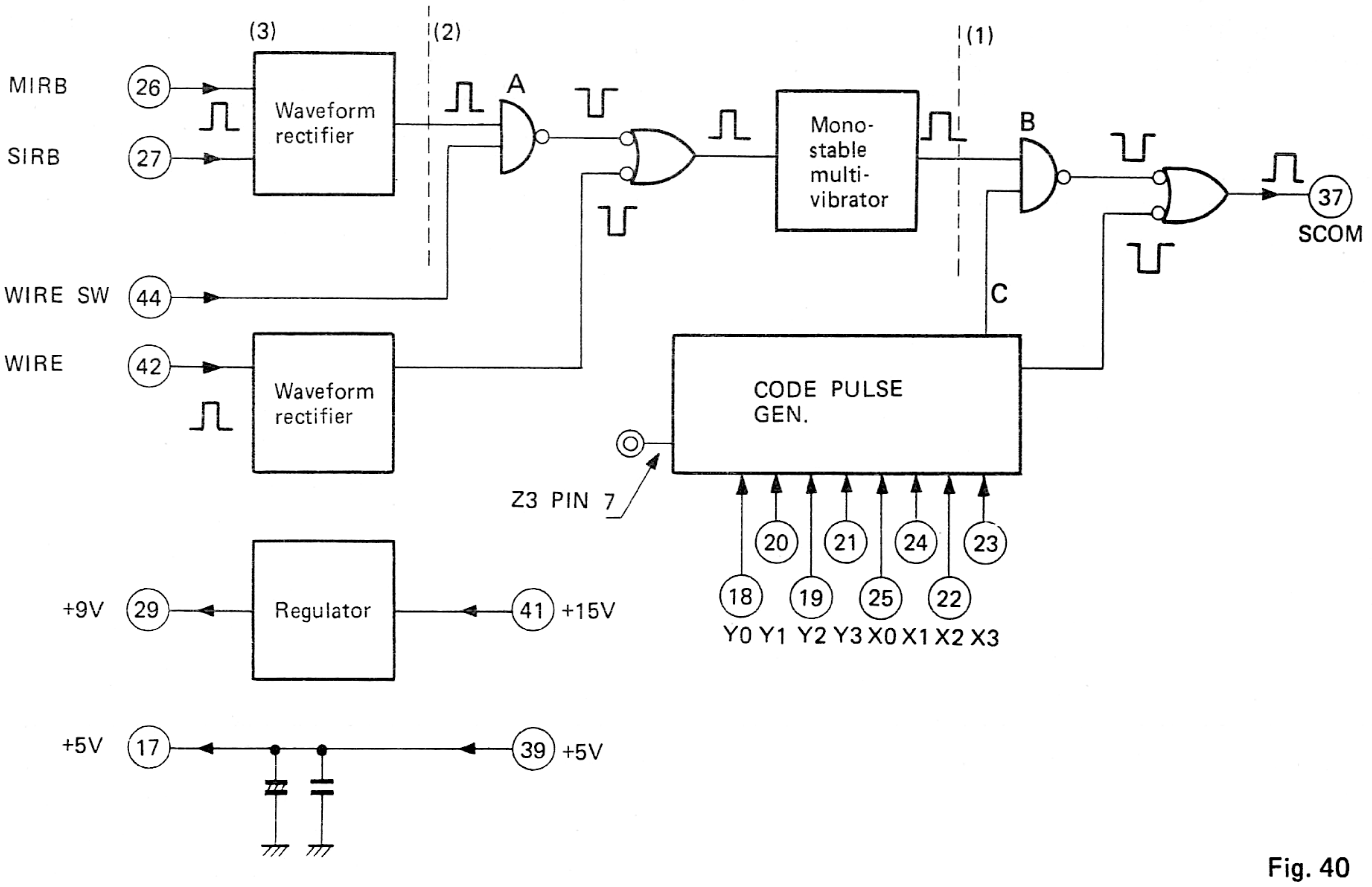


Fig. 40

9.21 PHDB

This photo detector features photo-sensitive diodes in 3 multi-element stages (A, B and C), and is used to detect FM signals and servo control signals. Stage B consists of photo-sensitive diodes in 4 parts.

The zero order laser beam reflected back from the surface of the video disc is directed into stage B, while the first order laser beams are directed into stages A and C. In stage B, the playback FM signal is obtained by matching focus control signals from the 2 pairs of opposing photo-sensitive diodes. Tracking control signals are obtained from the photo-sensitive diodes in stages A and C. All of these signals are then applied to the head amplifier.

9.22 FFMP

The FFMP (Fuse & Focus Motor Protector) circuit consists of 3 major parts:— (1) the power transformer secondary coil fuse, (2) the focus motor protector circuit which prevents the focus lens from dropping if the power supply is cut during VDP operation as a result of a mishap (such as a power failure), and (3) a power input line filter.

a. Fuse Stage

Four fuses (2A rating for the 5V line and 3A rating for the 15V line) are inserted between the secondary winding of the power transformer and the SYPS circuit.

b. Focus Motor Protector Stage

This circuit is designed to protect the focus lens, and the video disc, if the power supply line should be cut accidently during VDP operation. While the power is on, the AC output from pin No.8 is rectified in order to activate the relay, thereby ensuring that the focus drive signal is applied to the focus motor. However, if the power supply is inadvertently cut, the relay will be switched to position 2, and a DC voltage will be applied to the focus motor via the focus motor pull up circuit activated by the voltage applied by the battery. The focus lens will thus be raised. This DC voltage is applied for about 60 seconds in which time the video disc will have stopped rotating. Both and the lens and disc are thereby protected against possible damage.

c. Line Filter Stage

The AC power supplied via the power connector is applied to pin Nos.16 and 17, through the primary coil fuse (F_1 3A) and line filter, and on to the primary coil transformer. Besides removing external noise, the line filter also prevents leakage of VDP noise back to the power supply. Pin No.15 is connected to the ANT terminal in order to ensure against possible danger from lightning.

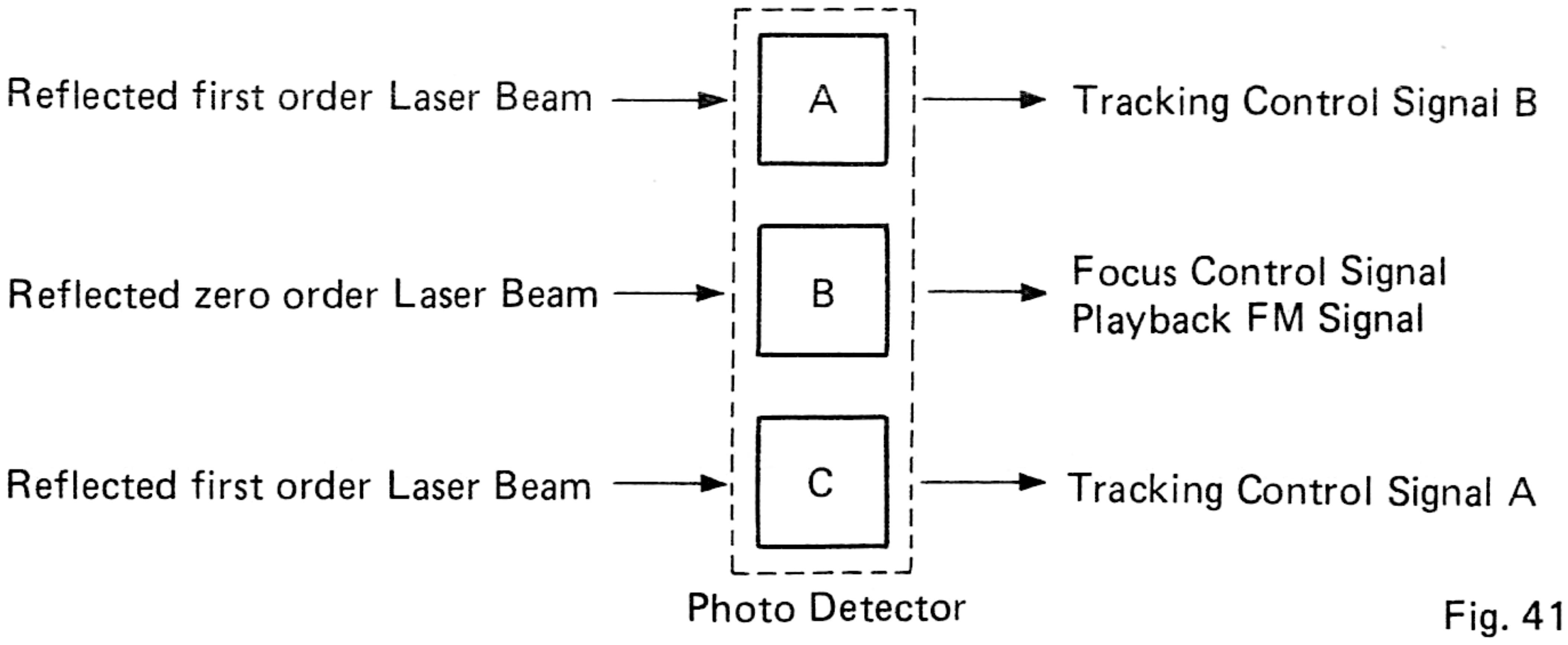

Reflected first order Laser Beam
A
Tracking Control Signal B
Reflected zero order Laser Beam
B
Focus Control Signal
Playback FM Signal
Reflected first order Laser Beam
C
Tracking Control Signal A
Photo Detector

Fig. 41

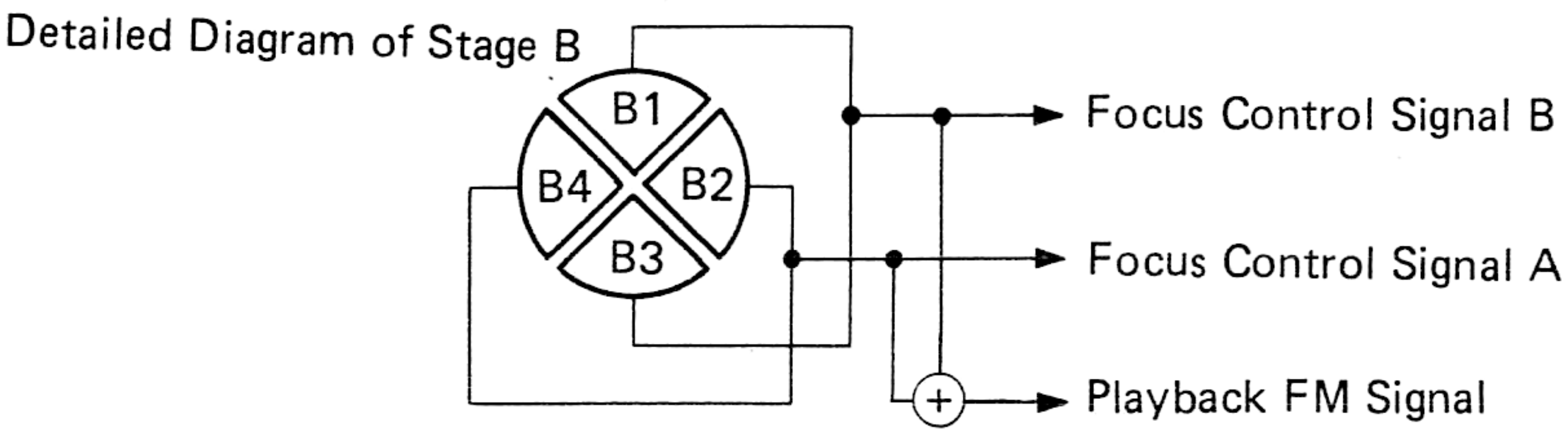


Fig. 42

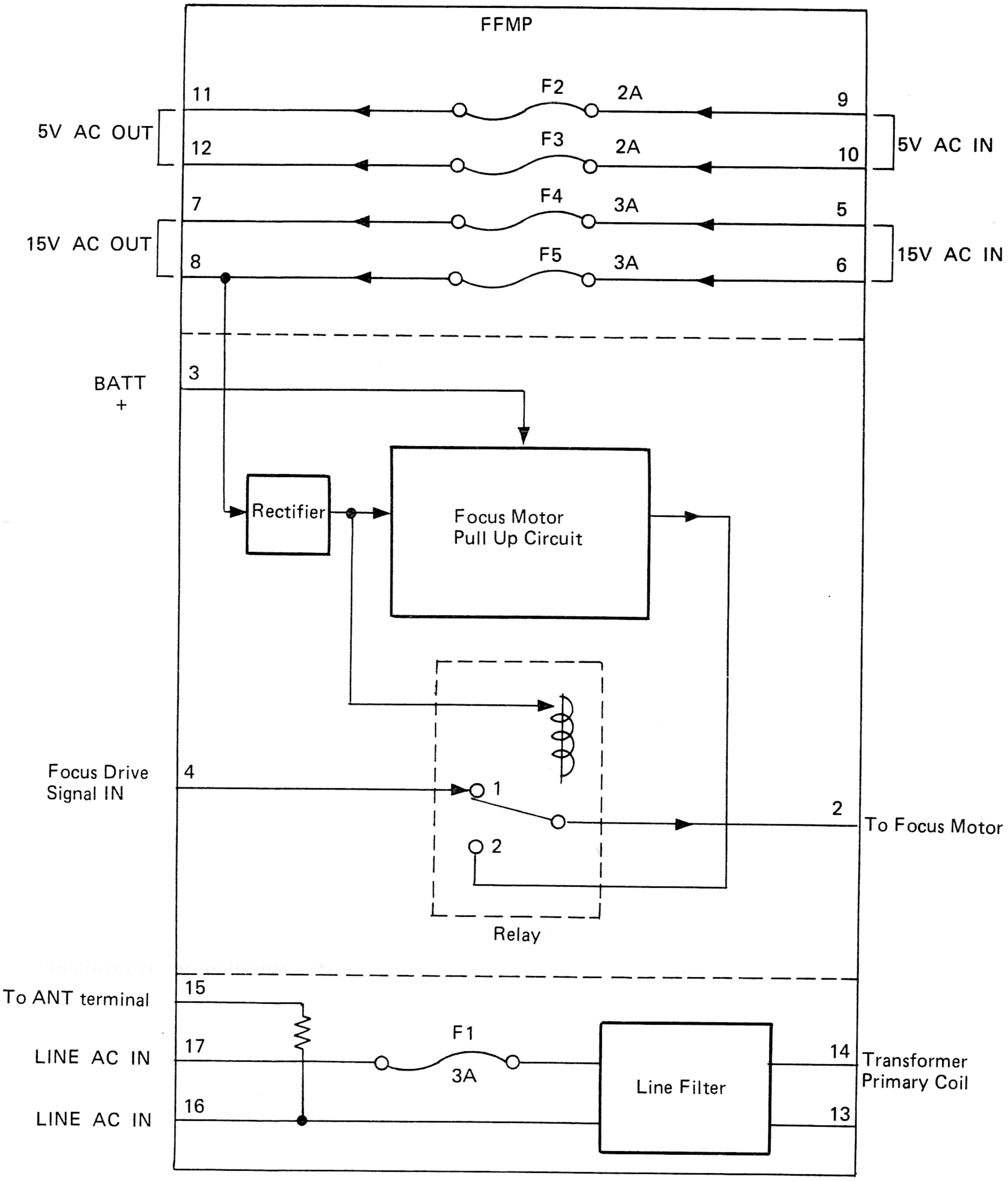
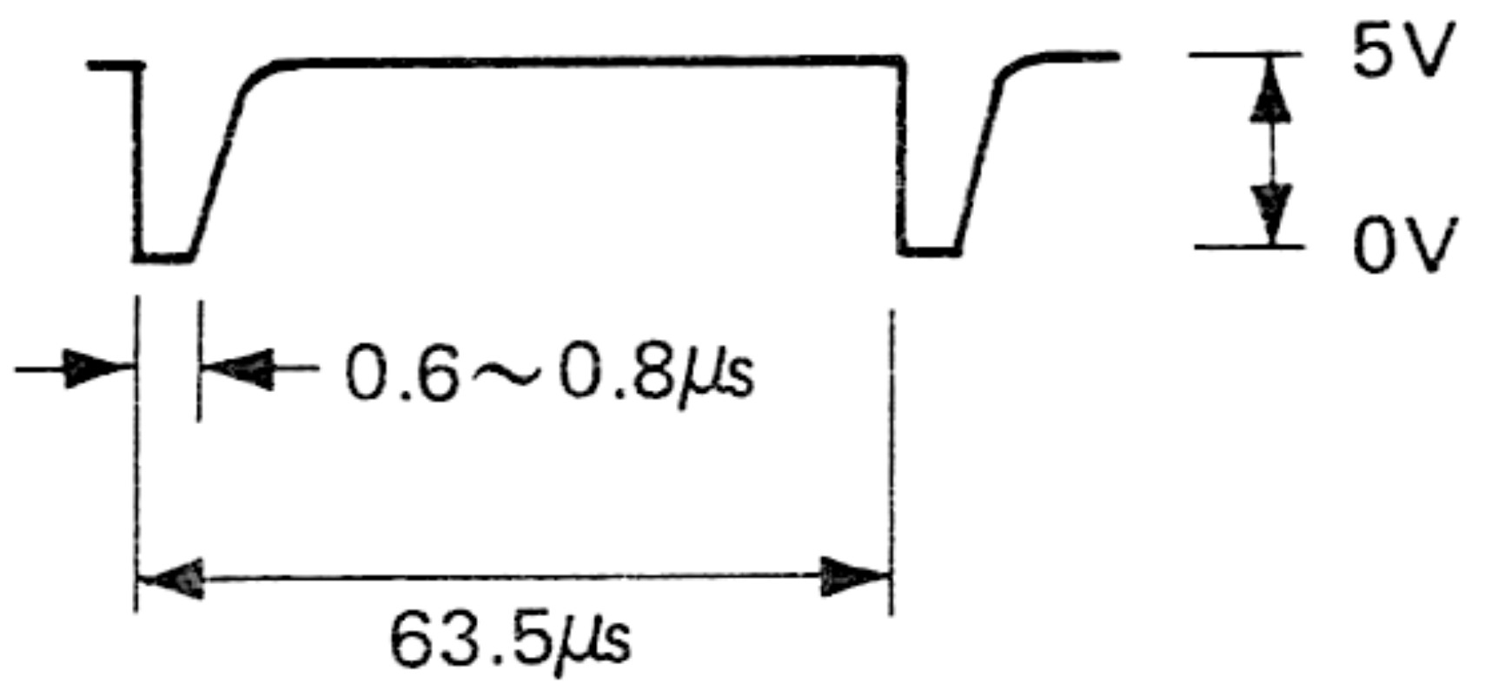
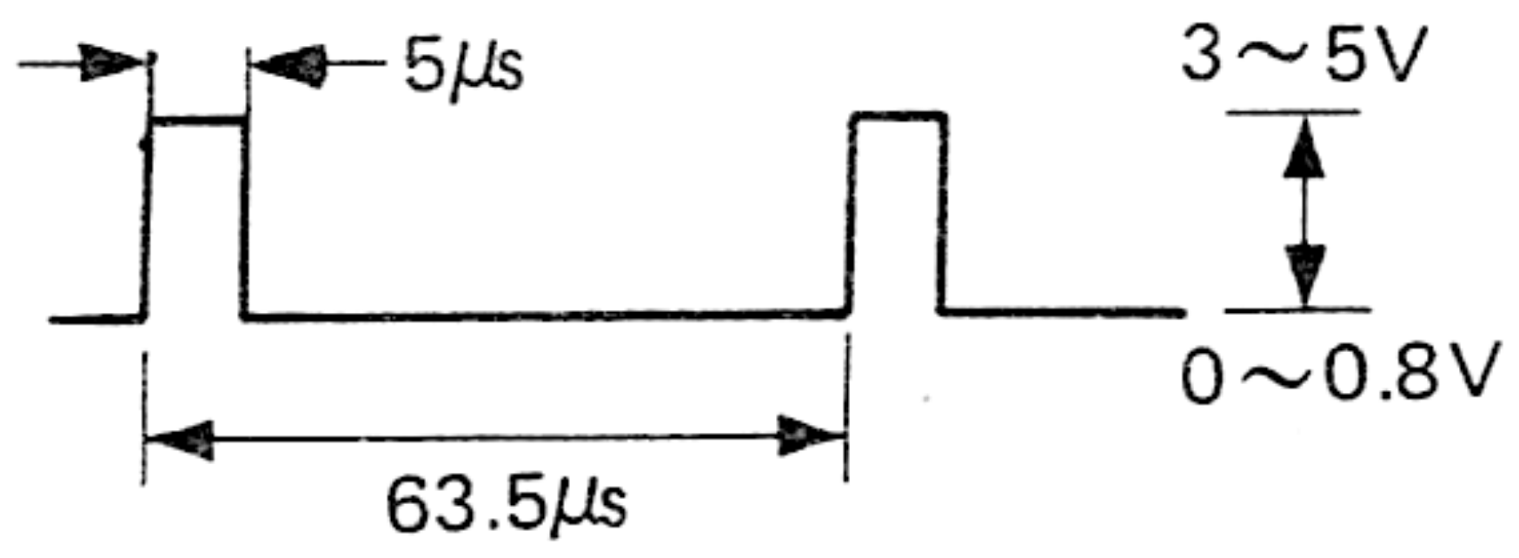
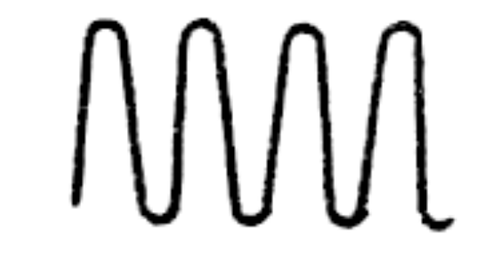

FFMP
11
F2
2A
9
5V AC OUT
12
F3
2A
10
5V AC IN
7
F4
3A
5
15V AC OUT
8
F5
3A
6
15V AC IN
BATT
+
3
Rectifier
Focus Motor
Pull Up Circuit
Focus Drive
Signal IN
4
1
2
2
To Focus Motor
Relay
To ANT terminal
15
LINE AC IN
17
F1
3A
Line Filter
14
Transformer
Primary Coil
LINE AC IN
16
13

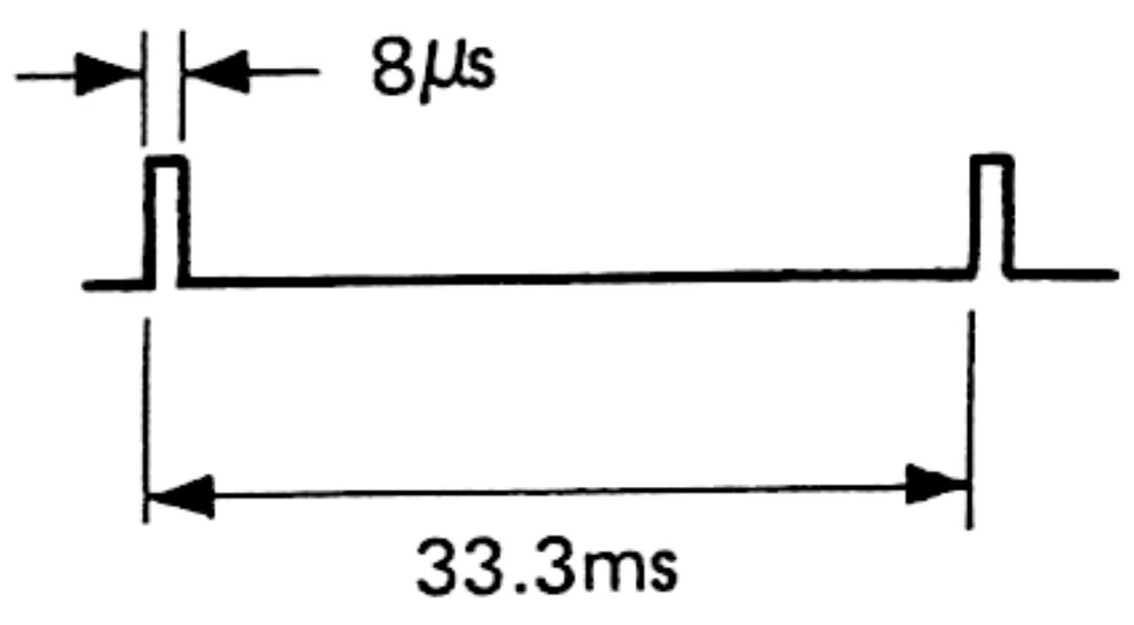
Fig. 43

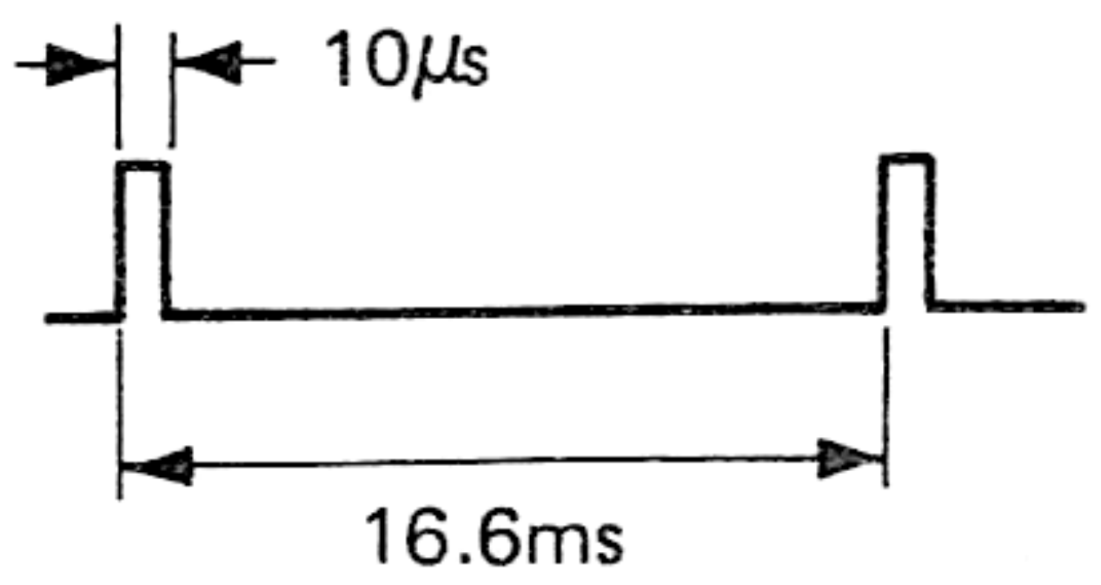
10. TROUBLE SHOOTING CHART

	Problem	Cause	Repair Method
1.	Power lamp does not light up when power switched on.	AC 115V power cord not connected.	
	(Primary coil fuse blown)	Defective transformer	Disconnect all secondary wiring insert a fresh fuse, and turn the power back on. If the fuse blows again, replace the transformer altogether.
	(Secondary coil fuse blown)	Power supply wiring in contact with metal parts.	Extract all circuit boards and measure the resistance between the power output terminals and ground. If a zero resistance is obtained, search for the contacting point.
		Defective circuit board.	Again extract all circuit boards, and check output voltages after replacing the fuse. Locate the defective board by replacing one by one.
2.	Disc fails to move after pressing the PLAY push-button.	Displacement in PARK switch position.	Check the PARK switch position.
		Defective PARK switch.	Replace switch.
		Defective carriage motor.	Replace motor.
		Defective CARG circuit board.	Replace circuit board.
		Defective MCPR circuit board.	Replace circuit board.
3.	Proper focussing not attained.	Beam shutter fails to open.	Adjust the beam shutter mechanism.
		Laser not activated.	Check the high voltage power supply circuit.
		Defective FOCS circuit board.	Replace circuit board.
		Platform connector disconnected.	Reconnect connector properly.
		Displacement of platform light axis.	Measure the focus error with the supplied jig. If problem is due to focus error, readjust the platform as described in the platform adjustment section.
4.	Spindle Motor fails to rotate after the PLAY push-button has been pressed.	SPDL circuit board free-run not adjusted properly.	Adjust SPDL VR5.
		Defective SPDL circuit board.	Replace circuit board.

	Problem	Cause	Repair Method
5.	Tracking servo control fails to have effect.	Displacement of platform mounting position.	Check the difference between the disc inside and outside tracking error levels. The outside level should be 0 to —4dB below the inside level. If it exceeds this difference, re-adjust the mounting position.
		Off-set VR out of adjustment.	
		Grating displacement	Adjust the grating.
		Drop in laser power.	Measure the laser power level at the laser output. If it is low, check the laser power supply.
		Defective TRKG circuit board.	Replace circuit board.
		Defective mirror unit.	Replace mirror unit.
		Defective CARG circuit board.	Replace circuit board.
		Focus gain off-set out of adjustment.	Adjust FOCUS VR1 and VR2.
		No O/L signal from MCPR.	Check TRKG (5).
6.	No picture after shift to inner circumference of disc when PLAY push-button is pressed.	SYNC switch still in EXT position.	Return the rear panel SYNC switch to the INT position, and check SPDL (4).
		SPDL circuit board not properly adjusted.	Adjust TP11 to 0 ± 0.3V by VR3, and TP8 to the same level by VR4.
		Defective SPDL circuit board.	Replace the circuit board if LOCK fails after proper adjustment.
		Defective VTBC citcuit board.	If SPDL TP8 is normal, the VTBC will be defective, and must be replaced.
7.	Spindle motor stops after attaining focus.	Defective VDEM circuit board.	Replace circuit board.
		Displaced platform light axis.	Measure laser power at laser output and below the focussing lens. Check for focus error with the supplied jig.
		Defective SPDL circuit board.	Replace circuit board.
		Anticipate Inside out of adjustment.	Adjust DSPL VR2.
		Defective carriage potentiometer.	Check voltage on SPDL (24).

	Problem	Cause	Repair Method
8.	Color lock failure although picture is obtained.	SPDL lock detector not operating.	Measure VTBC connector (16) which should be "H" when the lock is operating normally. If "L" is measured, readjust by SPDL VR3, VR4, and VR2.
		VTBC phase error sampling circuit fails to operate.	Measure VTBC TP2. Normal  Adjust VR2.
		Playback sync not applied to VTBC.	Measure VTBC (8). Normal  If no pulse signal is measured, replace the STPM circuit board.
		Sub-carrier not applied to VTBC.	Measure VTBC (26). Normally, a 250mV sine wave signal will appear. Normal  If there is no sine wave signal, measure SPDL (8), and replace the SPDL circuit board if still no signal is generated.

	Problem	Cause	Repair Method
	Color lock failure although picture is obtained.	Defective VTBC circuit board.	If SYNC, SC and VIDEO IN signals are normal, replace the circuit board.
		Defective VDEM	Measure VTBC (11) and check the presence of a burst in the video signal. Replace the VDEM circuit board if the burst is absent, but replace the VTBC circuit board if the burst is present.
9.	No sound.	Defective AUDB	Switch channel 1 and channel 2 on the front panel, and check AUDB during the switching action by measuring at the TP3 and TP4 terminals. Replace the AUDB circuit board if no waveform appears. If there is a signal present, check the harness between the circuit board and the output terminals.
		Defective MCPR.	Switch front panel channel 1 and channel 2. If the switching operation fails to occur, replace the MCPR circuit board.
10.	Still picture not obtained when the STOP push-button is pressed.	White flag signal not detected at STPM.	Attach a lead to Z13 (8) in the STPM circuit board, and press the PLAY push-button. If there is no pulse signal, replace the STPM board.
		Defective TRKG circuit board.	If the white flag signal appears in STPM circuit board, measure (9) in the TRKG circuit board. If pulses are present, replace the TRKG board.
		Defective MCPR circuit board.	When there is no pulse at (9) in the TRKG circuit board (with a normal STPM board), replace MCPR. 

	Problem	Cause	Repair Method
11.	No change in the frame number shown in the screen.	D & CR circuit board not adjusted properly.	Observe the waveform at TP9 in the D & CR circuit boad. Adjust the mechanical center point to within the range of valid data pulse. 
		Defective DSPL or MCPR circuit board.	If the valid data appears normally, replace DSPL and MCPR.

11. GENERAL ADJUSTMENTS

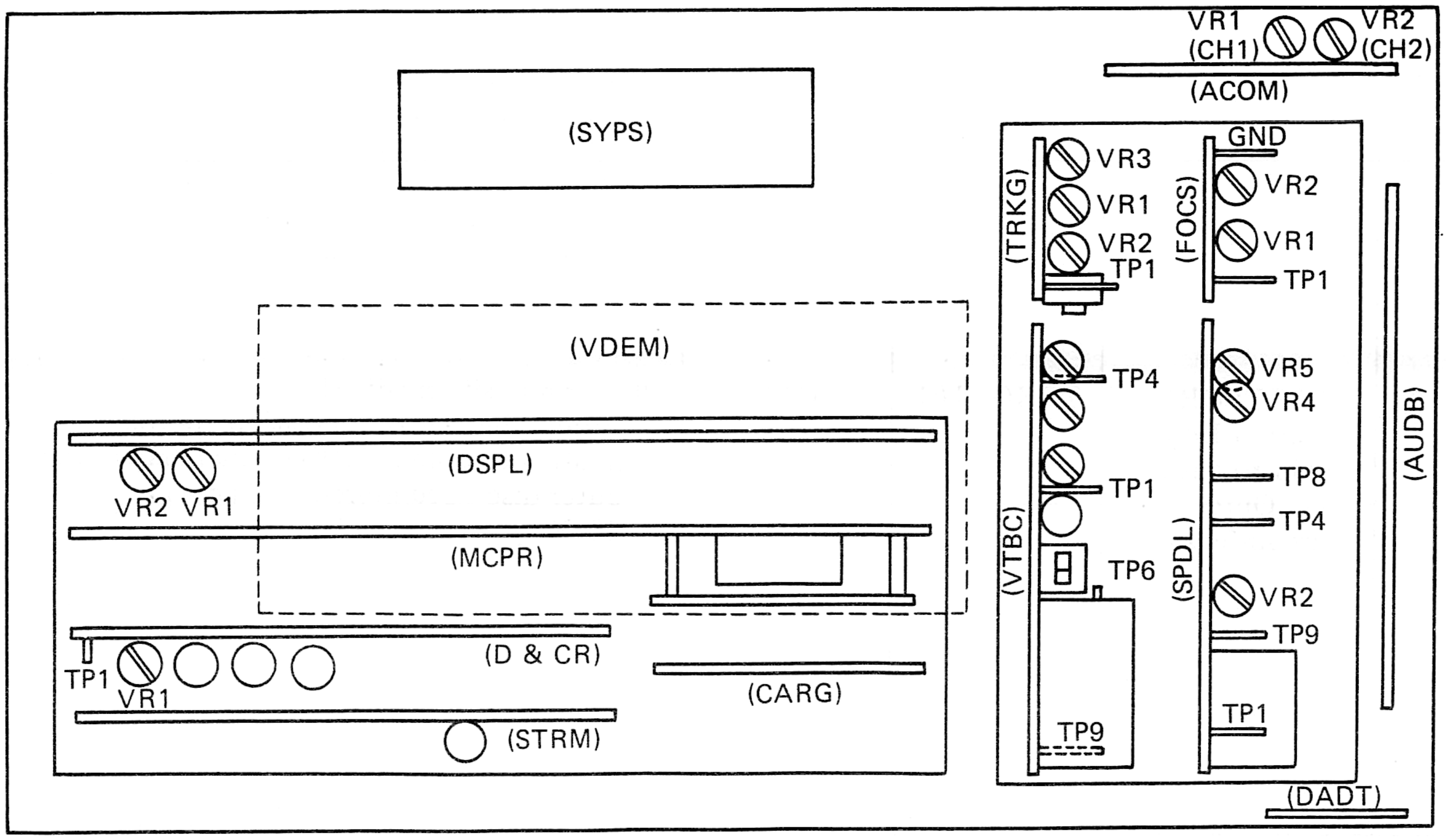
Check the following points prior to commencing a general adjustment of the PR-7820.

1. Check all power supply voltages, and the positions of all microswitches. Also check resistance (150 ± 50Ω) at CARG. POT. end position.
2. Preset the DSPL VR1 & 2 (Anticipate Outside & Inside). (Turn VR1 clockwise and VR2 counter-clockwise to max position).
3. Check FFMP operation (focus motor lens up by power switch ON ↔ OFF during "battery support").
4. Check that the SYNC selector switch is in the INT position, the VTBC loop switch in the O/L position, and the TRKG loop switch in the C/L position.
5. All discs used should be UPC test discs (CAV, CLV, and program dumping).
6. Although the μ-com is used, operate in service mode until completion of platform adjustments.

NOTES:

1. *Since LENS UP & DOWN can also be operated manually, immediately move the lens up (stop/push operations) if proper focus is not attained).*
2. *When the PARK or END position is reached during SCAN FWD & REV MODE, release the button immediately.*

ADJUSTMENT LOCATION

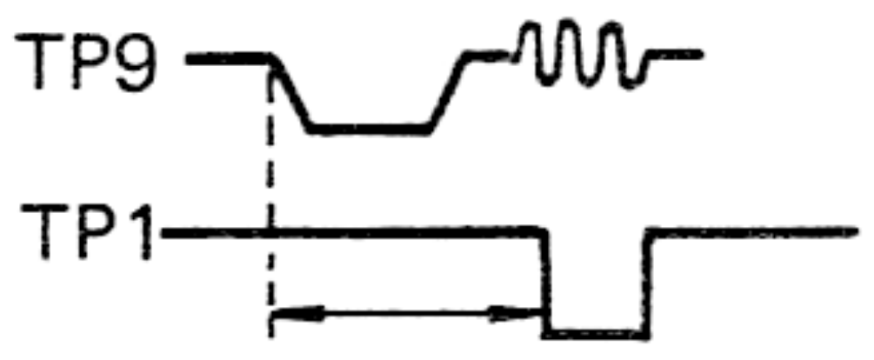
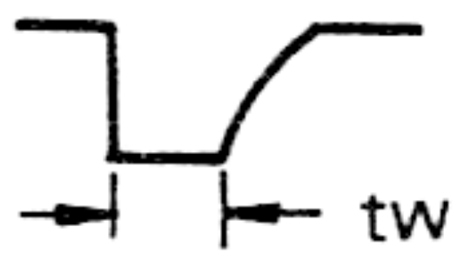


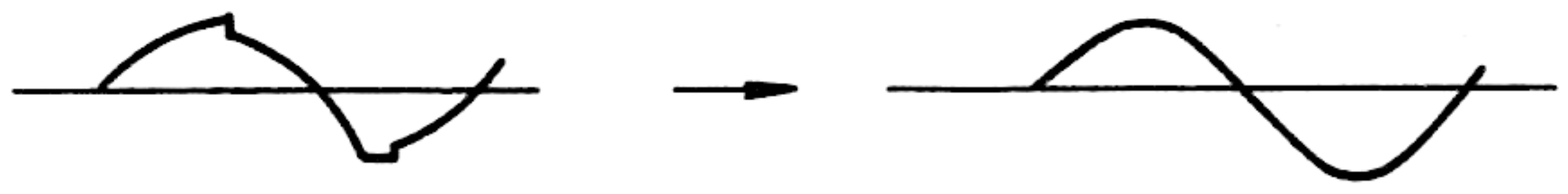
STEP NO.	Adjustment circuit board (and VR No.) or name of adjustment position.	TP NO.	Disc and conditions	Adjustment and check details
1			CAV	Set μ-com to service mode (& RAM CLEAR) Turn power switch on while pressing the RAM CLEAR switch.
2			CAV	Spindle running check Confirm the Spindle running when the SEARCH button is pressed, and Spindle stop when the AUTO STOP button is pressed.
3			CAV	Carriage operation check Switch back and forth between PARK and END position by SCAN FWD and SCAN REV. modes, and check for normal carriage transport speed.
4	TRKG VR3		CAV	TRKG. mirror bias check Check that the voltage of TRKG. mirror drive position, is a 0V ± 0.1V (readjusting VR3 at TRKG O/L if necessary).
5			CAV	Proper focussing check (Set the FOCS gain VR2 into an approximate 10 o'clock position). Check the proper focussing is obtained while switch back and forth between PLAY (lens down) and STOP (lens up) positions.
6	PLATFORM Position Rough adjustment at Outer circumference	TRKG: TP1	CAV	Platform position adj.—1 Adjust the platform position approximately to obtain TRKG signal max at the outer disc circumference (frame no. 40,000).

STEP NO.	Adjustment circuit board (and VR No.) or name of adjustment position.	TP NO.	Disc and conditions	Adjustment and check details
7	FOCS: VR1	TRKG: TP1	CAV	Platform position adj.—2 Adjust FOCS offset VR1 to obtain TRKG signal max.
8	PLATFORM back and forth position adjustment	TRKG: TP1	CAV	Platform position adj.—3 After shifting DISC to inside circumference (frame no. 100), fine adjust the platform back and forth position; and set temporarily at the TRKG signal max position.
9	GRATING	TRKG: TP1	CAV	Grating adjustment Shift disc to frame no 10,000, and turn the grating adjustment screw clockwise. Check positioning above the same track as the main beam with the waveform at the first TRACK signal min position. Then turn counter-clockwise, and temporarily set at TRKG signal max. Also check TRKG signal max at both frame no. 100 and 40,000.
10		TRKG: TP1	CAV	Platform position setting Check that the TRKG signal level difference between the disc outer and inner circumferences lies within the 0 ~ −4dB range. Then lock the platform set screw and grating. (If readjustment is considered necessary, repeat step 8).
11	TRKG: VR1	TRKG: TP1	CAV	TRKG O/L signal AC offset adjustment Adjust the TRKG signal waveform AC center to 0V at the disc outer circumference (frame no. 40,000). (The positive and negative peak values should be equal in respect to 0V DC).

STEP NO.	Adjustment circuit board (and VR No.) or name of adjustment position.	TP NO.	Disc and conditions	Adjustment and check details
12	FOCS: VR1	FOCS: TP1	CAV	Check FOCS offset voltage at TRKG O/L signal max Push AUDIO—2 [TRKG C/L] at disc frame no. 100, turn the offset VR (VR_1) CW and CCW direction, then read the voltage $VT_{(-)}$, $V_{T(+)}$ of the drop out begin to show on the screen. And then, Set VR to middle (V_T) of the both values, and read the RF level (E_{RT}).
13	FOCS: VR1 & RF. TP. Point	FOCS: TP1 & RF. TP.	CAV	Check FOCS offset voltage for RF signal max Adjust offset VR1 to obtain RF max, and take note of the voltage reading (E_{RM}). (Specification rating: $\|V_T\| \leqq 0.8V$, $E_{RT}/E_{RM} > 0.85$.
14	FOCS: VR1	FOCS: TP1	CAV	Check voltage difference between RF max and TRKG max FOCS offset voltages Check that the voltage difference between RF max offset voltage (V_R) and TRKG max offset voltage (V_T) is less than ±0.7V. Then at frame no. 100, set the FOCS offset to V_T.
15	TRKG: VR2	TRKG: TP1	CAV	Approximate TRKG gain adjustment Push AUDIO—2 (TRKG C/L) and adjust to optain TRKG error min, checking that there is no oscillation at the innermost circumference. (Note that approximate adjustment only is required at this stage).
16	FOCS: VR2	FOCS: TP1	F/N #45000	FOCS gain adjustment Adjust VR2 to obtain FOCS error min at the outer disc circumference (frame no. 45,000), but checking that the gain is not increased too far.

STEP NO.	Adjustment circuit board (and VR No.) or name of adjustment position.	TP NO.	Disc and conditions	Adjustment and check details
17			F/N #100	Proper focussing and TRKG O/C check Switch back and forth between PLAY (lens down) and STOP (lens up) positions several times at the inside disc circumference (frame no. 100) to check for normal operation. Then switch back and forth between AUDIO—2 (TRKG C/L) and AUDIO—1 (TRKG O/L) several times, again to check for normal operation.
18	SPDL: VR1	Strobescope	CLV	SPDL free run speed adjustment Adjust to about 1700 ± 50rpm at the PARK position during μ-com service mode. Note, however, that the final specification is 1800 ± 100rpm.
19			CLV	Set μ-com to normal mode Turn power switch off and on, and then press PLAY.
20	SPDL: VR4	SPDL: TP8	CLV	SPDL H-error offset adj.—1 Monitor the H-error, and adjust the center of the 30Hz AC component to 0V (approximate adjustment). Then check SPDL lock from the waveform.
21	SPDL: VR3	SPDL: TP11	CLV	SPDL tacho error offset adjustment (0.25 ± 0.1V)
22	SPDL: VR4	SPDL: TP8	CLV	SPDL H-error offset adj.—2 Repeat SCAN FWD, REV and REJ, PLAY 3 to 5 times within the +1V~ −1V SPDL H-error offset range (at 85μm eccentricity), and adjust that the lock in point is within several seconds in either case. Then, confirm that H-error is not hunting.

STEP NO.	Adjustment circuit board (and VR No.) or name of adjustment position.	TP NO.	Disc and conditions	Adjustment and check details
23	VDEM VR1 VR5		CAV F/N #100	VDEM DOS sensitivity adjustment Stop at the innermost disc circumference (frame no. 100). Turn VR1 counter-clockwise and stop at a position with many drop-outs shown in the screen. Next turn VR5 to a position with minimum drop-outs on the screen, and fix at that position. Then with VR1 turned fully clockwise, check that the screen drop-outs have been compensated, and fix at that position.
24	VTBC VR1 VR2	VTBC TP1 TP2	CAV F/N #100	Burst gate timing adjustment Set the VTBC loop O/C switch to the O/L position. Turn VR1, and adjust the burst gate pulse negative going edge delay to 6 ± 0.2μsec from the SYNC tip negative edge.  Then turn VR2 and adjust pulse width to 0.7 ± 0.1μsec. 
25	VTBC VR4	TP4	CAV F/N #100	Error offset adjustment Adjust the AC center to 0V (0 ± 0.2V), and set the O/C switch to C/L.
26	VTBC VR10	Line out	CAV #2000 ~ #3500	Video level adjustment Adjust to 1V ± 0.1V (after first checking that the input level at pin 11 of the circuit board connector is 1V ± 0.1V).

STEP NO.	Adjustment circuit board (and VR No.) or name of adjustment position.	TP NO.	Disc and conditions	Adjustment and check details
27	VTBC VR5 VR6 VR7	TP4 TP6 TP9 PIN 11	CAV (80μm eccentricity)	H-error injection level adjustment Minimize the stepwise difference generated in the TP6 error waveform during PLAY mode at an inner disc circumference (below frame no. 1,000).  Adjust the amount of delay between pin 11 and TP9 to 45.5μsec. by means of VR6 (C/L) and VR7 (O/L), and then set to O/L.
28	SPDL VR2	VTBC: TP9 SPDL: TP1	CAV	SPDL H-sync phase adjustment Align the positive going edge of the SPDL TP1 square waveform with the negative going edge of the VTBC — TP9 playback video H-SYNC. (Specification rating: ±3μsec).
29	ACOM VR1 (CH1) VR2 (CH2)	AUDIO Line out	F/N #2700~ #1~	ACOM hum suppressor level adjustment Using the test disc CH1 (frame no. 2700) and CH2 (frame no. 1) unrecorded waveforms, adjust the AC level of all AUDIO outputs (particularly the 30Hz component) to minimum positions by means of corresponding VRs).
30	D & CR VR1	TP9	CAV	Valid data adjustment Adjust to the center of the range in which the valid data pulse rises.
31	TRKG VR2	TRKG TP1	F/N #100	Fine adjustment of TRKG gain Put into STOP mode at frame no. 100 of the disc, and adjust to minimize the error waveform. Check that the stop pulse transient has been reduced to less than half.

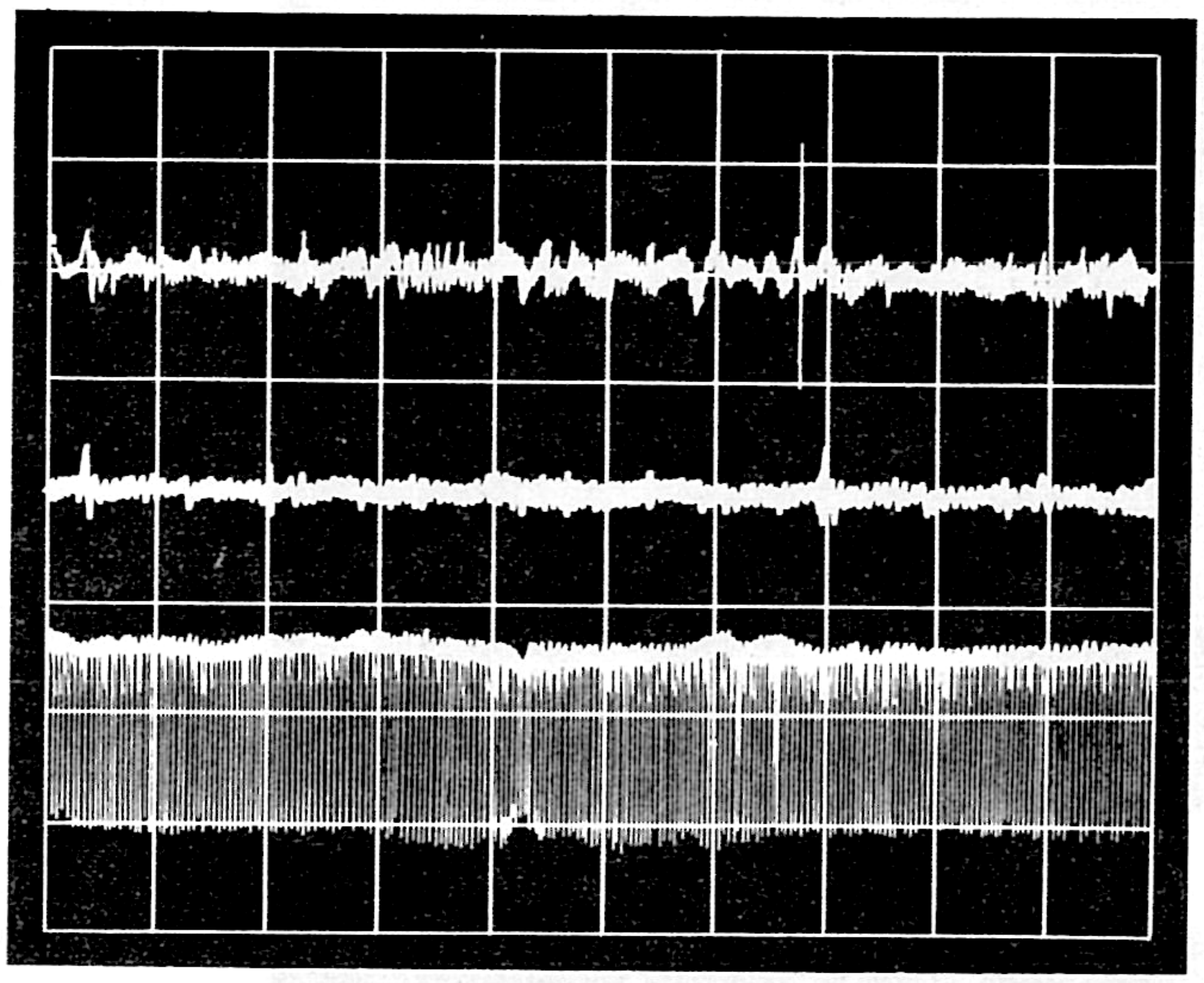
STEP NO.	Adjustment circuit board (and VR No.) or name of adjustment position.	TP No.	Disc and conditions	Adjustment and check details
32			CAV	Inside limit switch position check Set the DSPL VR2 to max position in clockwise direction, and while pressing SCAN REV, pass through frame no. 0, and confirm that the carriage shifts to the center of the disc prior to nearing a mechanical shock noise.
33	DSPL VR2	Monitor	CAV	Anticipate inside adjustment Set to SCAN REV mode from the center of the disc, and adjust so that the frame numbers for carriage speed change from mid to slow will be about 500 ± 150.
34	DSPL VR1	Monitor	F/N #49130 At above frame no. 49130 (which corresponds to frame no. 54000 when converted to the general disc).	Outside limit adjustment Set to SCAN FWD from the center of the disc, and adjust for switch over to STOP mode at a position a little above frame no. 54000.
35	SPDL	EXT-COMP & Line OUT	CAV	EXT — LOCK check Set the SYNC switch to EXT, and after applying the external COMP. SYNC and Sub carrier inputs, check that the external COMP. SYNC and LINE OUT frame & H-sync are in phase with each other. (Specification rating approximately ±5μsec). Also check color lock in monitor. (Also confirm absence of abnormal operation up to COMP SYNC : 2~4Vp-p, SC : 250mV ~2Vp-p).

STEP NO.	Adjustment circuit board (and VR No.) or name of adjustment position.	TP NO.	Disc and conditions	Adjustment and check details
36	Check of all CAV functions		CAV	CAV disc function checks Check all CAV disc functions (front panel and remote control switches (especially STEP, SLOW, and SEARCH).
37	TRACKING ERROR during SEARCH MODE	TRKG: TP1 SPDL: TP9 DC & R: TP9	CAV	Tracking error waveform during SEARCH mode During SEARCH mode covering frame nos. 100 to 40,000, the tracking error depression should be less than −6dB. However, for −5 to −6dB cases, check that there are no SPDL playback sync omissions, and that valid data is normal.
38	CLV DISC check		CLV	Check operation with CLV disc Play a CLV disc and confirm that the color lock and X-P lamps on the monitor light up. (Also check this operation at the outer and inside circumferences, and locking at inside disc circumference by repeating REJ ↔ PLAY several times).
39	SPDL		CLV	SPDL and free run check with CLV disc Play the CLV disc and shut the beam near the outer circumference of the disc (and wait several seconds). Then after infocussing, check that the SPDL — LOCK operates.
40	DATA-DUMPING		DUMP DISC	Data dumping operation check Turn the power switch off, and then on again and check that the AUDIO 1 & 2 indicator lamps light up. Then after PLAY/PUSH, confirm the automatic loading. (Repeat the REJ ↔ PLAY modes several times). Next turn AUDIO—2 off, and confirm normal PLAY by REJ ↔ PLAY operation.

STEP NO.	Adjustment circuit board (and VR No.) or name of adjustment position.	TP NO.	Disc and conditions	Adjustment and check details
41	Miscellaneous			Other check items 1) Picture quality (particularly beat and drop out). 2) VDP ↔ ANT selector switch. 3) Converter output. 5) EXT COMPUTER CONTROL.

12. WAVE FORMS

TRKG C/L: STOP

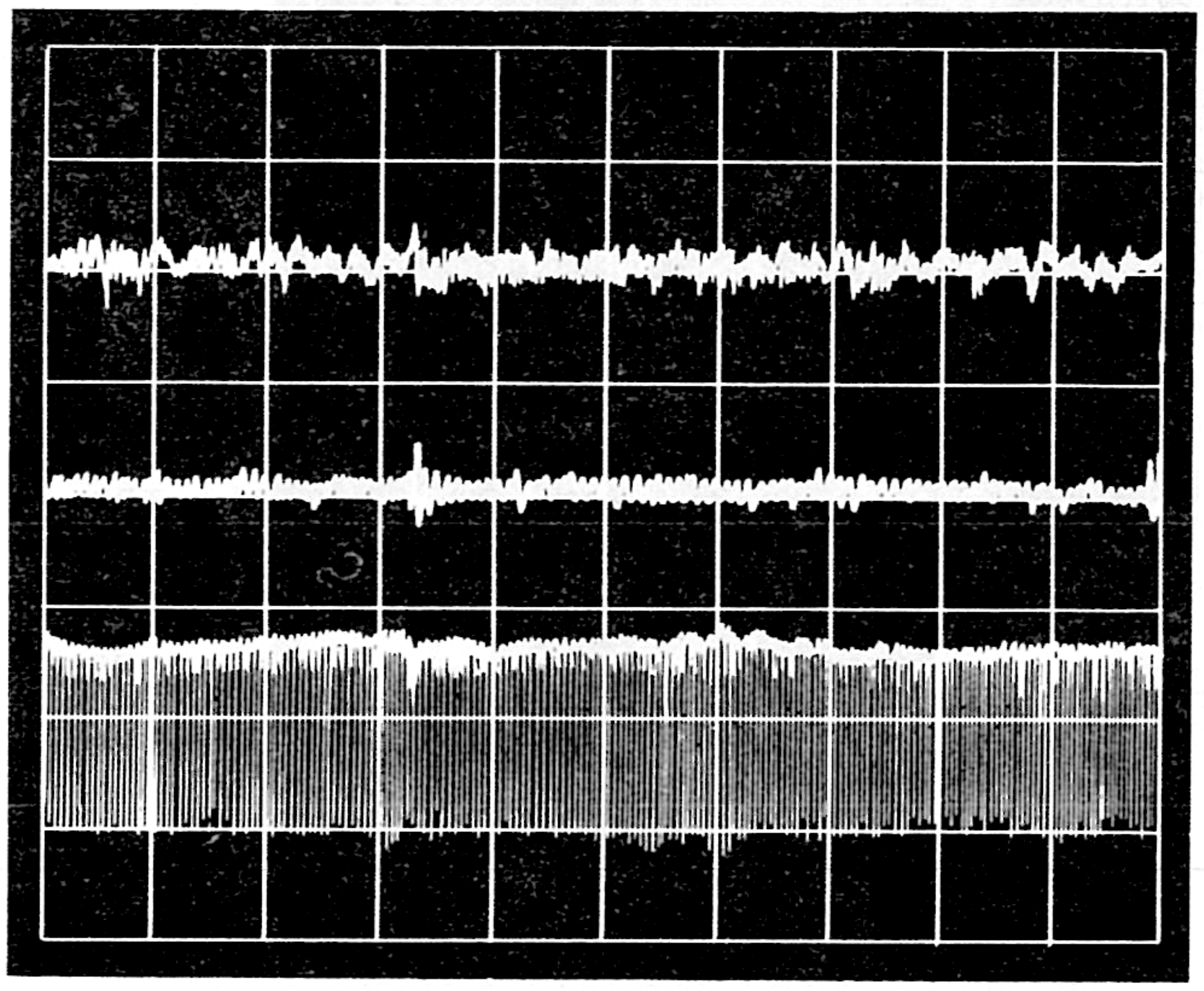


TRKG Ass'y: TP1 (Tracking Error)
5V/DIV 5ms/DIV

FOCUS Ass'y: TP1 (Focus Error)
5V/DIV 5ms/DIV

RF connector (RF Signal)
500mV/DIV 5ms/DIV

TRKG C/L: PLAY

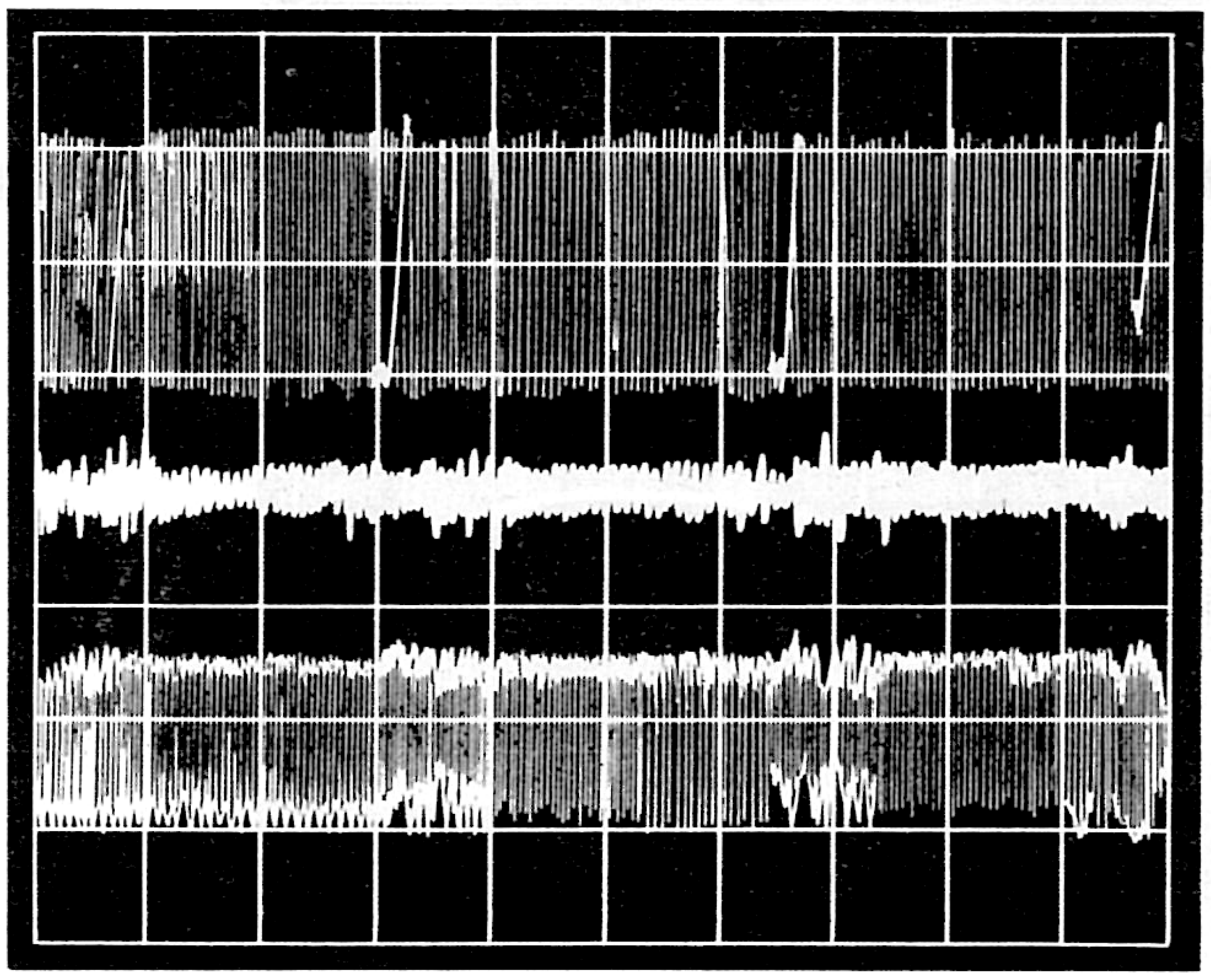


TRKG Ass'y: TP1 (Tracking Error)
5V/DIV 5ms/DIV

FOCUS Ass'y: TP1 (Focus Error)
5V/DIV 5ms/DIV

RF connector (RF Signal)
500mV/DIV 5ms/DIV

TRKG O/L: STOP

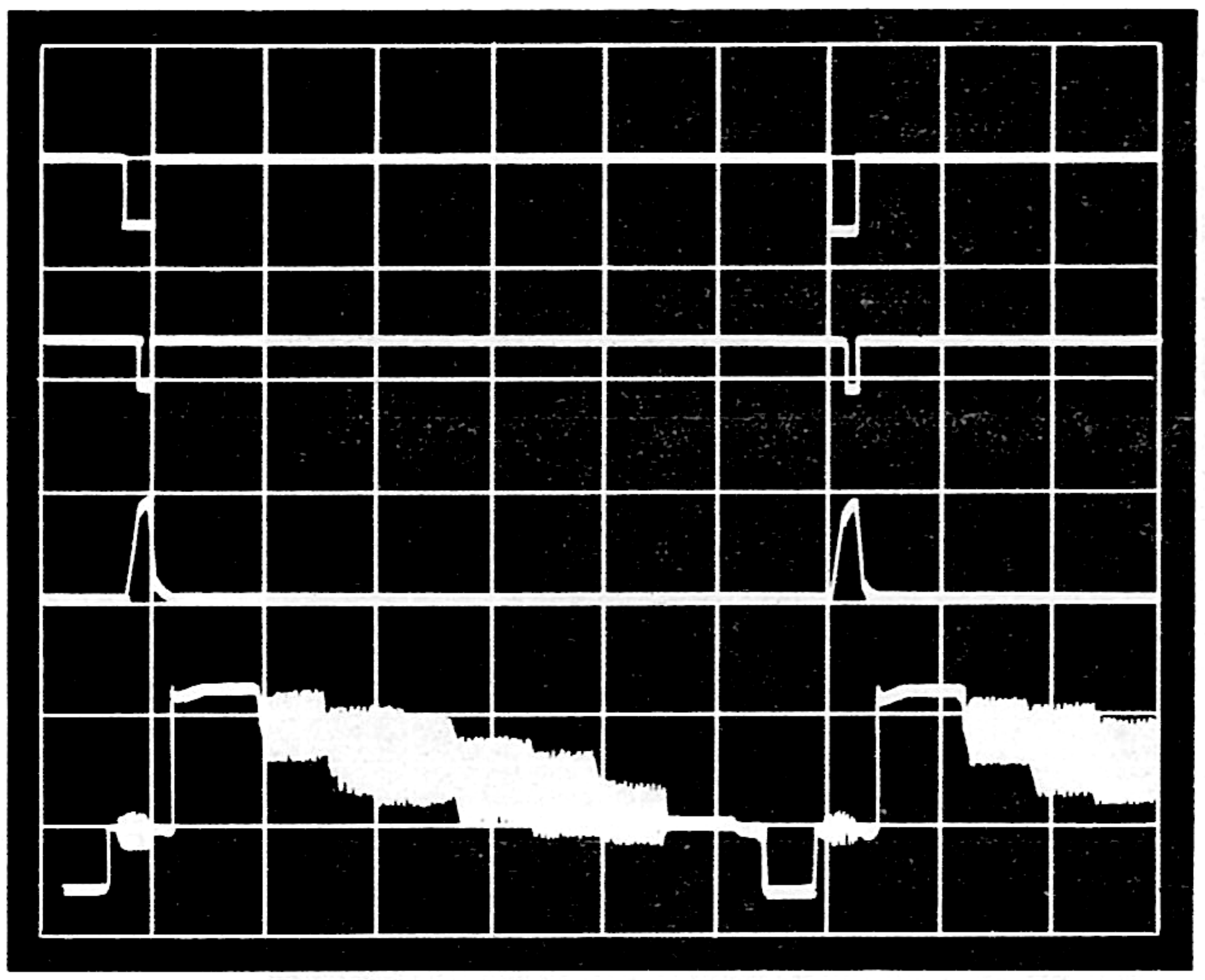


TRKG Ass'y: TP1 (Tracking Error)
5V/DIV 5ms/DIV

FOCUS Ass'y: TP1 (Focus Error)
5V/DIV 5ms/DIV

RF connector (RF Signal)
500mV/DIV 5ms/DIV

VTBC C/L: PLAY



VTBC Ass'y

TP1 (Burst Gate Pulse)

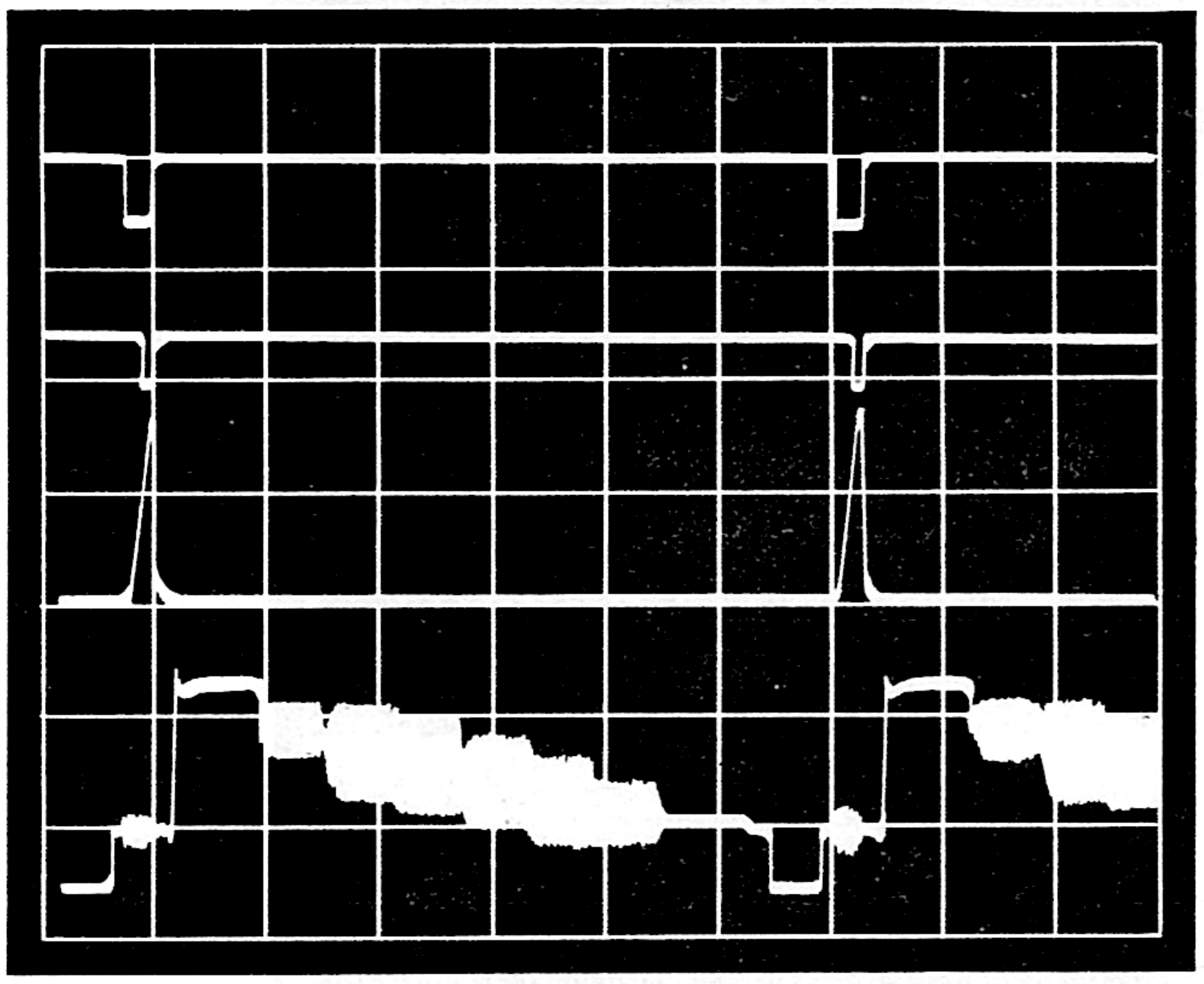
TP2 (Sampling Pulse)

5V/DIV 10μs/DIV

TP3 (Burst Phase Error)

TP8 (Playback Video Signal)

VTBC O/L: PLAY



VTBC Ass'y

TP1 (Burst Gate Pulse)

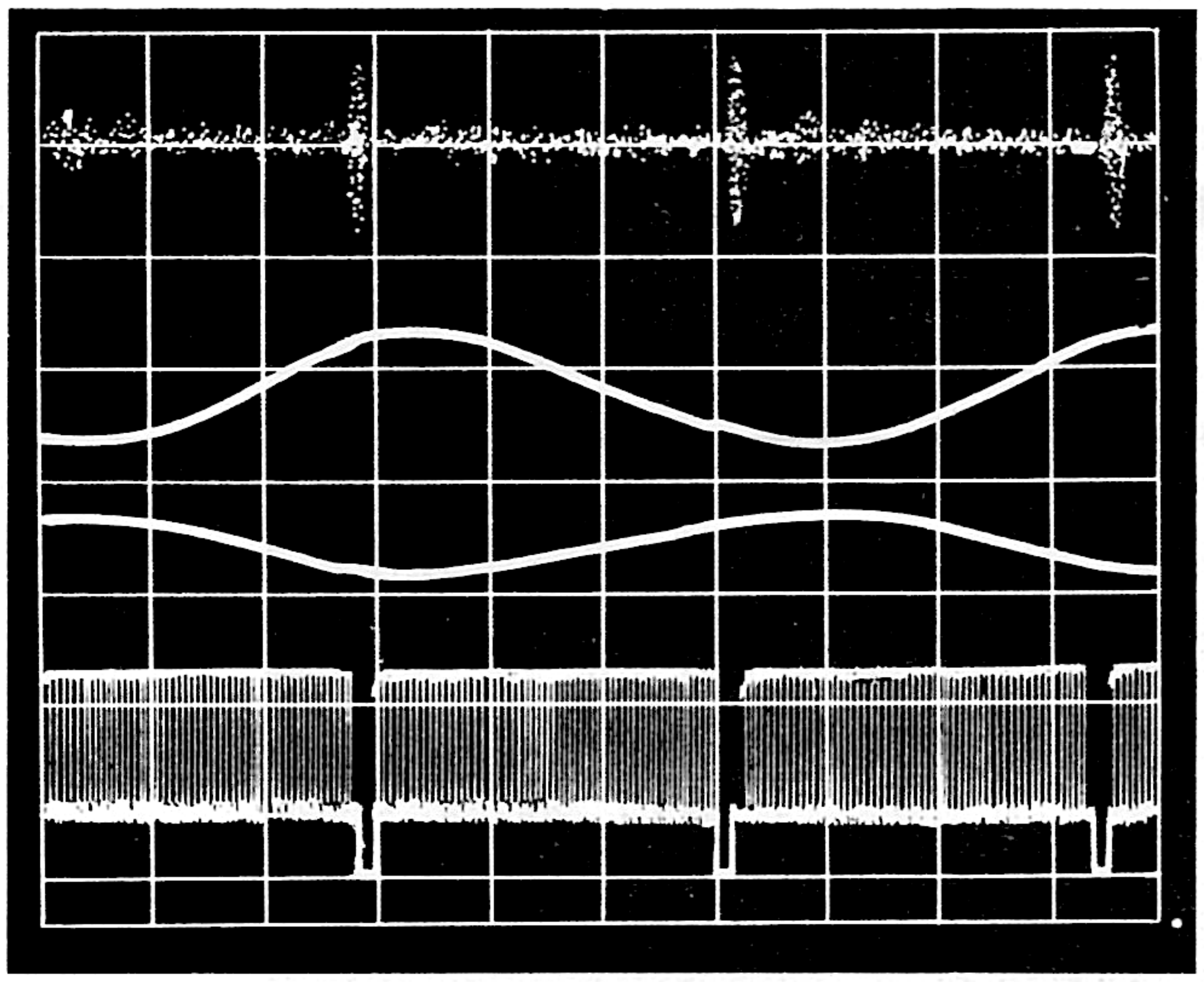
TP2 (Sampling Pulse)

5V/DIV 10μs/DIV

TP3 (Burst Phase Error)

TP8 1V/DIV 10μs/DIV
(Playback Video Signal)

VTBC C/L: STOP



VTBC Ass'y

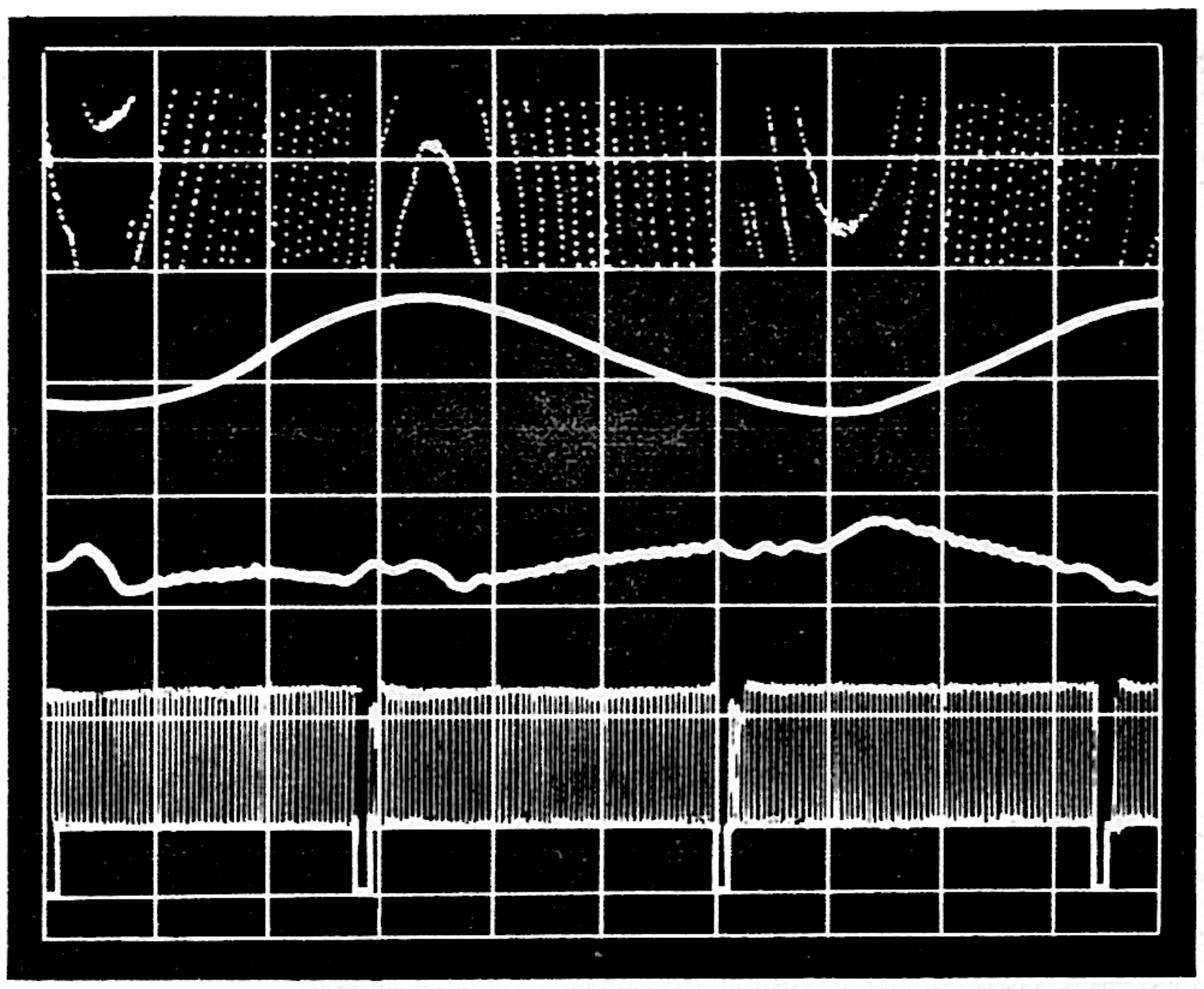
TP4 2V/DIV 5ms/DIV
(Time Base Error)

TP5 1V/DIV 5ms/DIV
(H Error)

TP6 5V/DIV 5ms/DIV
(Time Base Error)

TP9 1V/DIV 5ms/DIV
(Output Video)

VTBC O/L: STOP



VTBC Ass'y

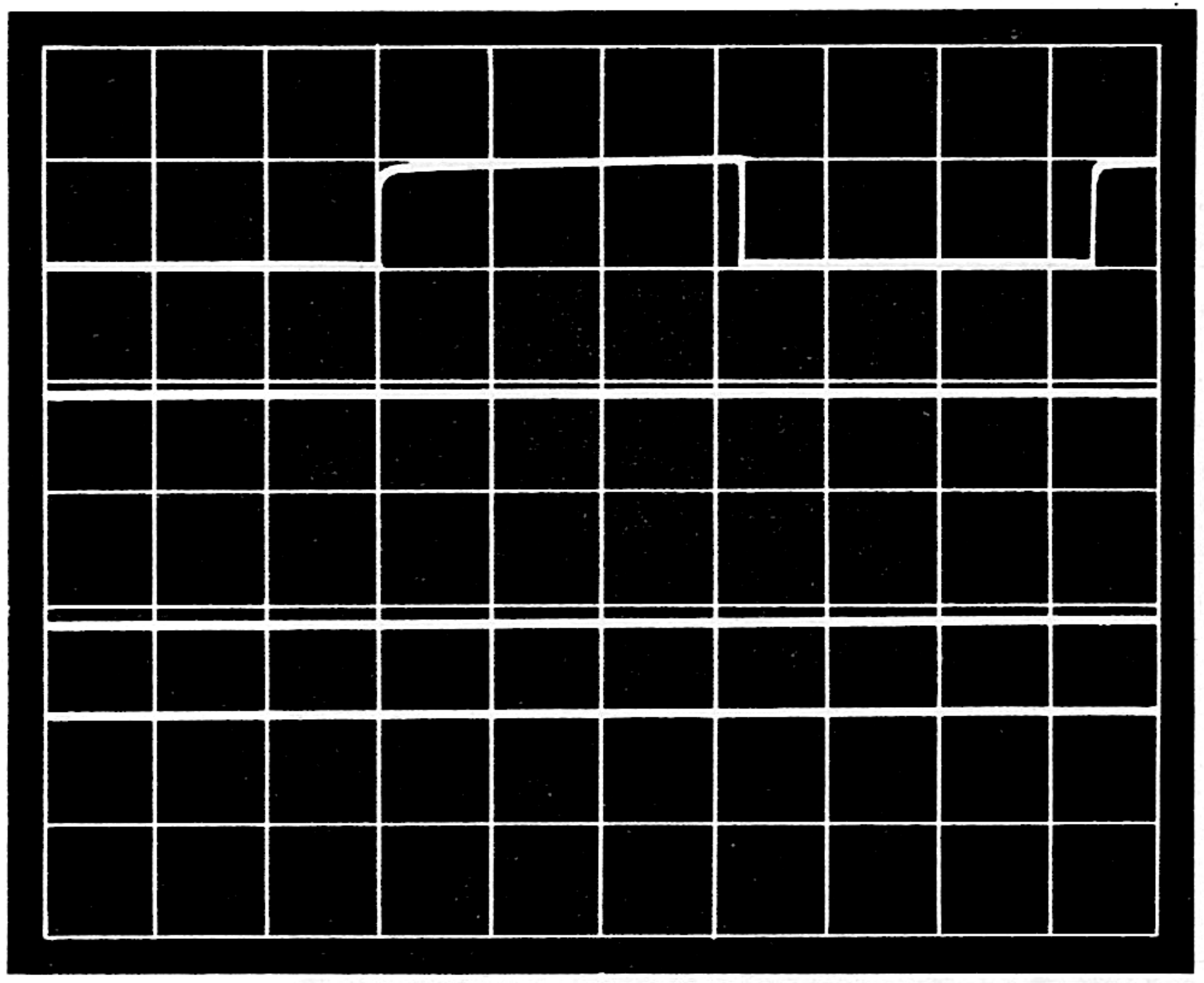
TP4 5V/DIV 5ms/DIV
(Time Base Error)

TP5 1V/DIV 5ms/DIV
(H Error)

TP6 10V/DIV 5ms/DIV
(Time Base Error)

TP9 1V/DIV 5ms/DIV
(Output Video)

SPDL
LOCK: INT



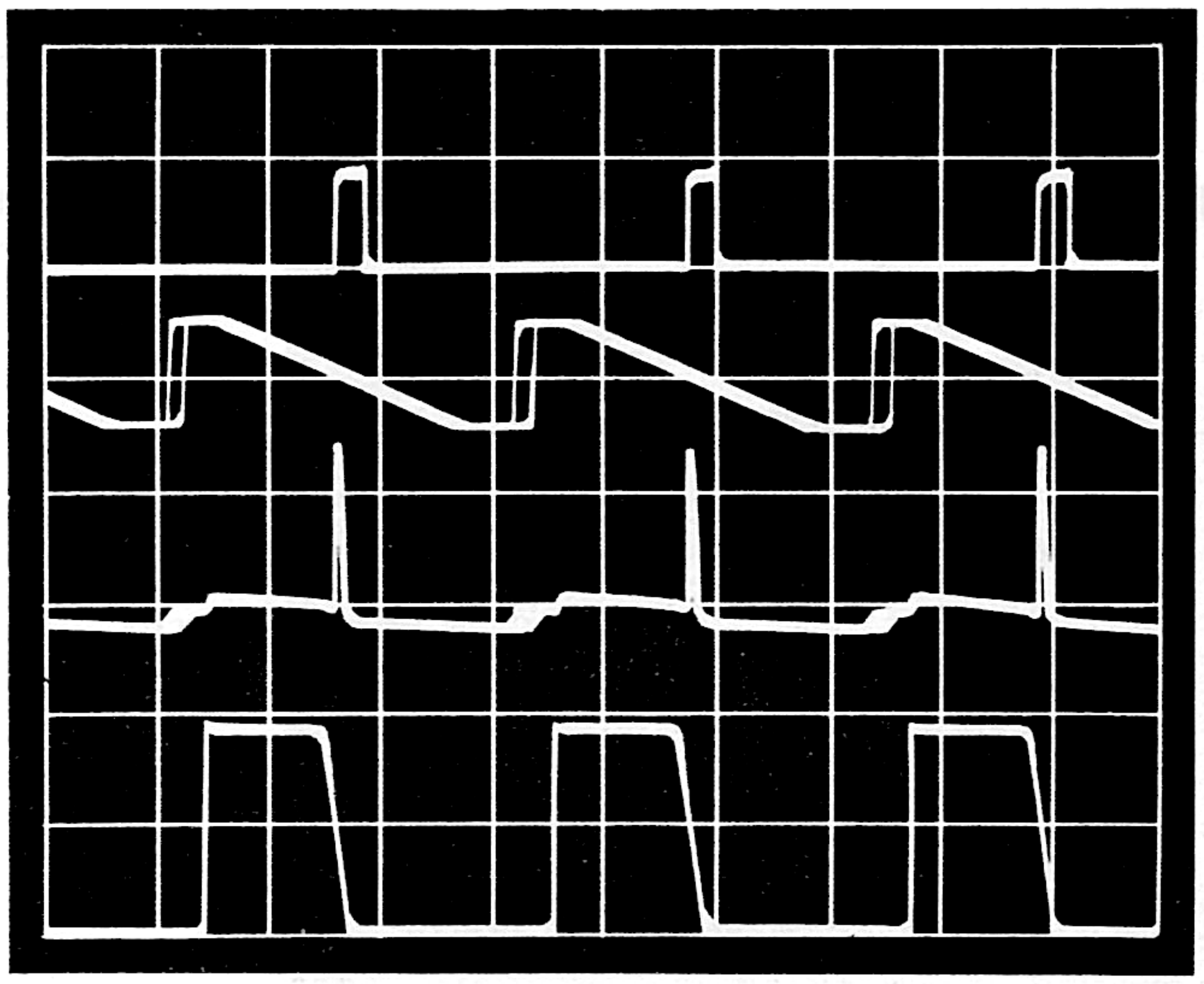
SPDL Ass'y

TP1 5V/DIV 10µs/DIV
(REF. Sync.)

TP3 +4.5V DC 10µs/DIV
(Frame Sawtooth)

TP4 −12V DC 10µs/DIV
(Playback Frame Sampling Pulse)
TP5 +5V DC 10µs/DIV
(Frame Error)

SPDL
LOCK: INT



SPDL Ass'y

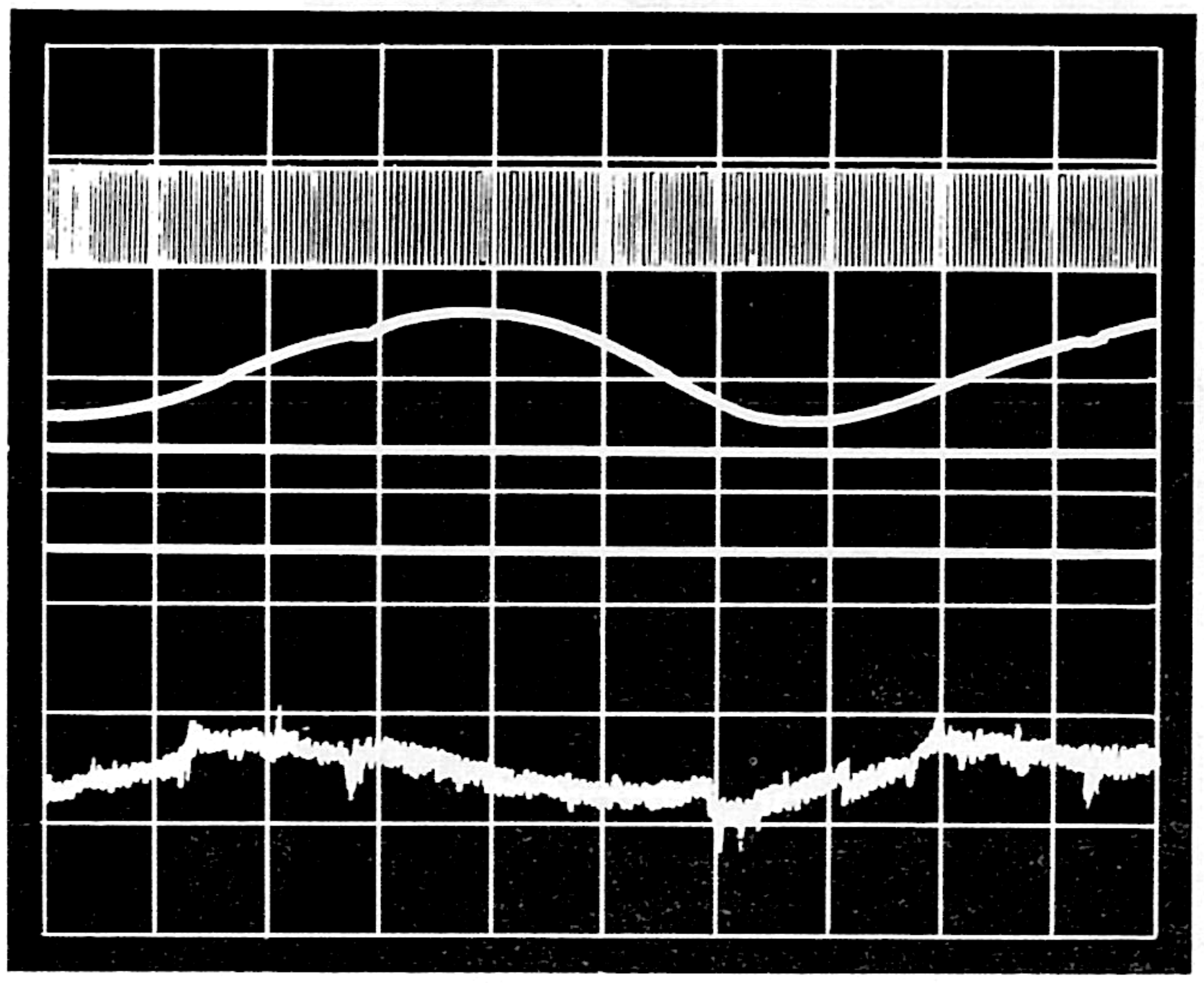
TP9 5V/DIV 20µs/DIV
(Playback Composite Sync.)

TP6 10V/DIV 20µs/DIV
(H Sawtooth)

TP7 10V/DIV 20µs/DIV
(Playback H Sampling Pulse)

TP10 5V/DIV 20µs/DIV
(Tacho Sawtooth)

SPDL
LOCK: INT
(H Rate)



SPDL Ass'y

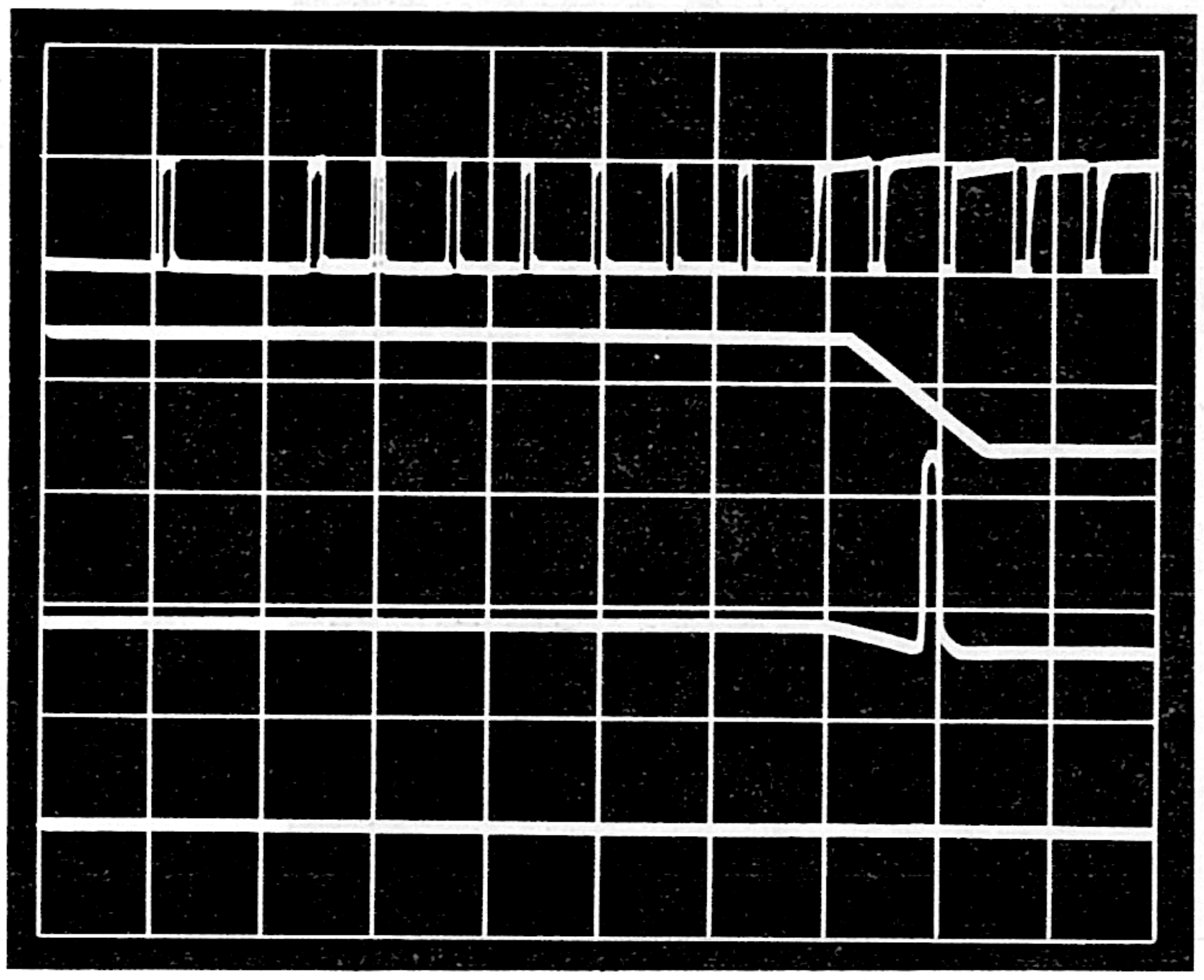
TP6 10V/DIV 5ms/DIV
(H Sawtooth)

TP8 1V/DIV 5ms/DIV
(H Error)

TP10 10V/DIV 5ms/DIV
(Tacho Sawtooth)

TP11 0.2V/DIV 5ms/DIV
(Tacho Error)

SPDL
LOCK: EXT
(H Rate)



SPDL Ass'y

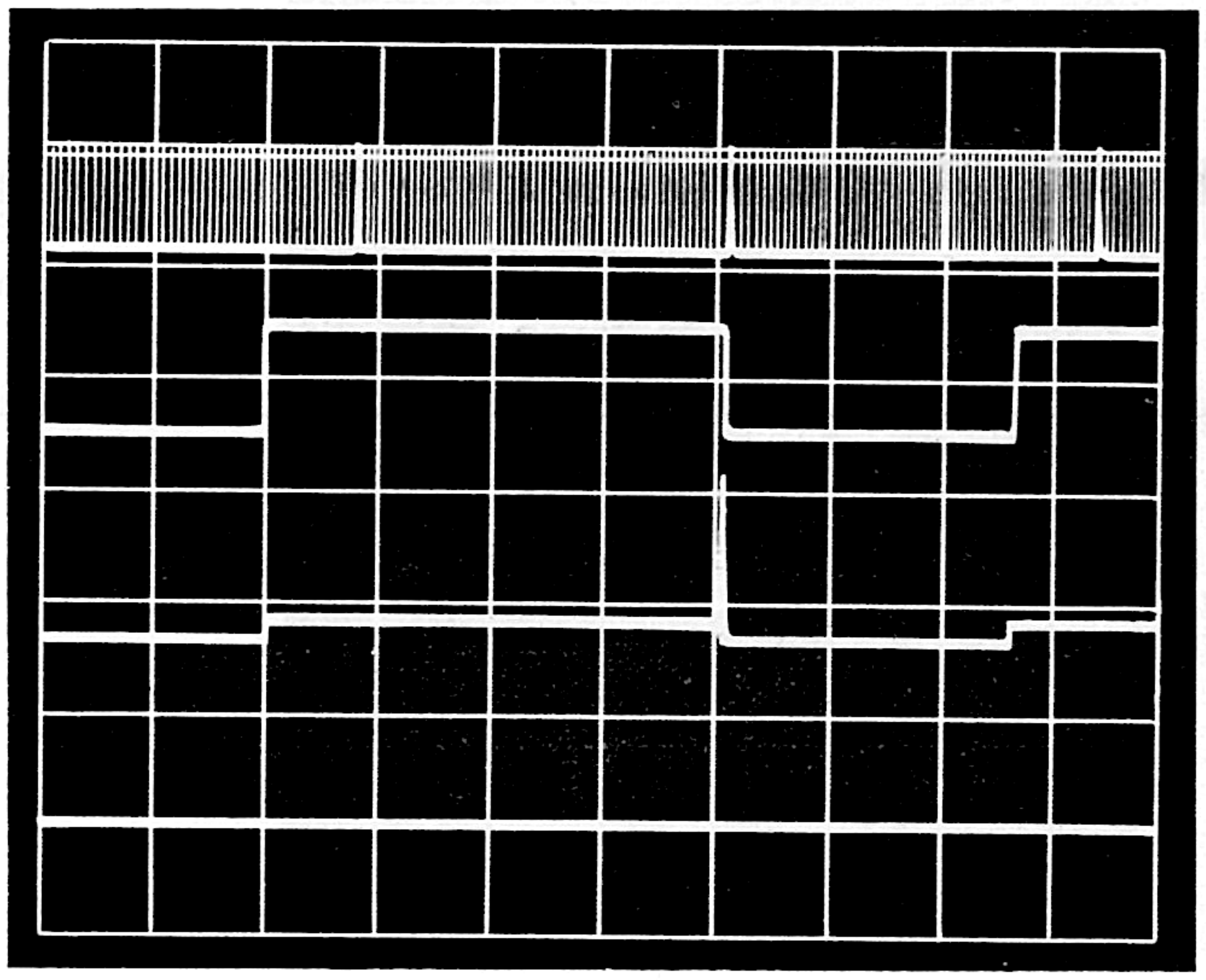
TP1 5V/DIV 50μs/DIV
(REF. Sync.)

TP3 10V/DIV 50μs/DIV
(From Sawtooth)

TP4 10V/DIV 50μs/DIV
(Playback Sampling Pulse)

TP5 0V DC 50μs/DIV
(Frame Error)

SPDL
LOCK: EXT
(V Rate)



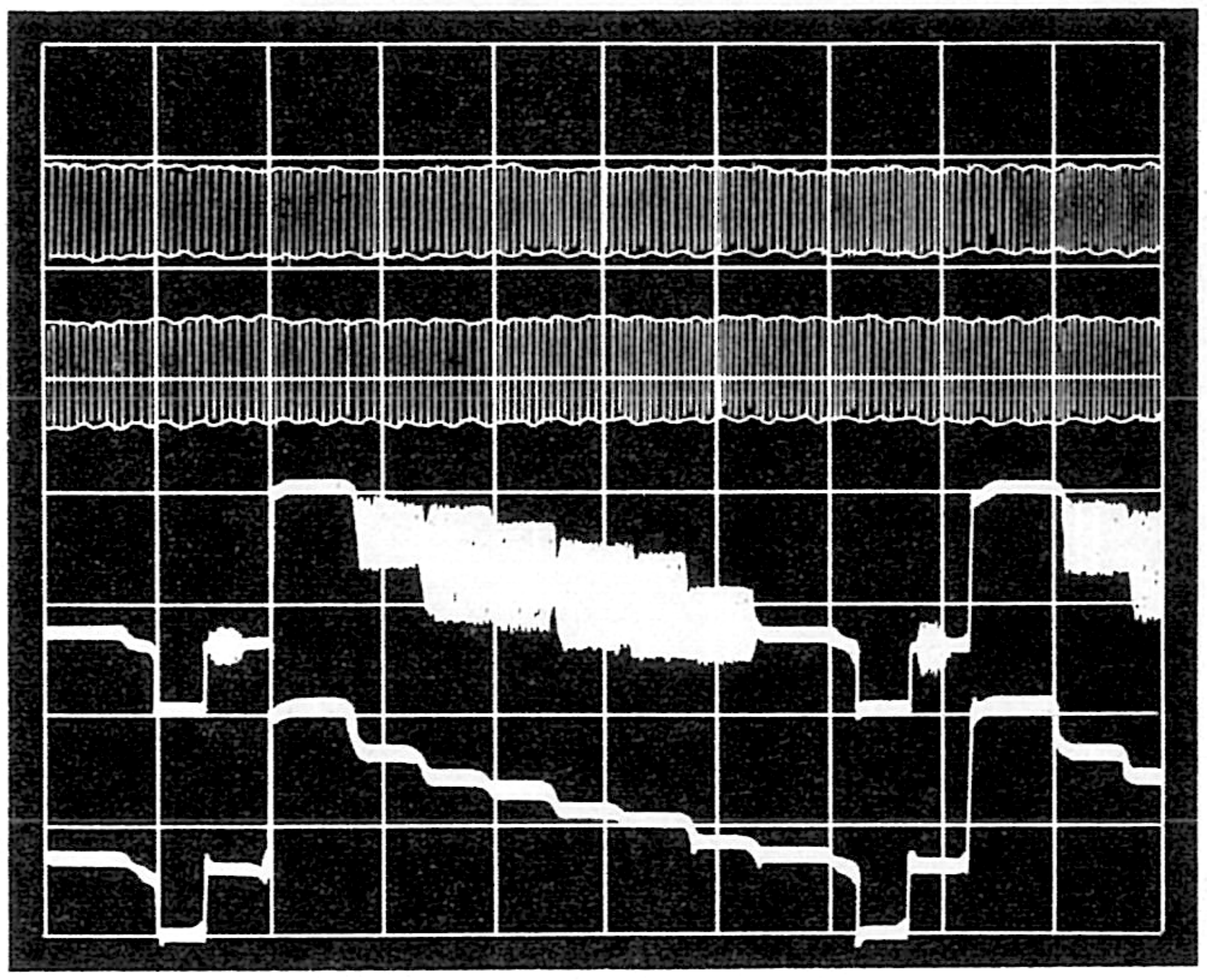
SPDL Ass'y

TP1 5V/DIV 5ms/DIV
(REF. Sync.)

TP3 10V/DIV 5ms/DIV
(Frame Sawtooth)

TP4 10V/DIV 5ms/DIV
(Playback Sampling Pulse)

TP5 OVDC 5ms/DIV
(Frame Error)



VDEM Ass'y

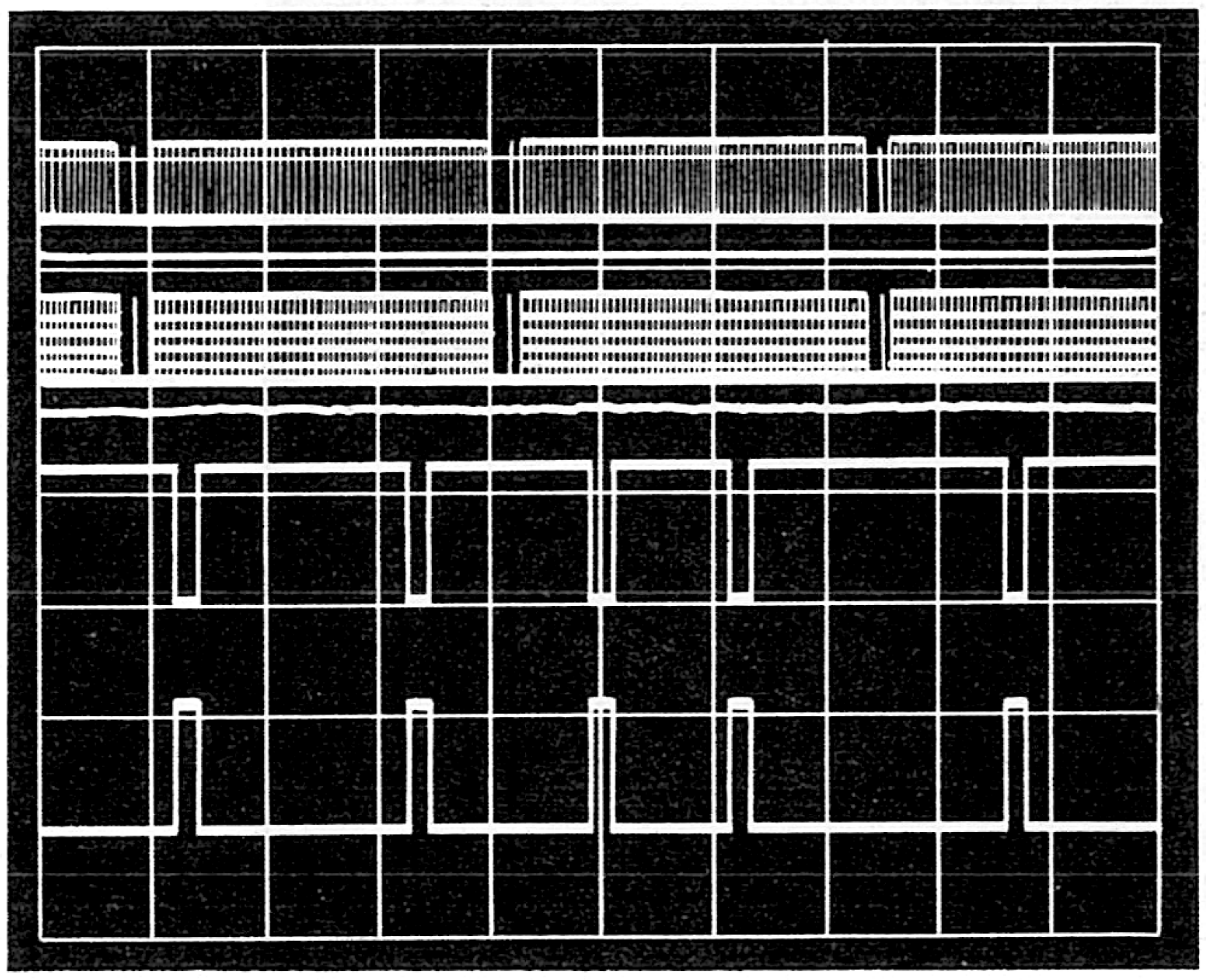
TP1 (Input FM)

TP9 (FM for Delayed Video)

1V/DIV 10μs/DIV

TP7 (Main Line Video)

TP8 (1H Delayed Video)



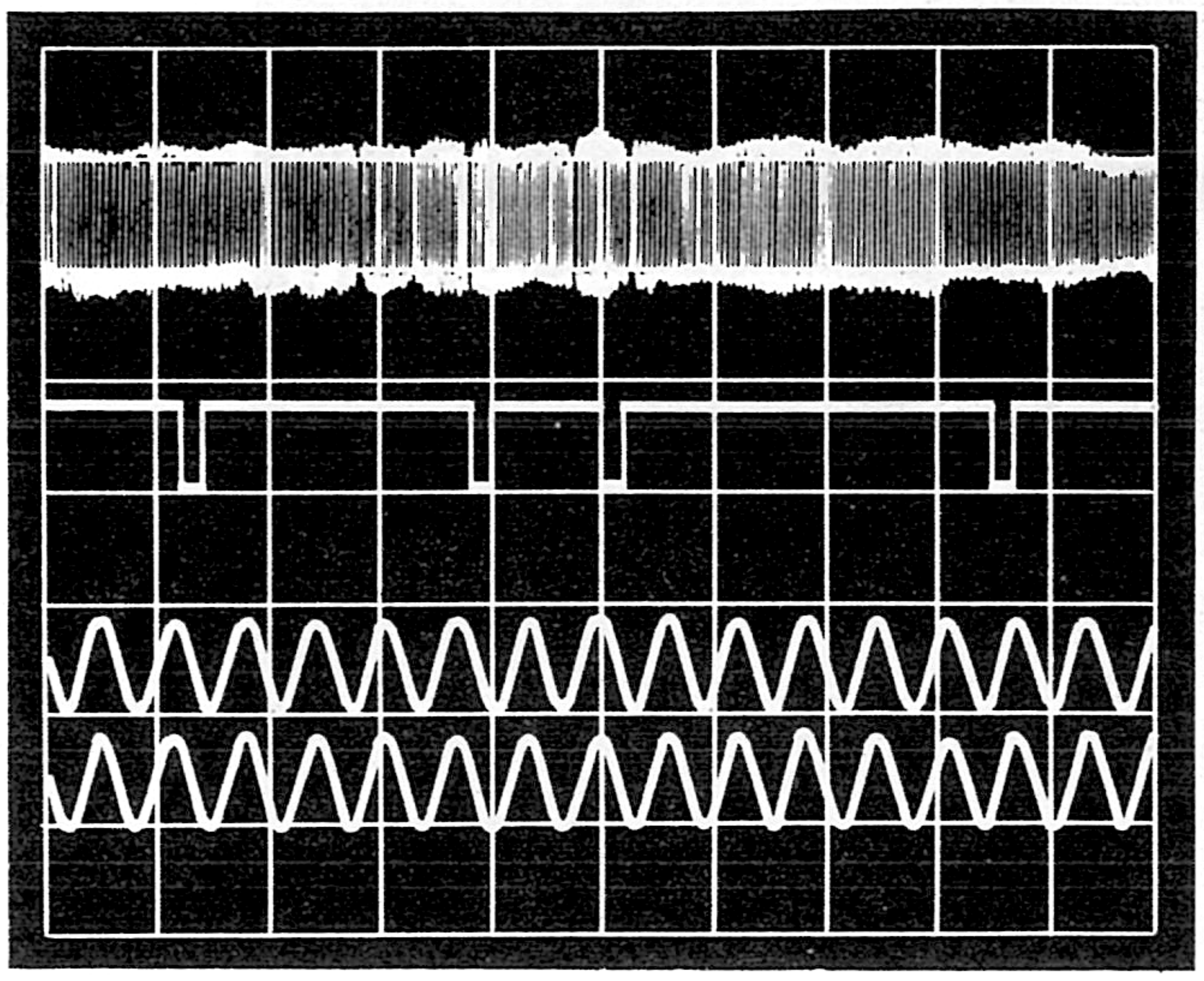
VDEM Ass'y

TP7 2V/DIV 5ms/DIV
(Main Line Video)

TP8 2V/DIV 5ms/DIV
(1H Delayed Video)

TP11 10V/DIV 5ms/DIV
(DOS)

TP12 10V/DIV 5ms/DIV
($\overline{\text{DOS}}$)



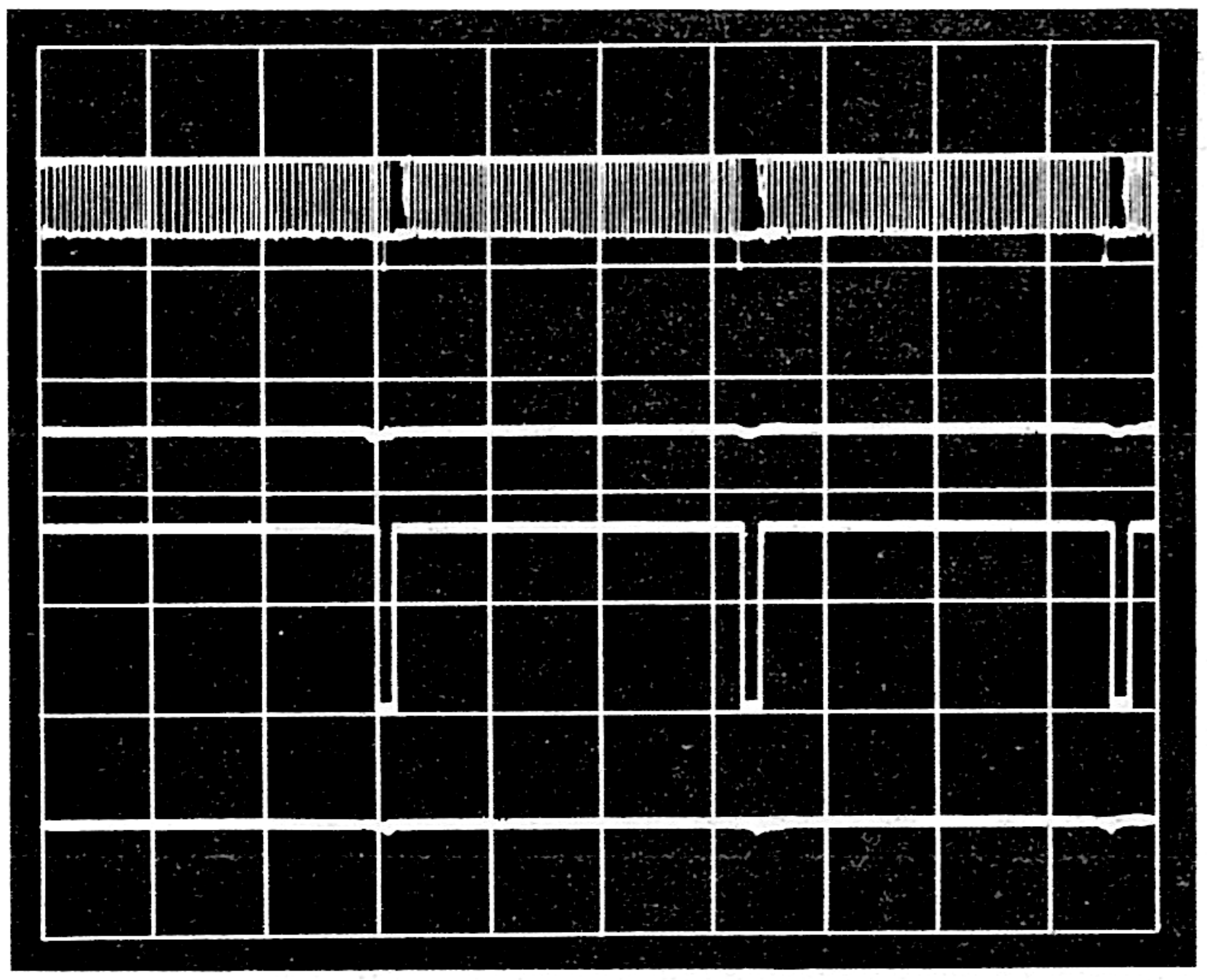
AUDB Ass'y

TP1 500mV/DIV 500μs/DIV
(Input FM)

TP2 5V/DIV 500μs/DIV
(AUDIO DOS)

TP3 1V/DIV 500μs/DIV
(AUDIO CH1)

TP4 1V/DIV 500μs/DIV
(AUDIO CH2)



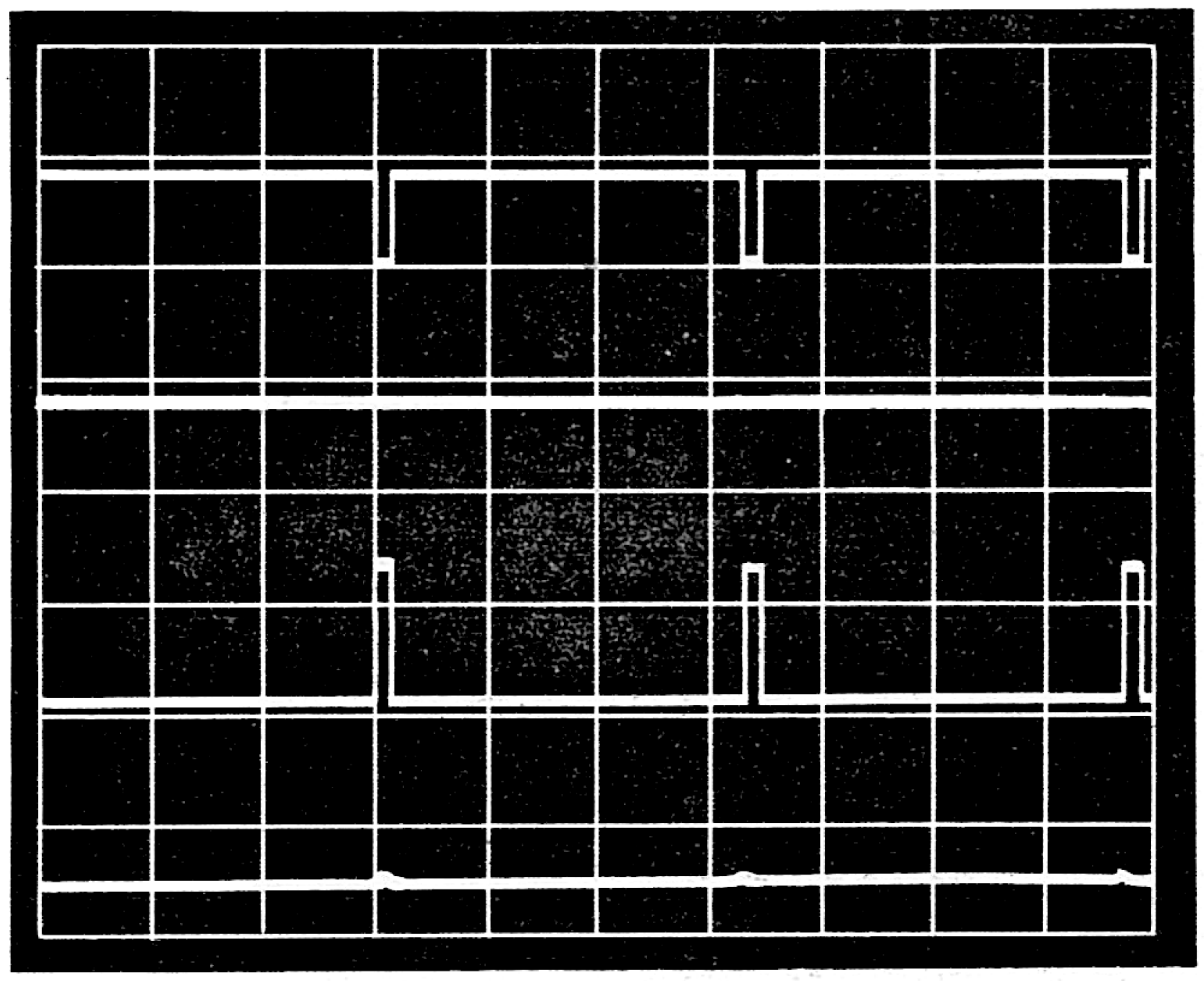
D & CR Ass'y

TP1 1V/DIV 5ms/DIV
(Input Video)

TP2 +0.6V DC 5ms/DIV
Sync. Sep. Threshold

TP3 1V/DIV 5ms/DIV
(V Sync.)

TP4 +1V DC 5ms/DIV
(V Sync:)



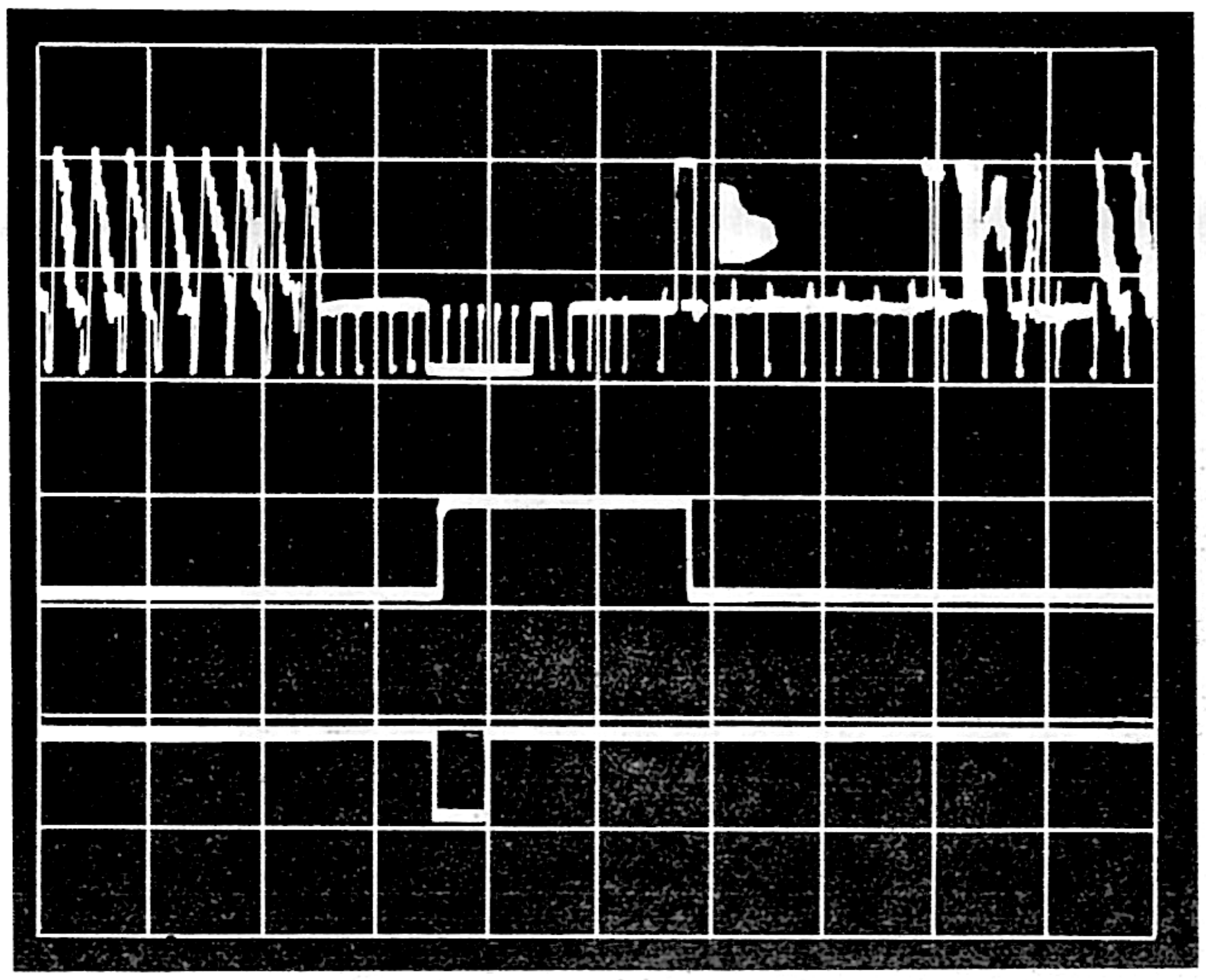
D & CR Ass'y

TP5 2V/DIV 5ms/DIV
FRAME NO. DATA

TP6 +0.8V DC 5ms/DIV
TP5 Threshold Level

TP7 1V/DIV 5ms/DIV
FRAME NO. DATA

TP8 +0.5V DC 5ms/DIV
TP7 Threshold Level

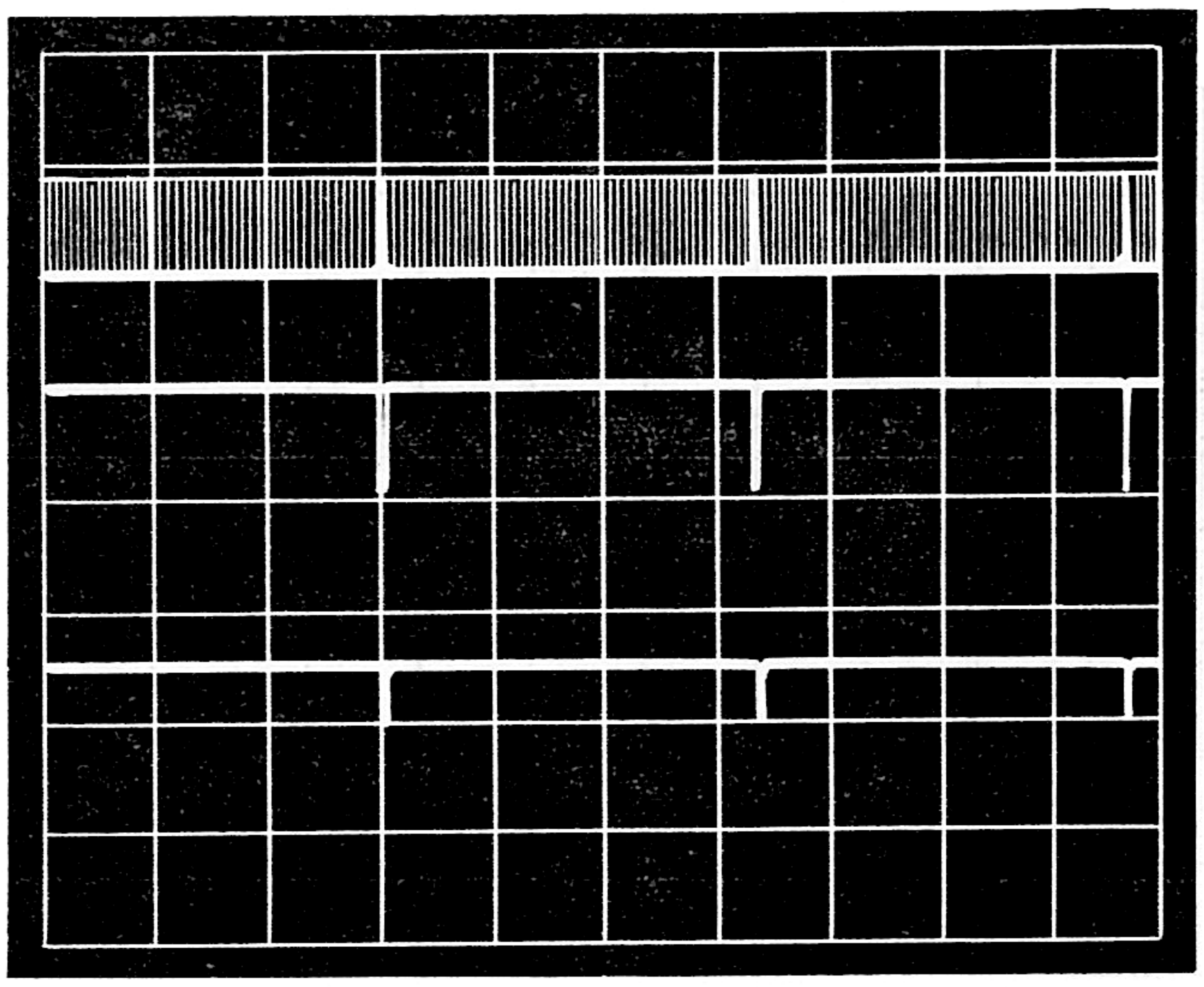


D & CR Ass'y

TP1 0.5mV/DIV 200μs/DIV
(Input Video)

TP9 5V/DIV 200μs/DIV
(Valid Data)

TP10 5V/DIV 200μs/DIV
(V Sync.)

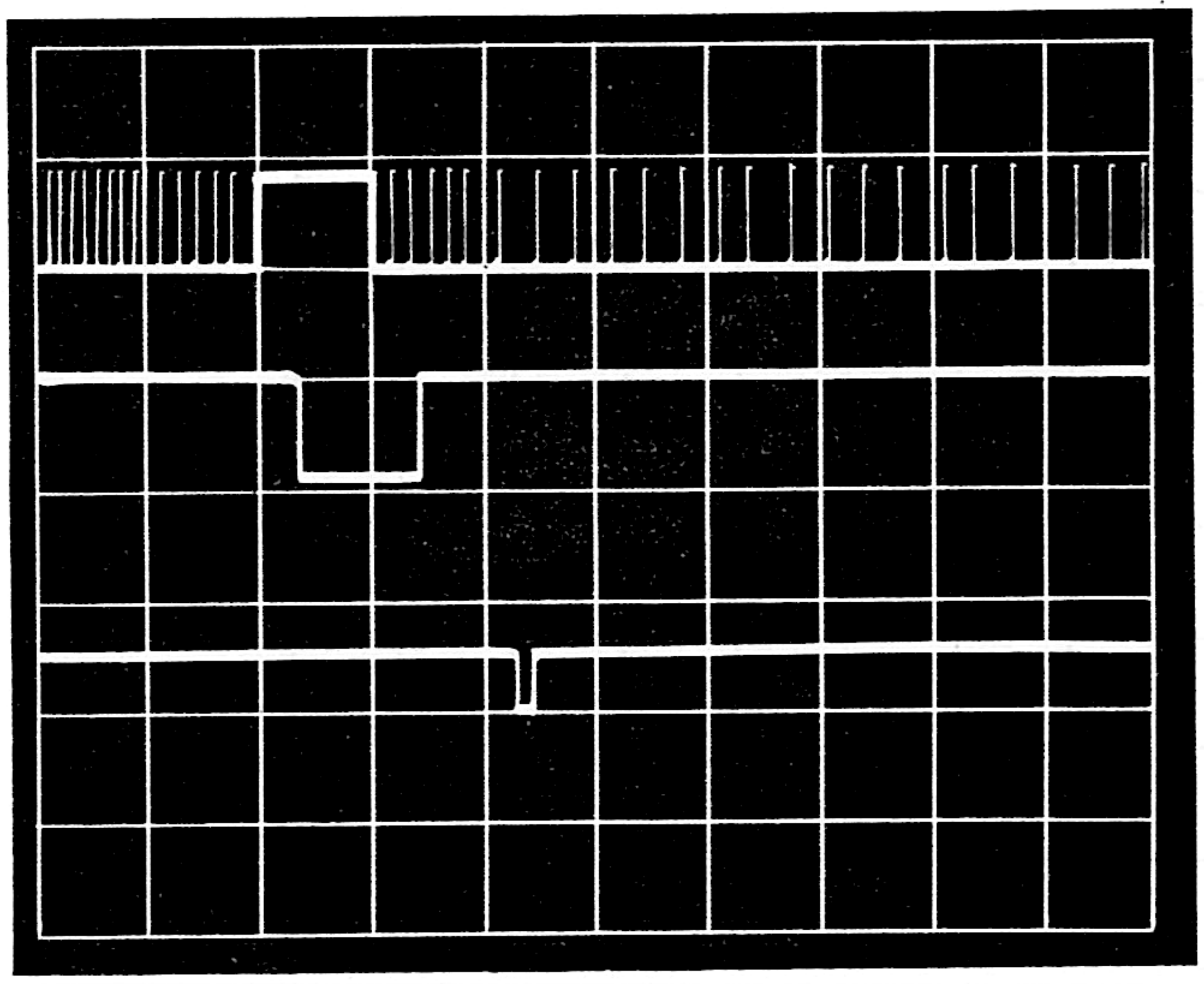


STPM Ass'y
(V Rate)

TP1 5V/DIV 5ms/DIV
(Sync. Sep.)

TP2 5V/DIV 5ms/DIV
(V Sync.)

TP3 5V/DIV 5ms/DIV
(White Flag)



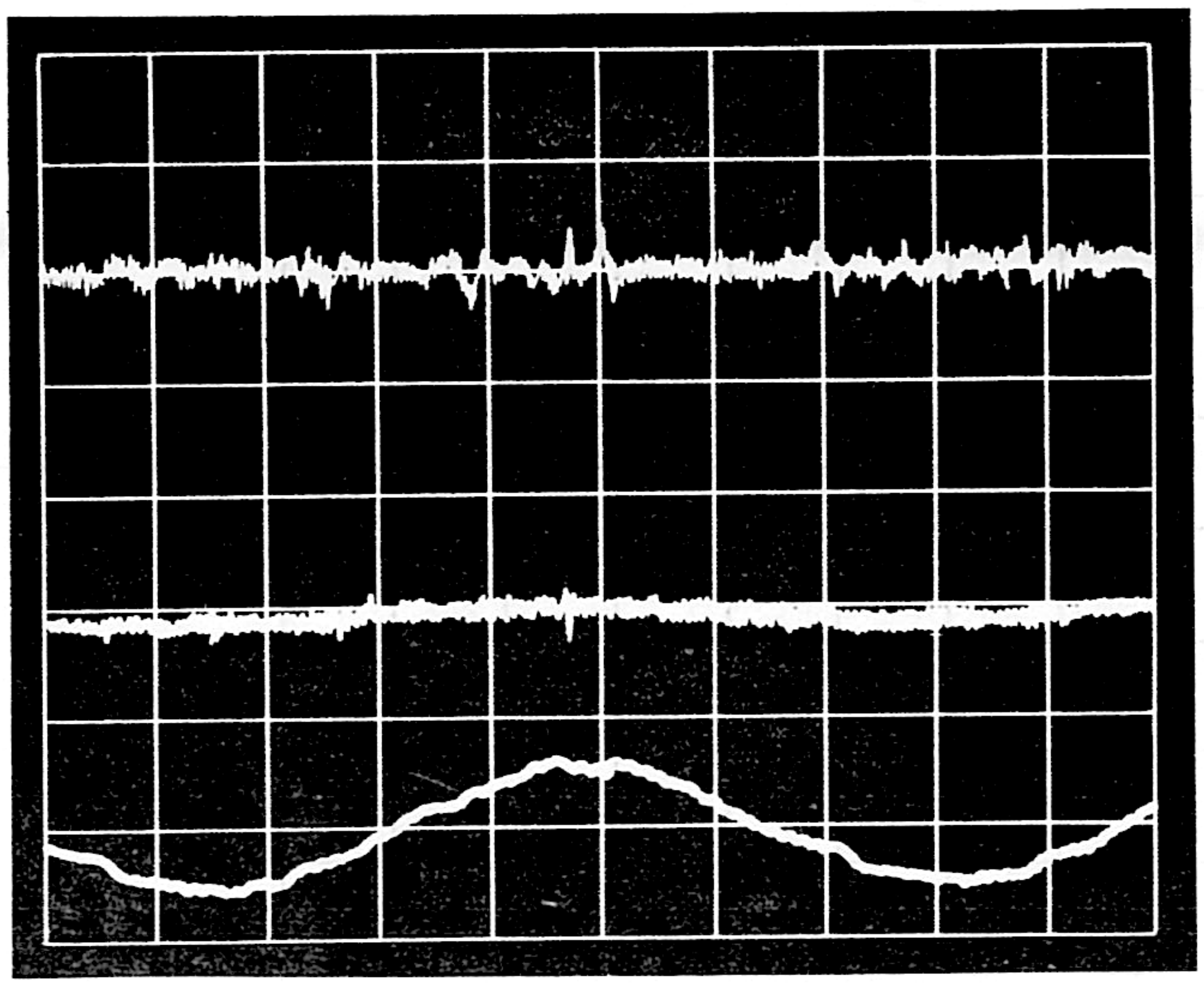
STPM Ass'y
(H Rate)

TP1 (Sync. Sep.)

TP2 (V Sync.)

5V/DIV 5ms/DIV

TP3 (White Flag)



CARG Ass'y

TRKG TP1 5V/DIV 5ms/DIV
(Tracking Error)

MIRROR TERMINAL 5V/DIV 5ms/DIV

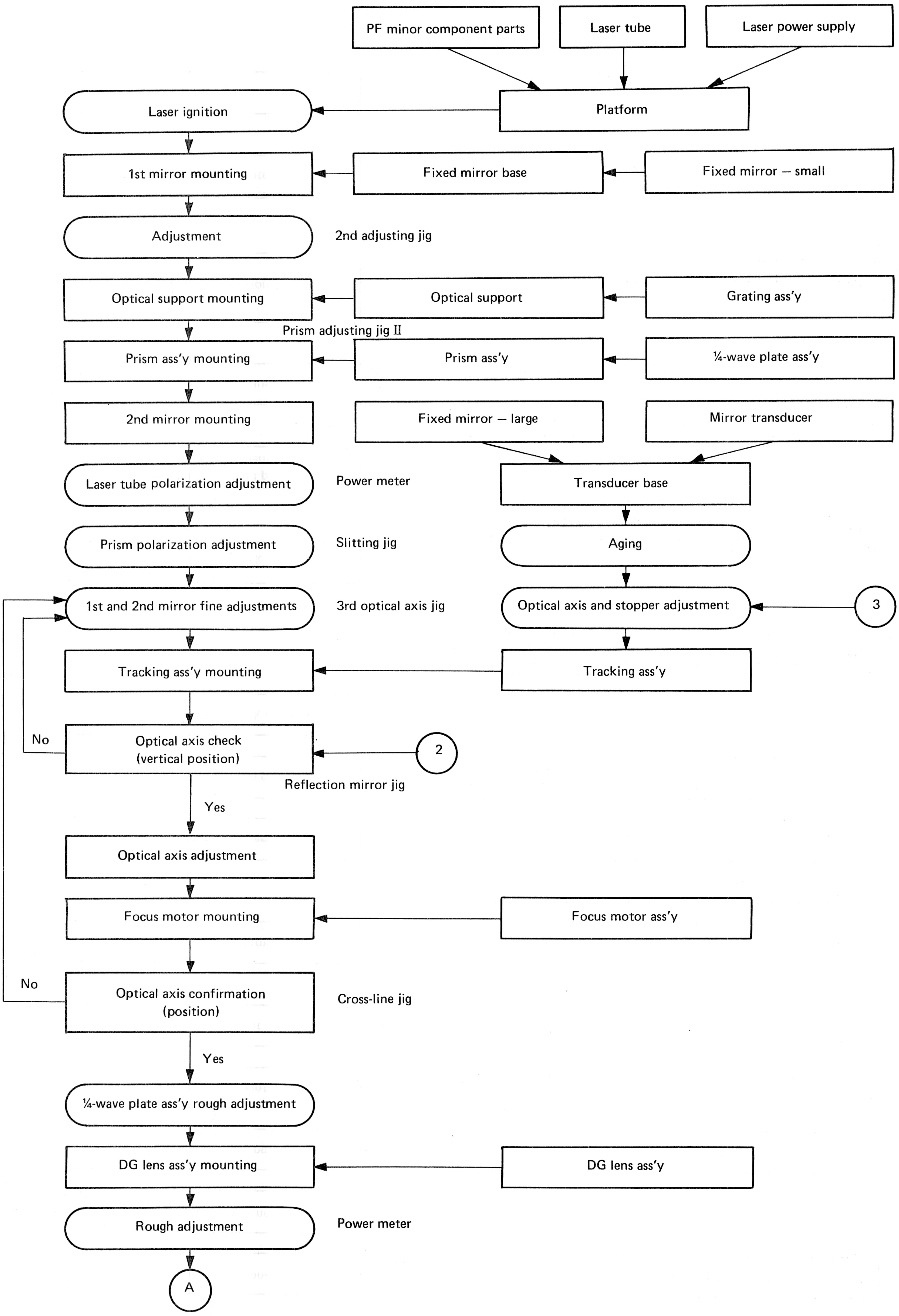
CARG TP1 500mV/DIV 5ms/DIV
(Tacho)

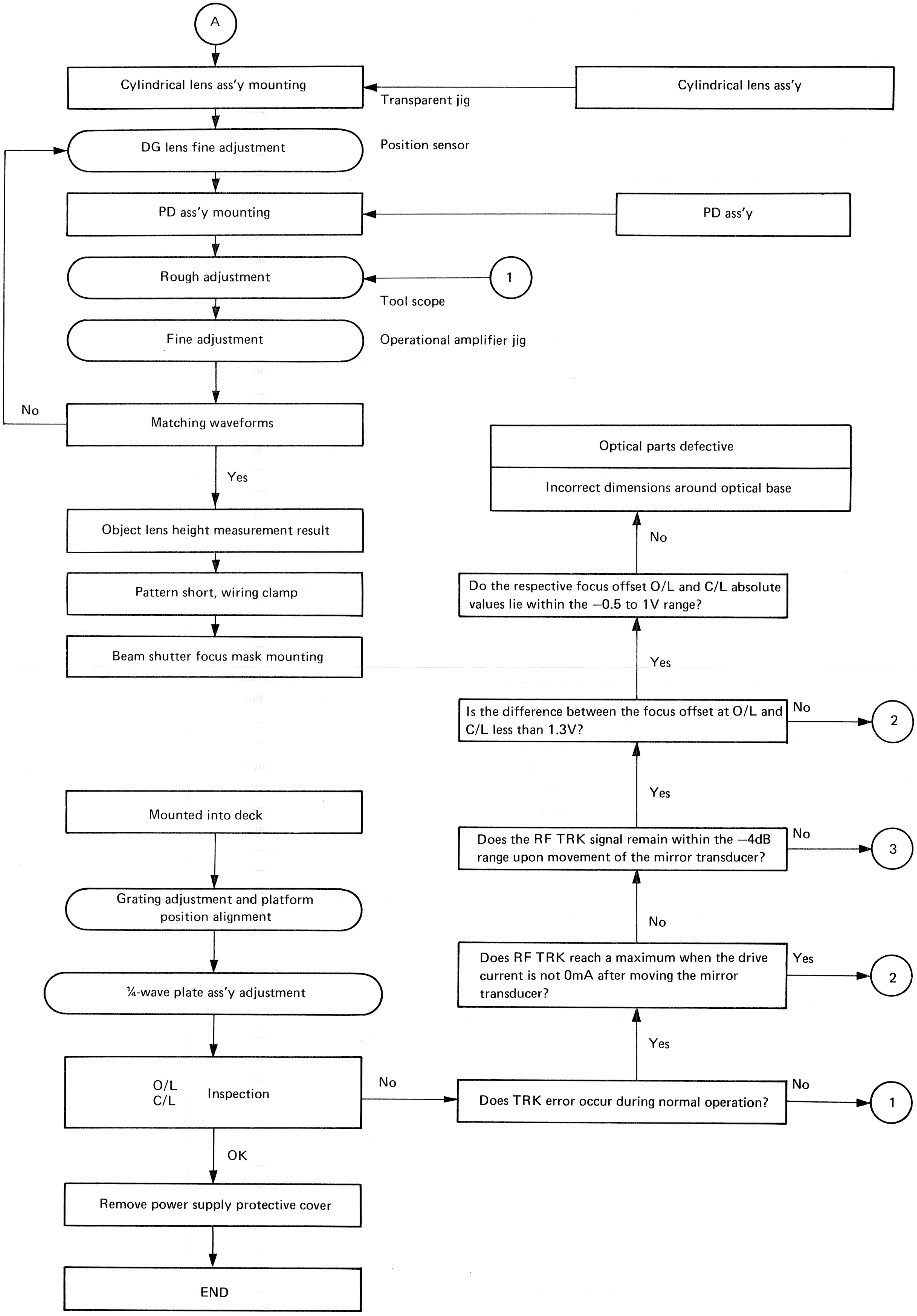
MEMO

13. PLATFORM ASSEMBLY AND ADJUSTMENT PROCEDURE

13.1 ADJUSTMENT PROCEDURE FLOW CHART

1. Adjustment Procedures Flowchart




A
Cylindrical lens ass'y mounting
Transparent jig
Cylindrical lens ass'y
DG lens fine adjustment
Position sensor
PD ass'y mounting
PD ass'y
Rough adjustment
1
Tool scope
Fine adjustment
Operational amplifier jig
No
Matching waveforms
Yes
Object lens height measurement result
Pattern short, wiring clamp
Beam shutter focus mask mounting
Optical parts defective
Incorrect dimensions around optical base
No
Do the respective focus offset O/L and C/L absolute values lie within the –0.5 to 1V range?
Yes
Is the difference between the focus offset at O/L and C/L less than 1.3V?
No
2
Yes
Mounted into deck
Does the RF TRK signal remain within the –4dB range upon movement of the mirror transducer?
No
3
Grating adjustment and platform position alignment
No
Does RF TRK reach a maximum when the drive current is not 0mA after moving the mirror transducer?
Yes
2
¼-wave plate ass'y adjustment
Yes
O/L
C/L
Inspection
No
Does TRK error occur during normal operation?
No
1
OK
Remove power supply protective cover
END

13.2 PREPARATORY PROCEDURES

13.2.1 Mount the DG lens, 1/4-wave plate, prism, grating and cylindrical lens assemblies, plus the large and small fixed mirrors according to the mounting specifications.

13.2.2 Preparation of tube plate ass'y

Mount the tube cushion as shown in the diagram up to about 2mm from the seat.

a. Preparation of PF cover ass'y

Mount the large cover packing around 3 sides flush with the sides of the PF cover as shown in the diagram. Then insert the small cover packing underneath the large cover packing, taking care to leave no gap between the two. Also check that the packing does not protrude beyond the side of the PF cover. Any uneveness in the packing should not exceed ±2mm.

b. Labeled power supply cover.

Paste the voltage warning label in the center of the cover (the ↔ mark may be positioned at either end).

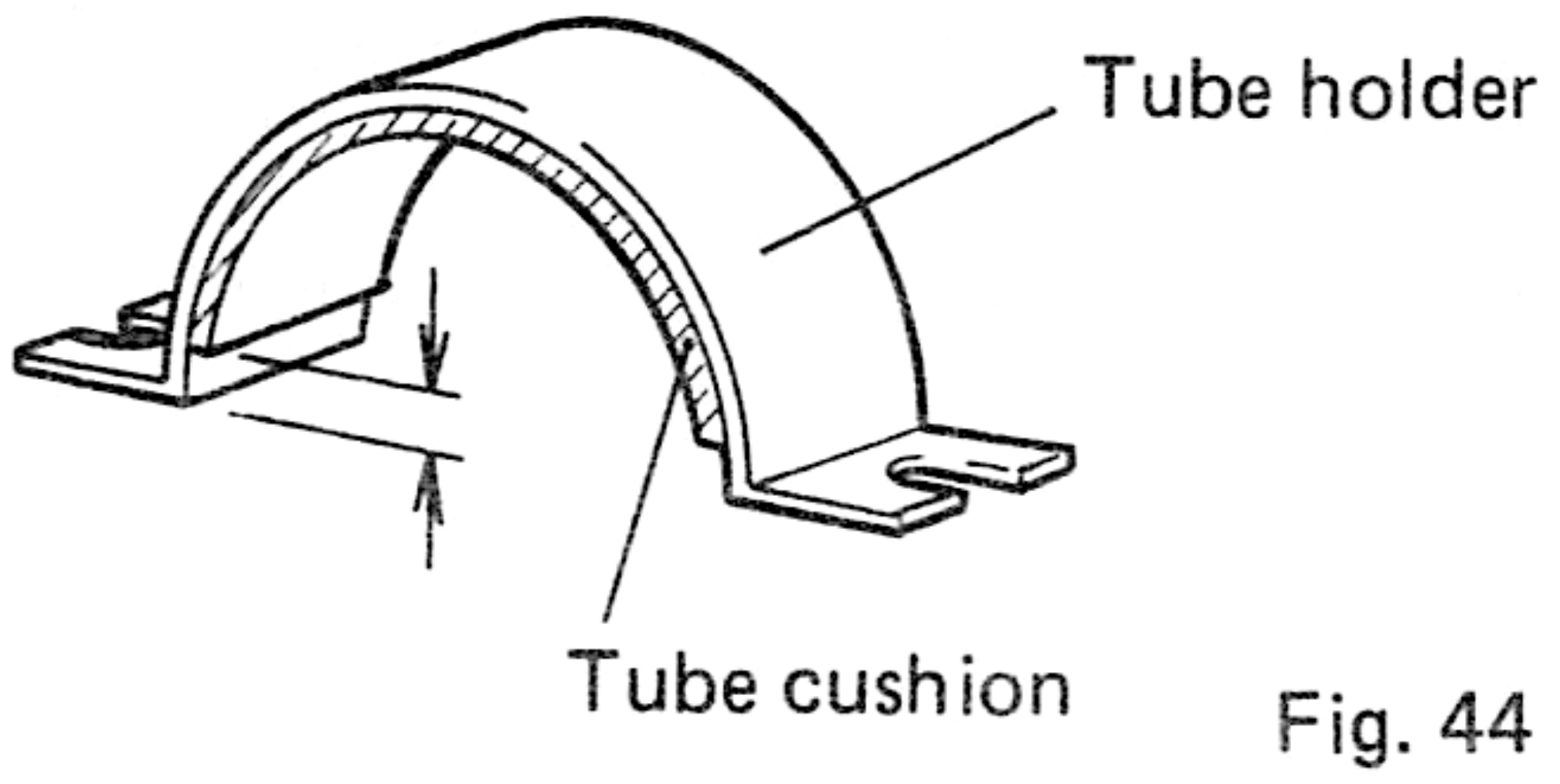


Fig. 44

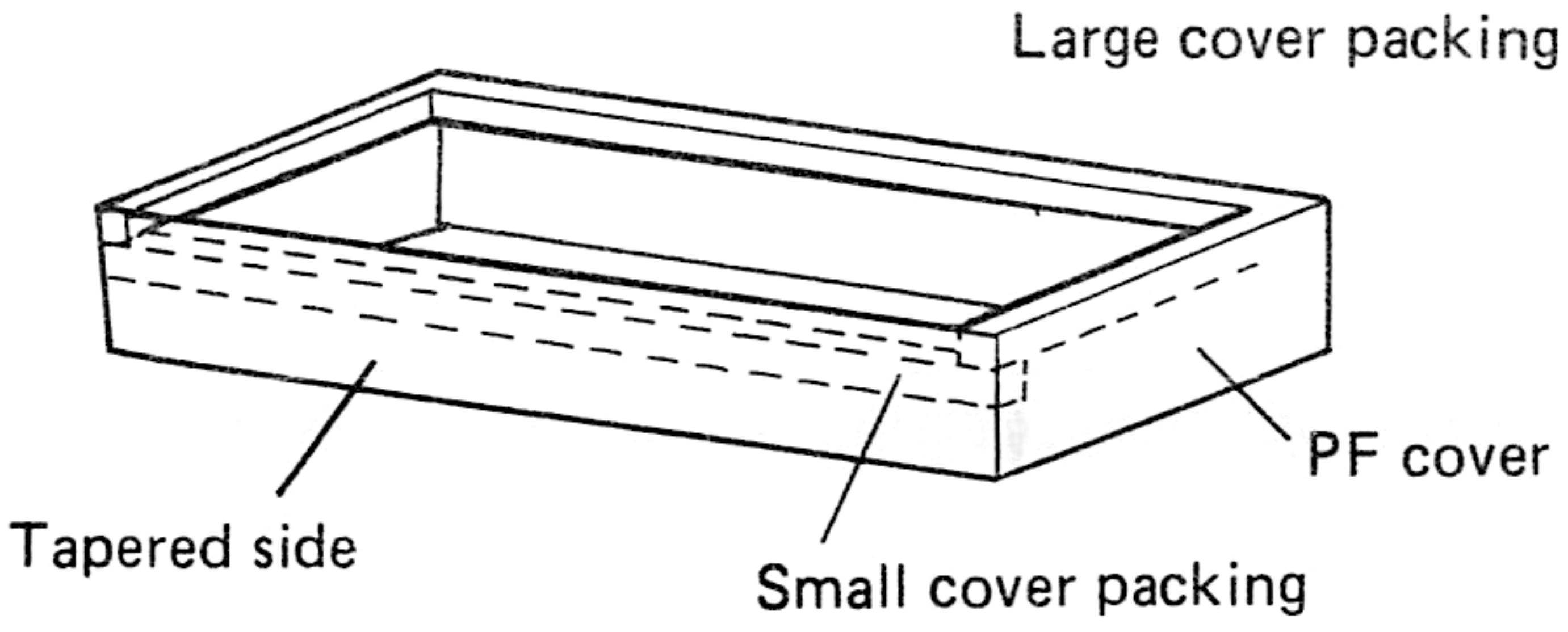


Fig. 45

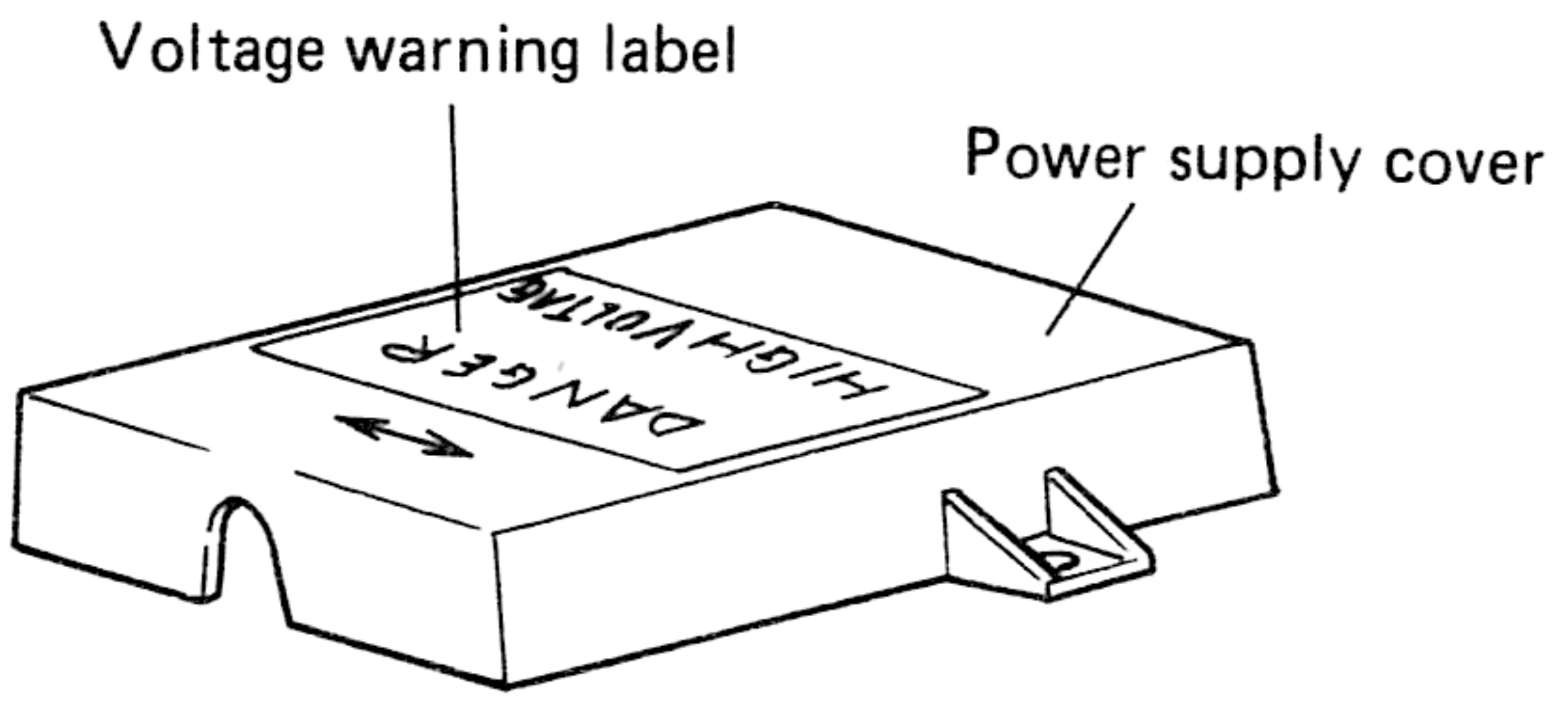


Fig. 45

13.3 PRELIMINARY PROCEDURES

13.3.1 Mount the 1/4-wave plate ass'y in the prism ass'y.

13-3-2 Mount the small fixed mirror in the fixed mirror base.

13.3.3 Mount the grating, PD nut and DG nut assemblies in the optical support.

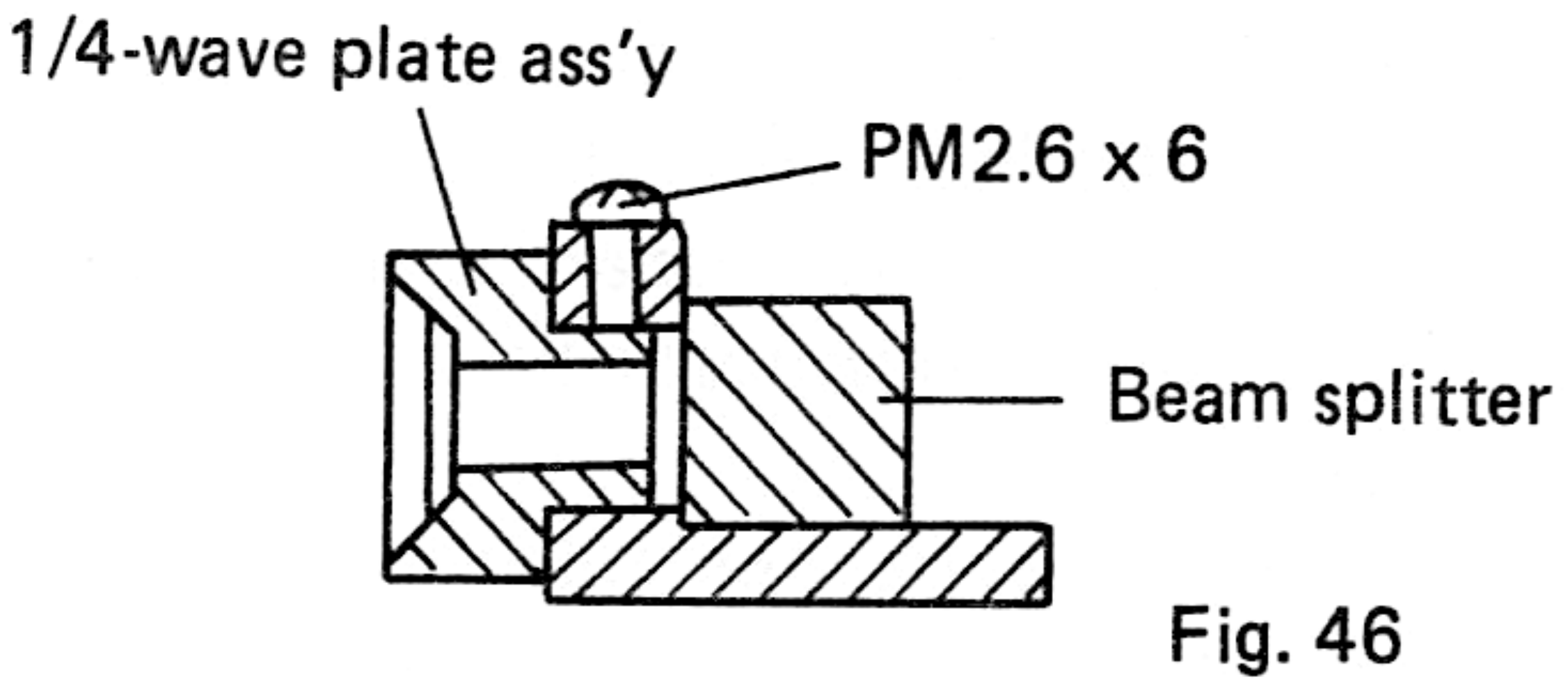


Fig. 46

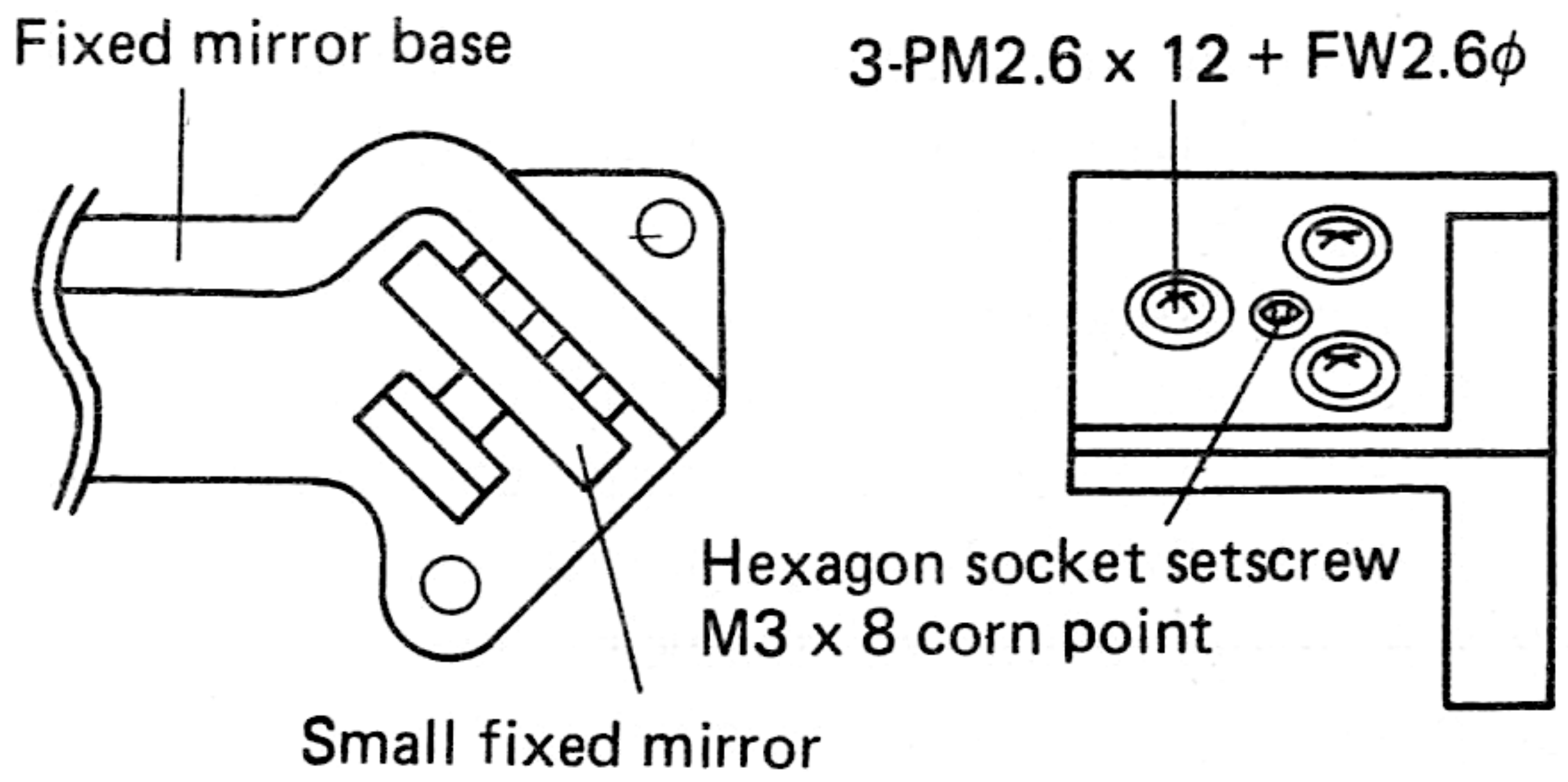


Fig. 46

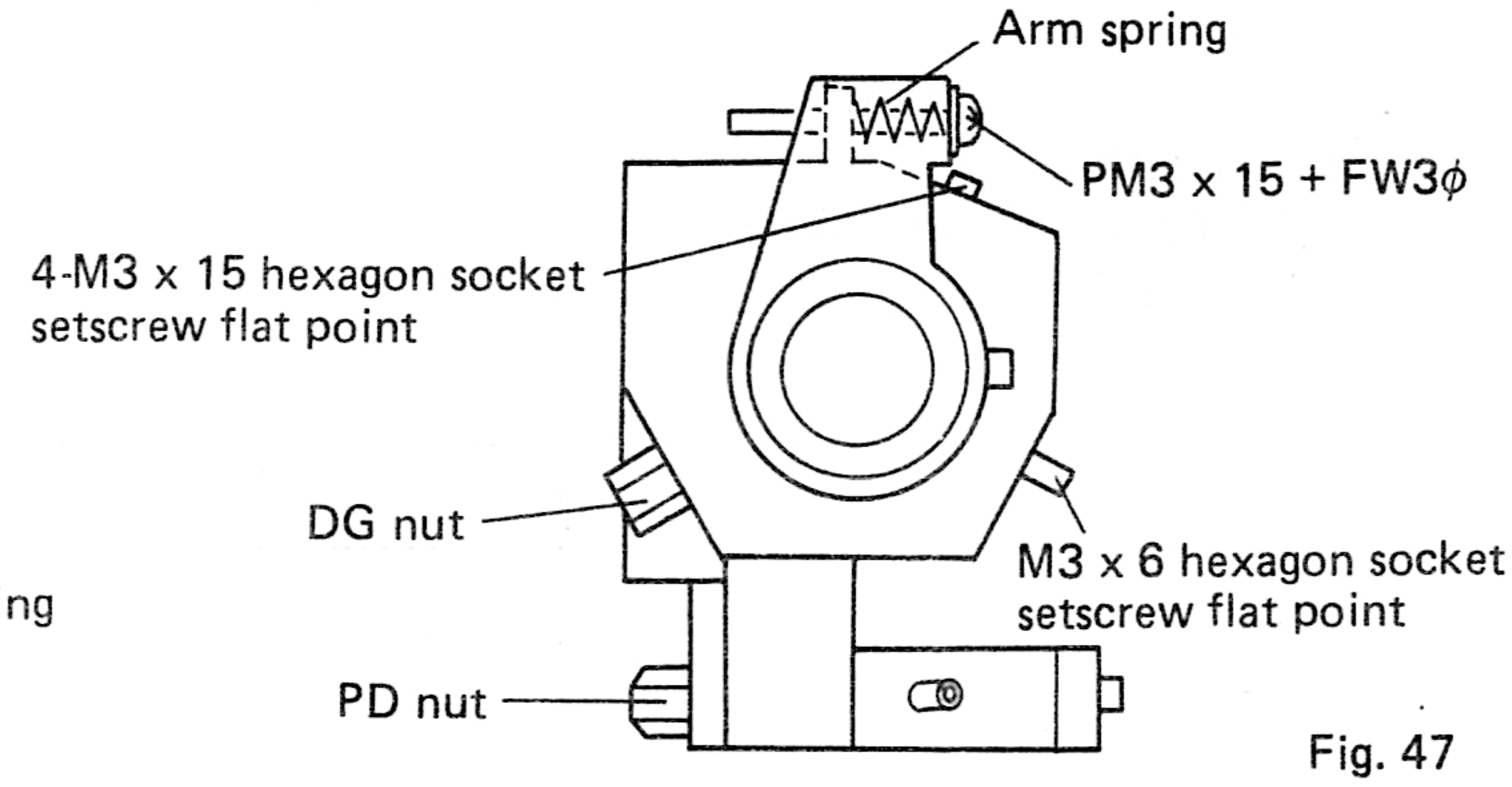

Arm spring
PM3 x 15 + FW3ϕ
4-M3 x 15 hexagon socket setscrew flat point
DG nut
M3 x 6 hexagon socket setscrew flat point
PD nut

Fig. 47

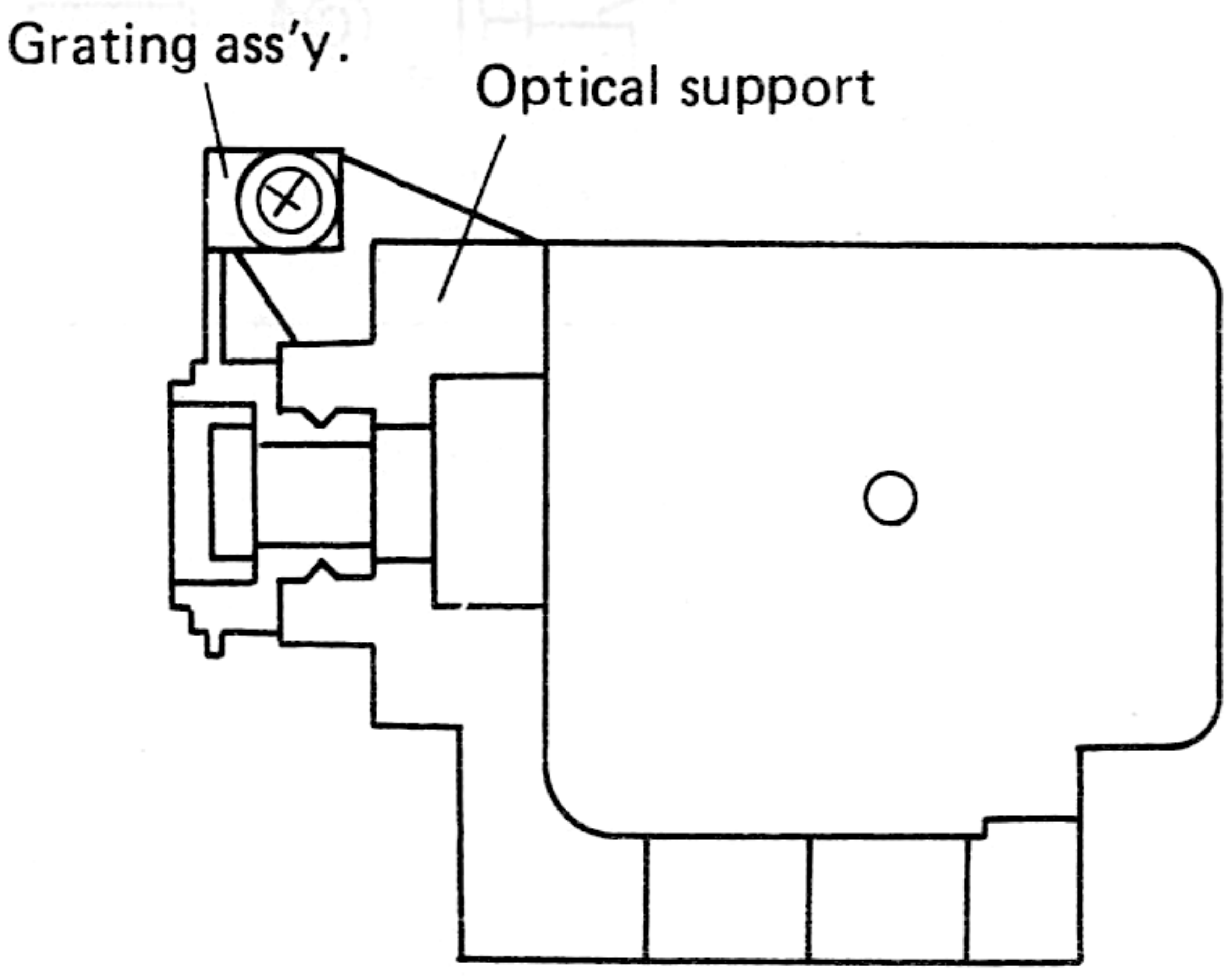


Fig. 48

13.3.4 Mount the laser tube and minor component parts, plus the power supply system into the platform.

a. Minor component parts

Mount the cord clamper, 2-pin ground terminal and shutter mask into the platform according to the general ass'y diagram.

b. Laser tube and power supply

- Place the laser tube on the platform with the high voltage terminal in the upper position, and secure temporarily with the tube holder ass'y.
- Insert the barrier underneath, and fix the power supply to the platform.
- Connect the ballast resistor to the high voltage cord, and bind the insulation and UL vinyl tubing with binder. Secure each cord to the platform as shown in the general ass'y diagram.

c. Place the power protection cover over the power supply (in order to avoid possible electric shock during operation).

13.3.5 Preparation of tracking ass'y.

a. Place the transducer base in the tracking ass'y adjustment jig, rotate clockwise, and then push in the direction of the arrow and tighten the screws.

b. Mount the large fixed mirror, and adjust angle and position by the rear screw to ensure that the reflected beam passes through the (A) and (B) pin holes.

c. Mount the mirror transducer ass'y into the transducer base, and adjust both front/rear and left/right, plus the flap fine adjustment to ensure passage through pin holes (C) and (D). The flap fine adjustment screw is to be screw-locked with Screw-Tight 300-UB.

d. Pass an AC current (line frequency below 20Hz) through the mirror transducer ass'y in order to drive the mirror. Adjust the left and right position adjustment screws to restrict the degree of deflection to within the deflection limit lines.

e. Remove the tracking ass'y from the jig, and subject it to the aging process (200mA p-p pink noise applied for at least 24 hours).

f. Then remount the tracking ass'y back into the adjustment jig, and adjust the optical axis as described below.

Displacement in X direction:
correct with 3rd mirror.
Displacement in Y direction:
correct with mirror transducer.

NOTE:
Do not try to make corrections with the mirror transducer flap.

g. Fine adjust the deflection limits (initially adjusted in step (4) above), and then screw-lock all adjustment screws with Screw-Tight 300-UB.

h. Remove from the tracking ass'y adjustment jig.

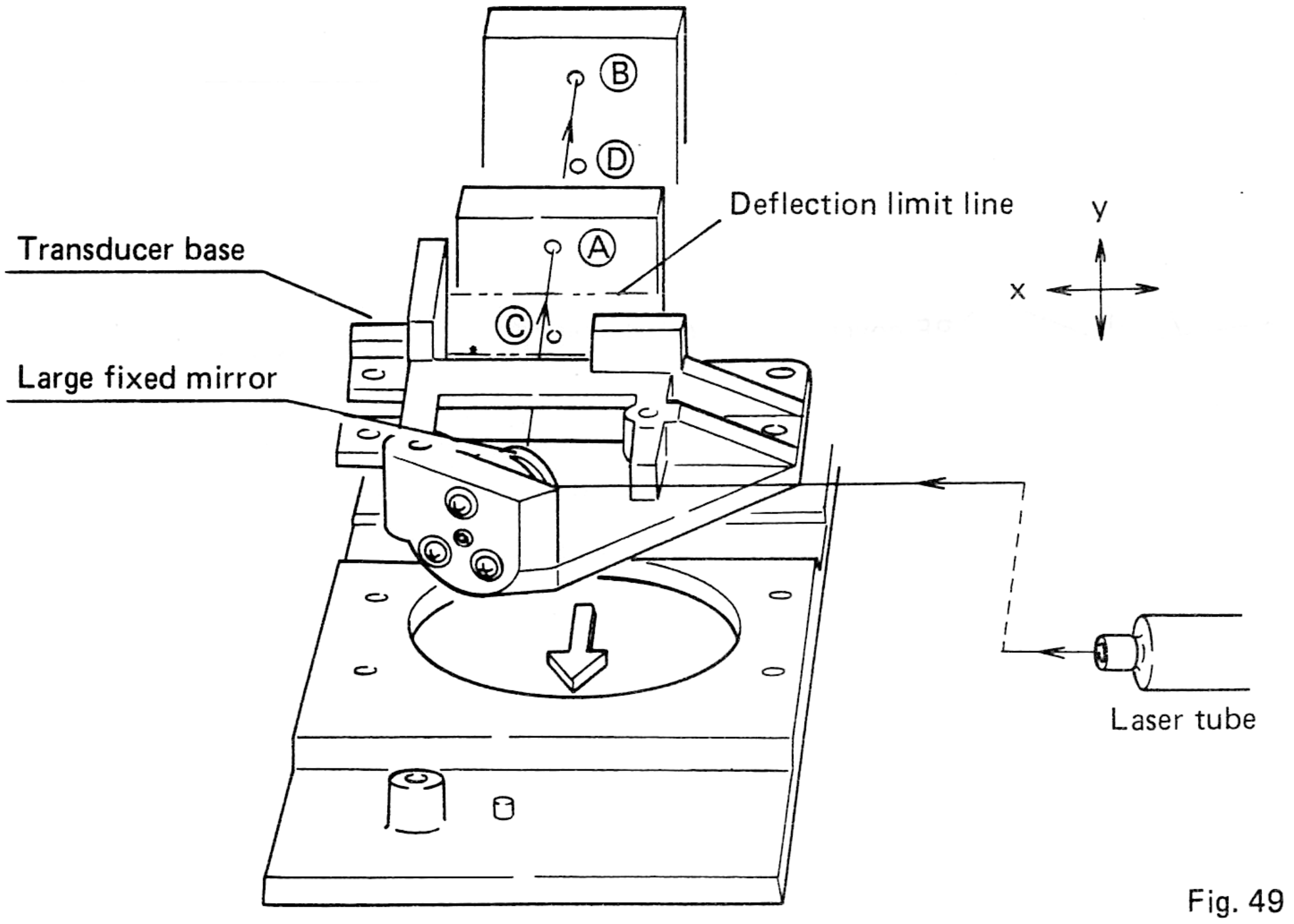


Fig. 49

13.4 MOUNTING AND ADJUSTMENT OF ALL PARTS ONTO THE PLATFORM

13.4.1 Connect the laser power supply to the jig transformer, and switch on.

13.4.2 1st mirror adjustment and fixing.

1. Mount the support ass'y onto the platform.
2. Adjust the 1st mirror with the 2nd adjustment jig so that the beam passes through the pin holes. Then remove the jig.

13.4.3 Mount the optical support and prism ass'y

Align and fix the optical support position with prism adjustment jig II, and temporarily fix the prism ass'y.

NOTE:
Turn the optical support around so that the A side is up against prism ass'y jig II.

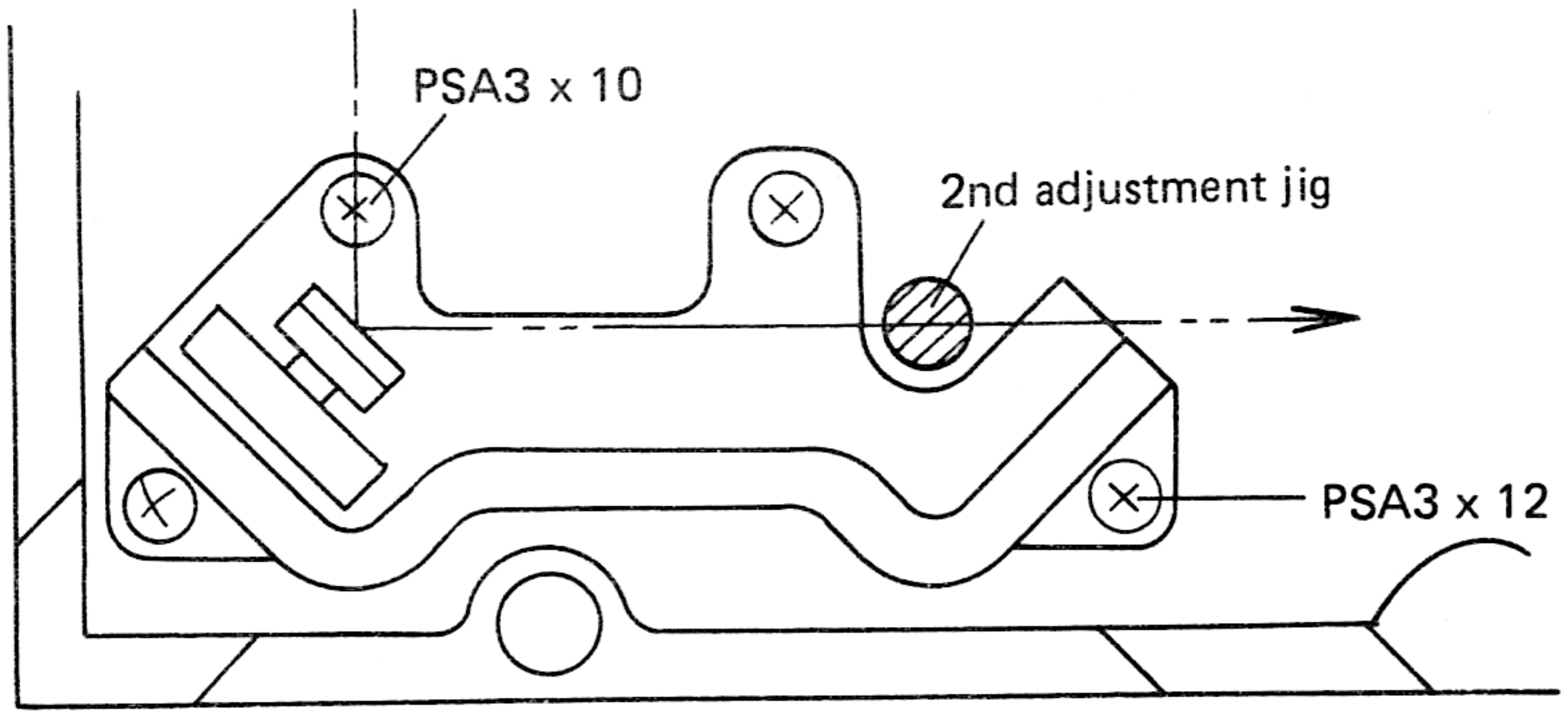


Fig. 50

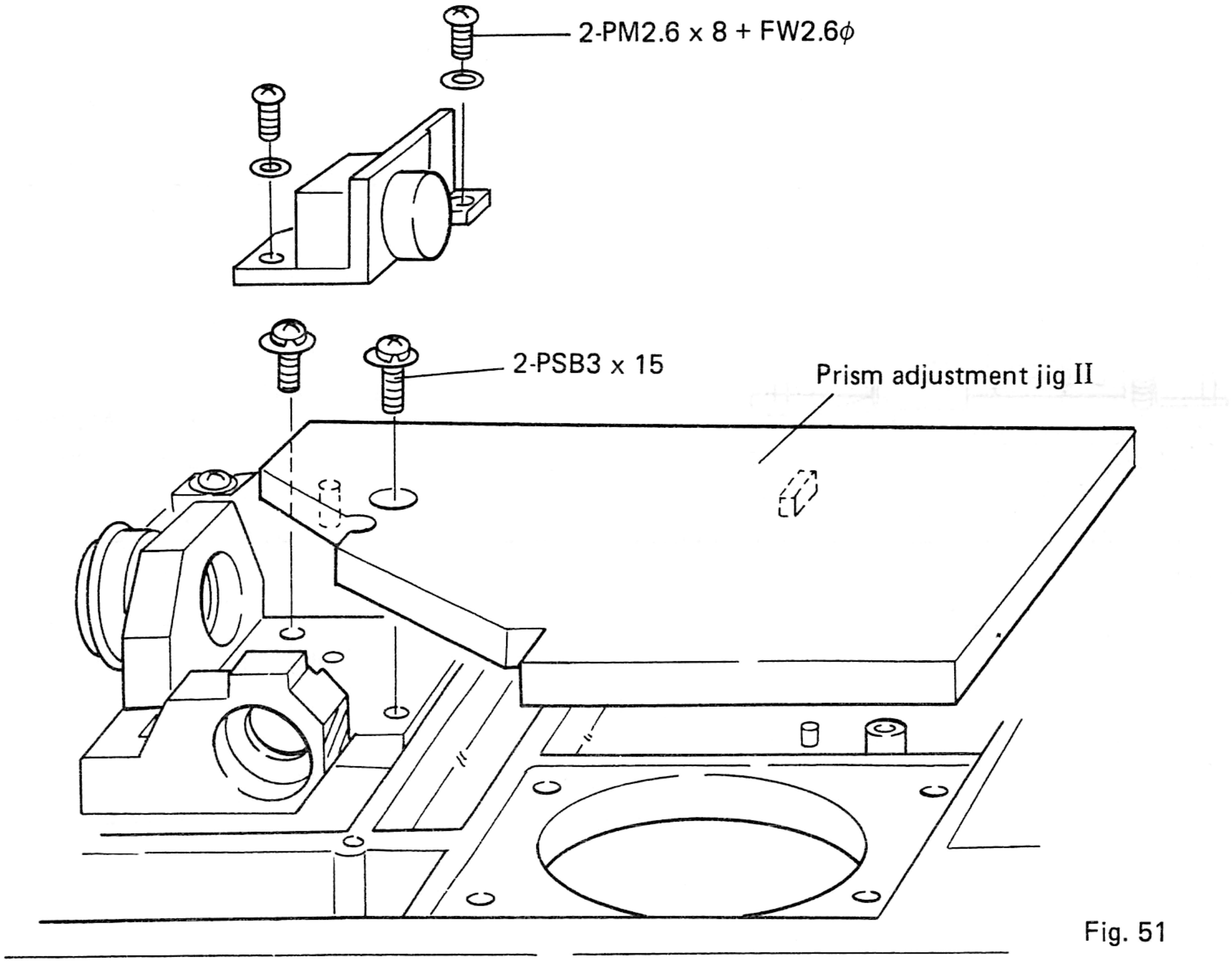


Fig. 51

13.4.4 Mount the 2nd mirror

Mount the small fixed mirror in the 2nd mirror position, and adjust so that the beam passes roughly through the center of the beam splitter prism.

13.4.5 Prism Ass'y adjustment and laser beam poralization adjustments.

a. Rotate the laser tube and secure at the position where the amount of light reflected at right angles to the optical axis by the prism is minimal in the direction opposite to the detector (adjust to obtain minimum reading in the power meter).
b. Observe the light reflected from the surface of the prism with the slitting jig, and rotate the prism so that the beam passes through the slit.

13.4.6 Fine adjustment of 1st and 2nd mirrors.

Use the 3rd optical axis jig to adjust the 1st and 2nd mirrors so that the beam passes through the 2 pin holes. Then lock the screws with Screw-Tight 300-UB.

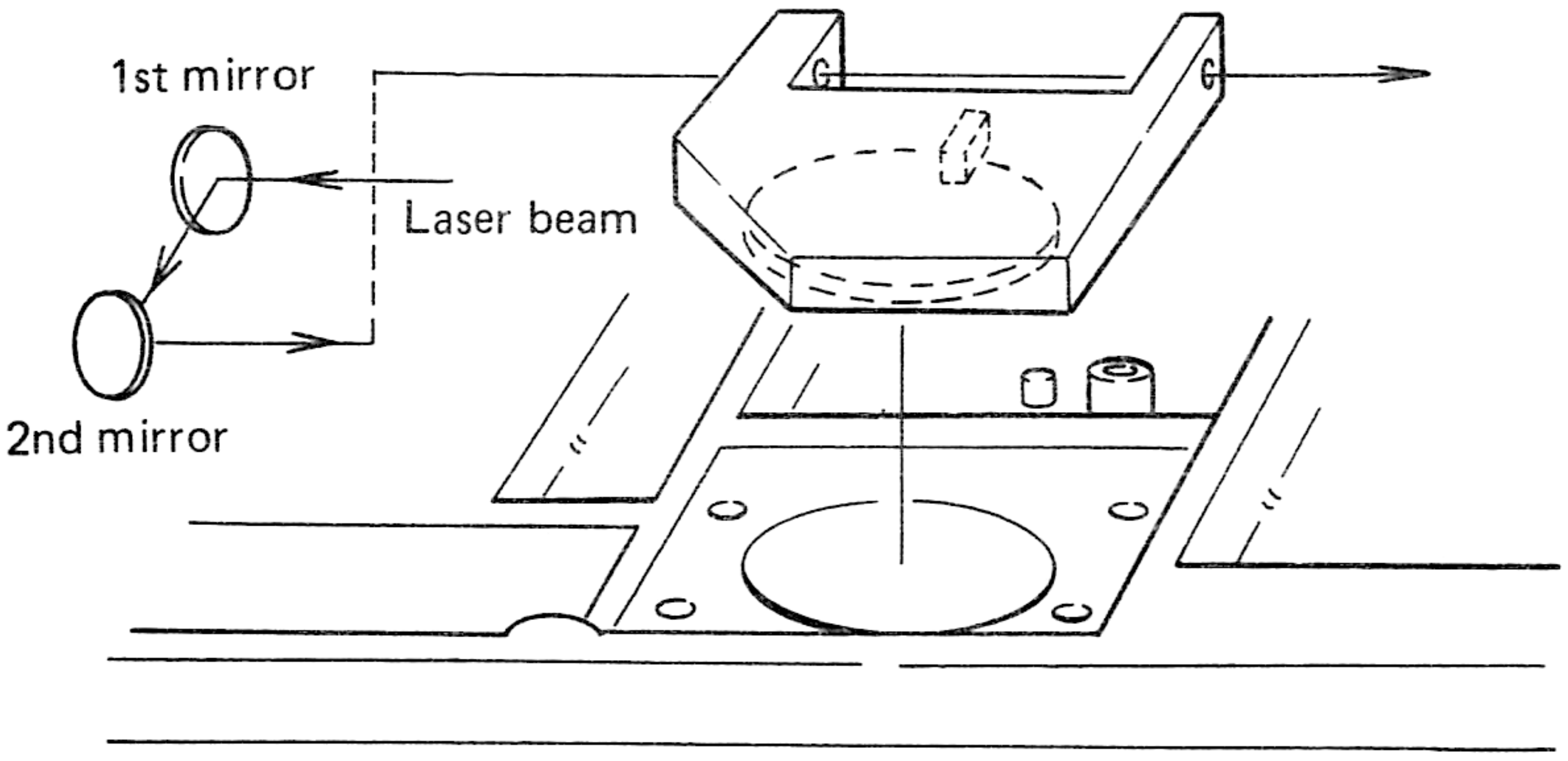


Fig. 52

13.4.7 Mount the tracking ass'y

Insert the tracking ass'y into the focus motor hole, rotate clockwise, push forward, and tighten the screws.

NOTE:
The positions of the prism adjustment jig and 3rd optical axis jig are determined in the same way.

13.4.8 Optical axis check

Insert the reflection mirror jig, and check the position and level accuracy of the beam at the focus motor position.

1. More than half of the beam reflected by the reflection mirror jig should overlap the forward beam at the prism stage (level accuracy).
2. The beam should pass over the marking line on the surface of the reflection mirror jig (position accuracy).

If the above conditions are not satisfied, the adjustments described under step 13-4-6 above should be repeated.

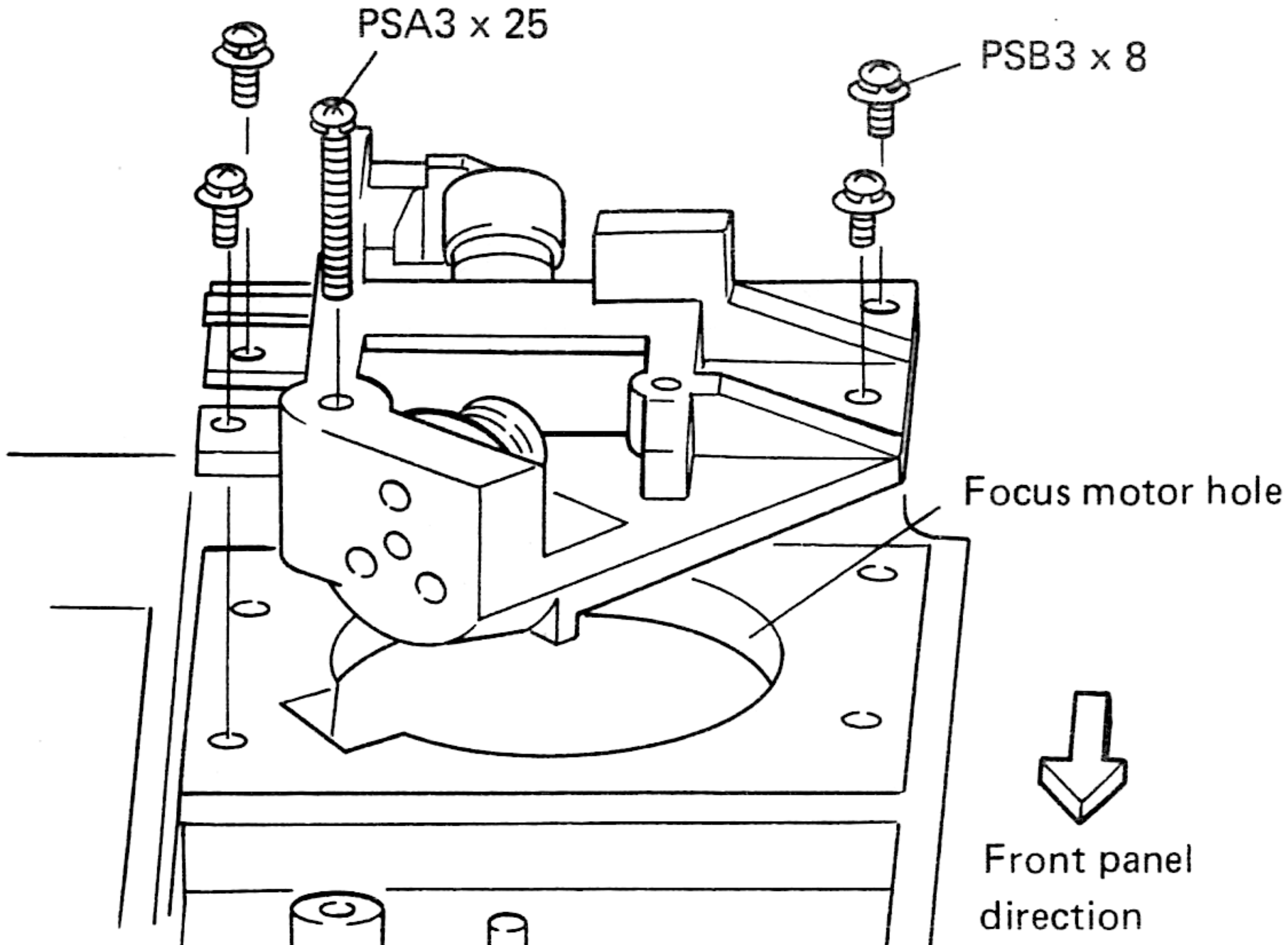


Fig. 53

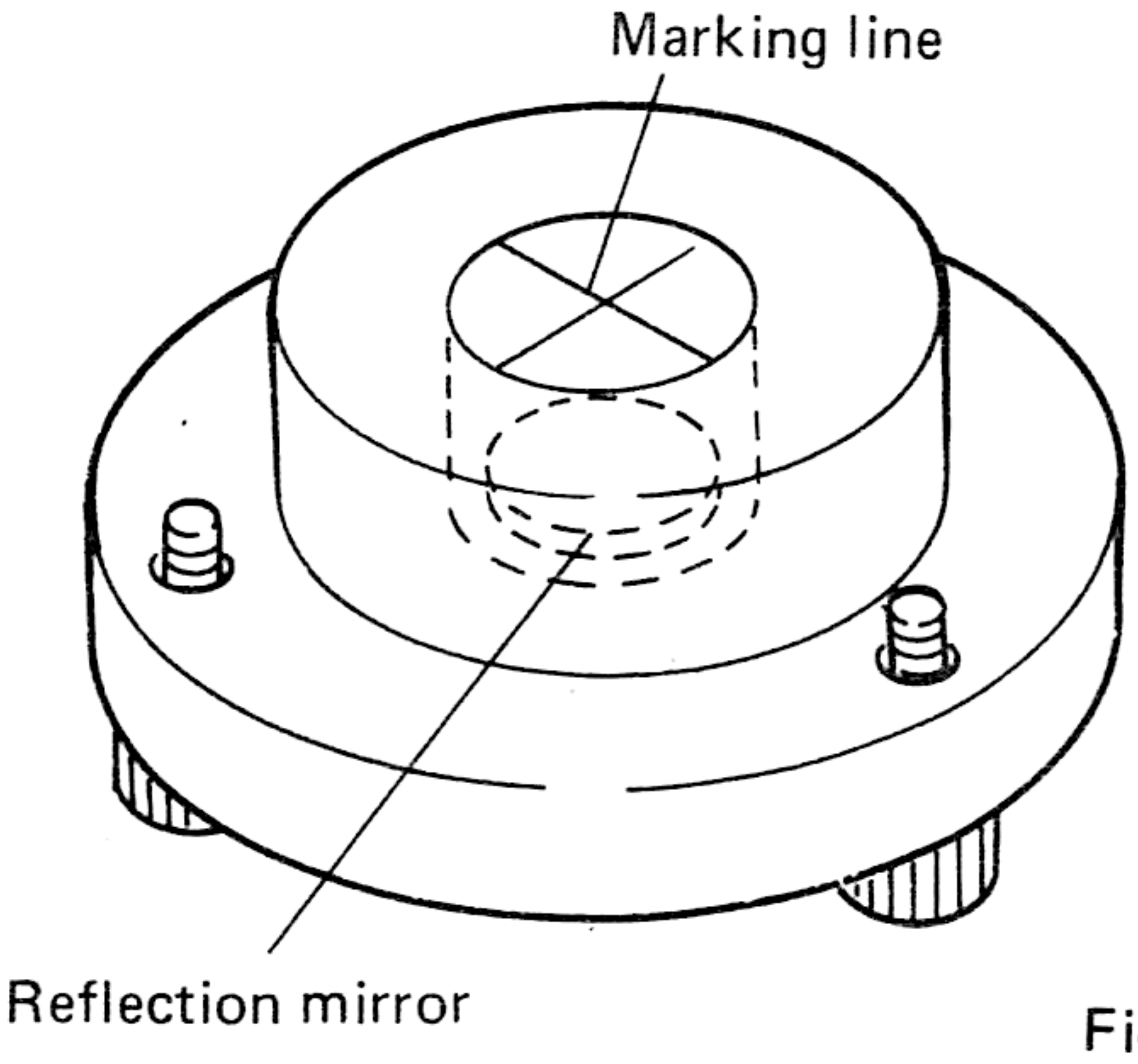


Fig. 54

13.5 OPTICAL AXIS ADJUSTMENT JIG ADJUSTMENTS

13.5.1 Focus motor mounting

Place the cross-line jig exactly under the optical axis prior to the focus motor mounting, and check that the optical axis after mounting the focus motor lies within the cross-line jig circle.

NOTE:
This above condition will always be satisfied as long as the points checked above under step 13-4-8 were OK. If the optical axis fails to lie inside the cross-line jig circle, it means that the points checked under 13-4-8 were not OK, and that step 13-4-6 will have to repeated.

13.5.2 Rough adjustment of 1/4-wave plate ass'y

Turn the 1/4-wave plate ass'y and fix temporarily at the position which gives approximately maximum reflected light at the photo detector position (setting the reflection mirror below the objective lens).

13.5.3 Adjustment and fixing of DG lens and cylindrical lens assemblies

1. Place the DG lens in its prescribed position, and make a rough position adjustment to obtain maximum amount of light below the objective lens.
2. Cylindrical lens mounting and adjustment
   Attach the transparent jig to the wall of the platform, adjust the height of the mobile reflection mirror, and focus the beam onto the transparent jig prior to mounting the cylindrical lens. Either mark the height with several lines, or adjust the height of the jig to that of the beam. Next mount the cylindrical lens, and readjust the height of the mobile reflection mirror, adjusting the height of the cylindrical lens so that the beam is focussed onto the transparent jig at the same height as before.

NOTE:
Push in firmly against the A side before commencing the adjustment.

3. Set the mobile reflection mirror under the objective lens and place the position sensor in the position for the head amplifier. Then adjust the height of the reflection mirror so that the beam focusses onto that position, and also adjust the position of position sensor jig so that the beam passes roughly through the center.
4. Adjust (and fix) the position of the DG lens ass'y to obtain the minimum AC voltage at the position sensor output to drive the mobile reflection mirror.

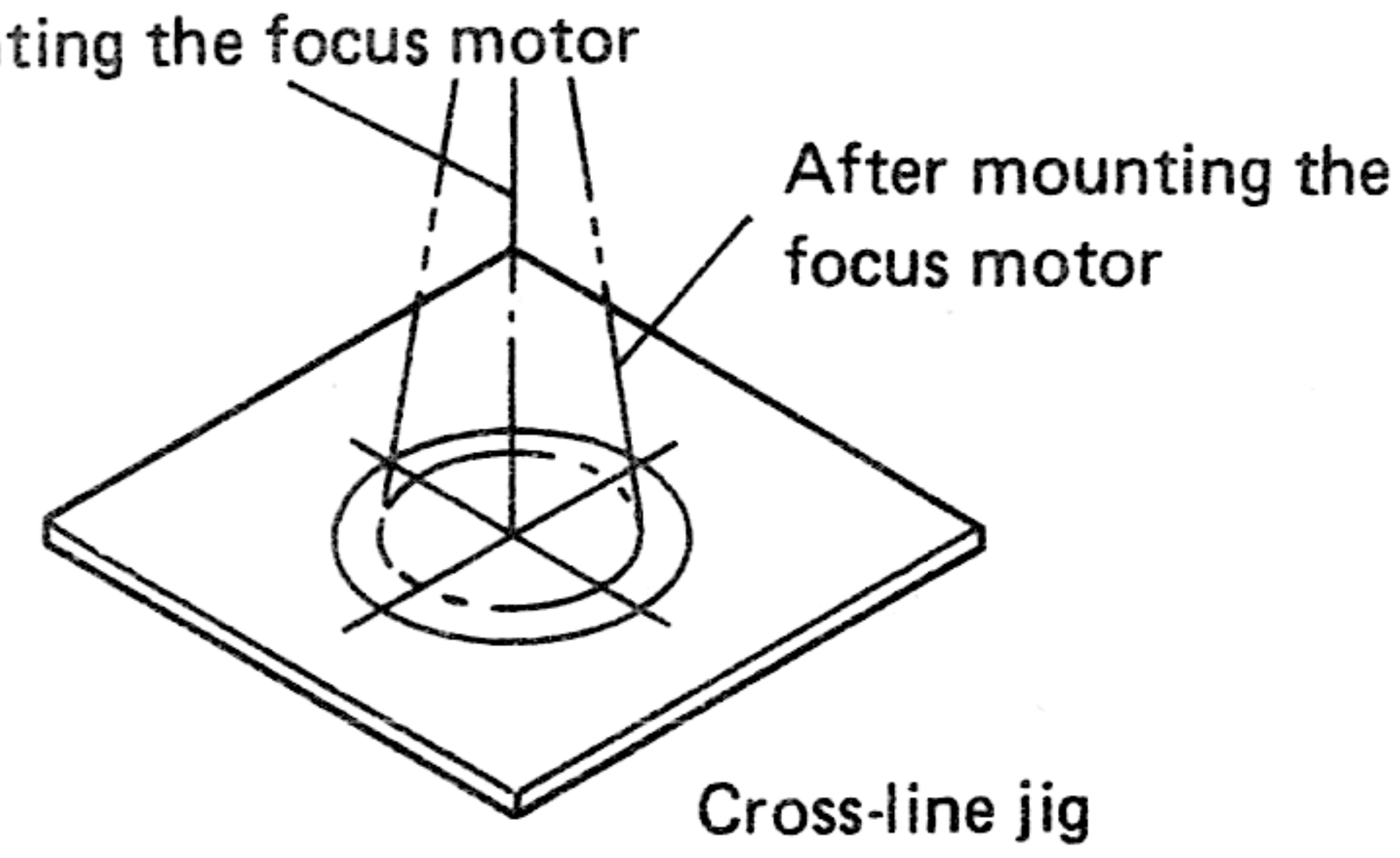

Prior to mounting the focus motor
After mounting the focus motor
Cross-line jig

Fig. 55

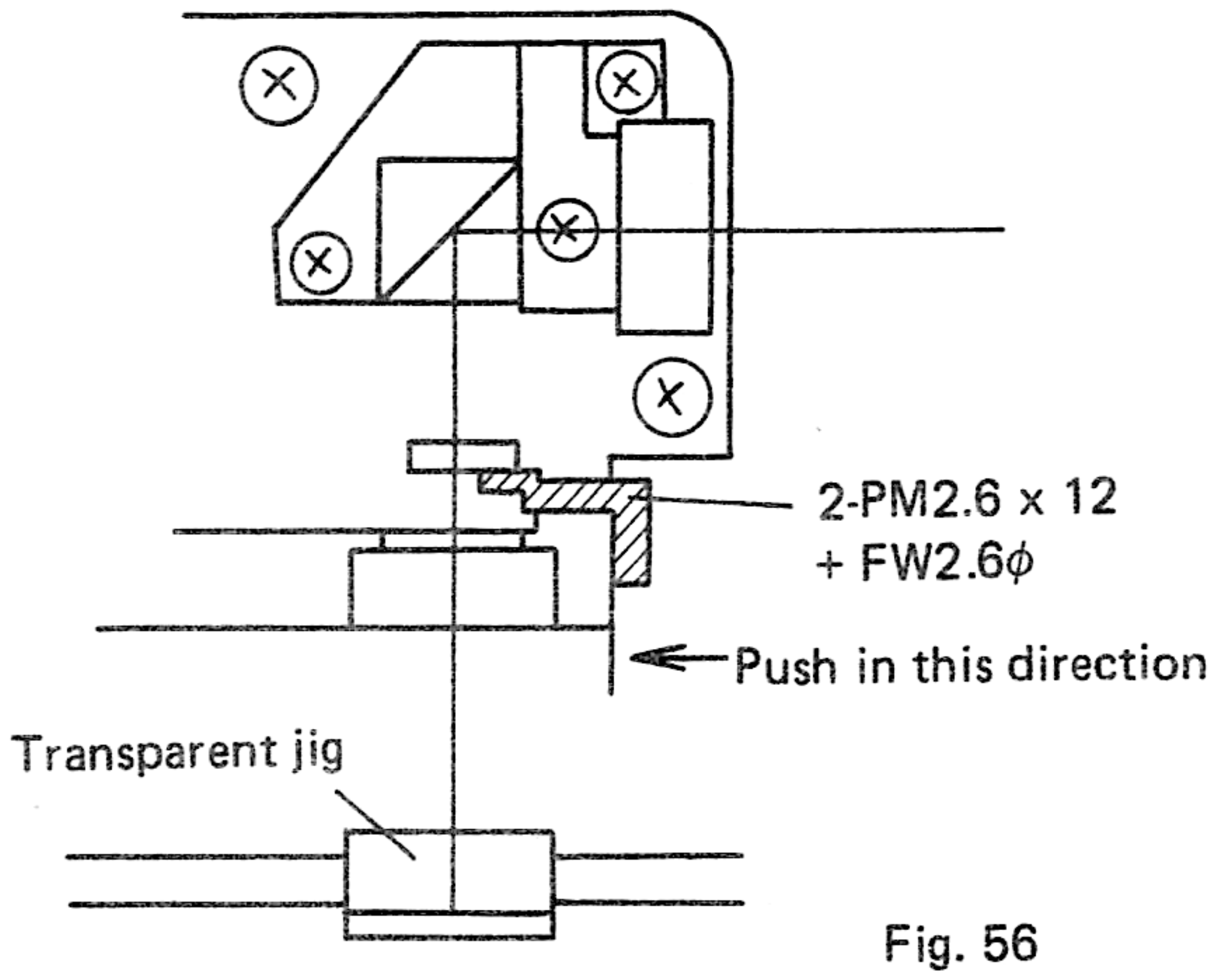


Fig. 56

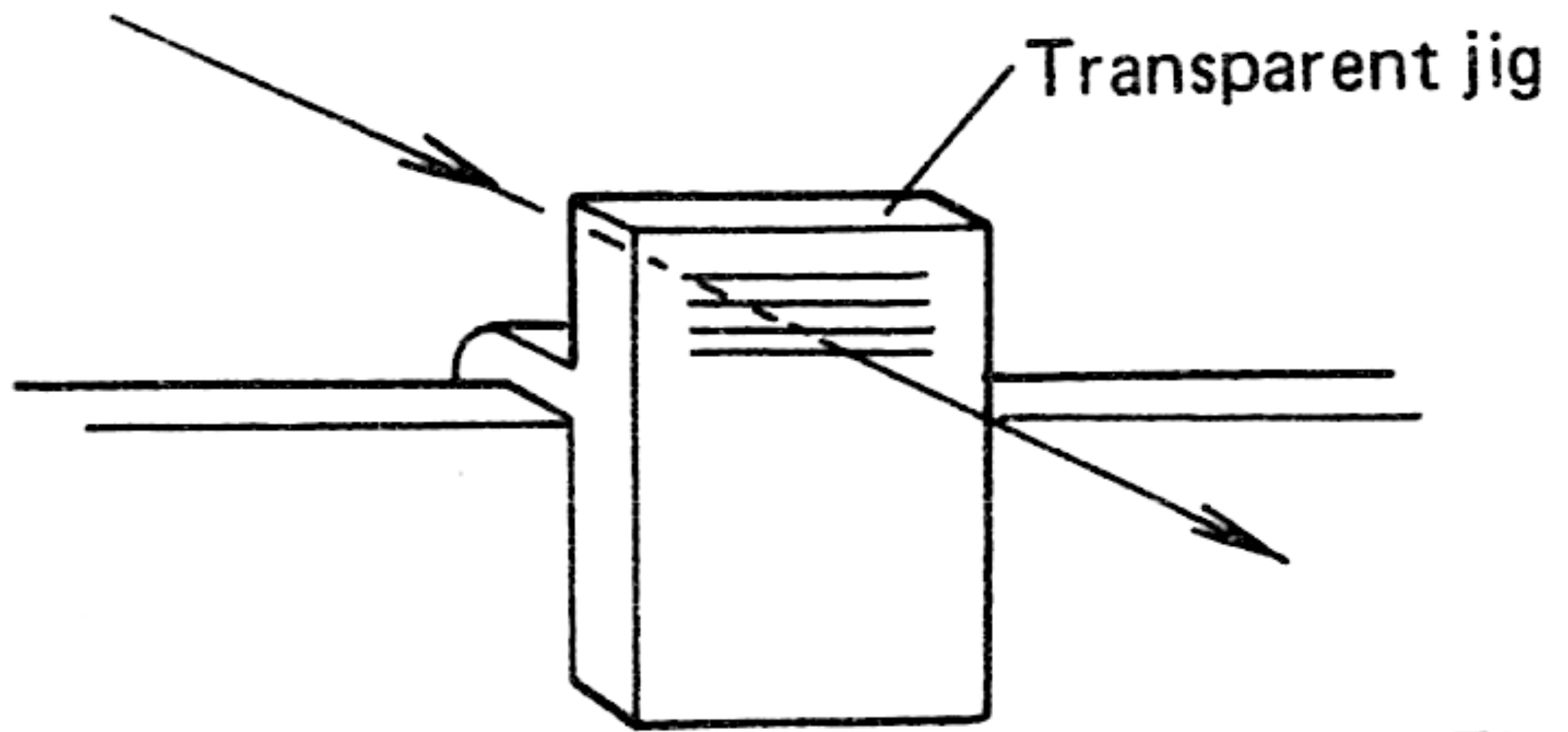


Fig. 57

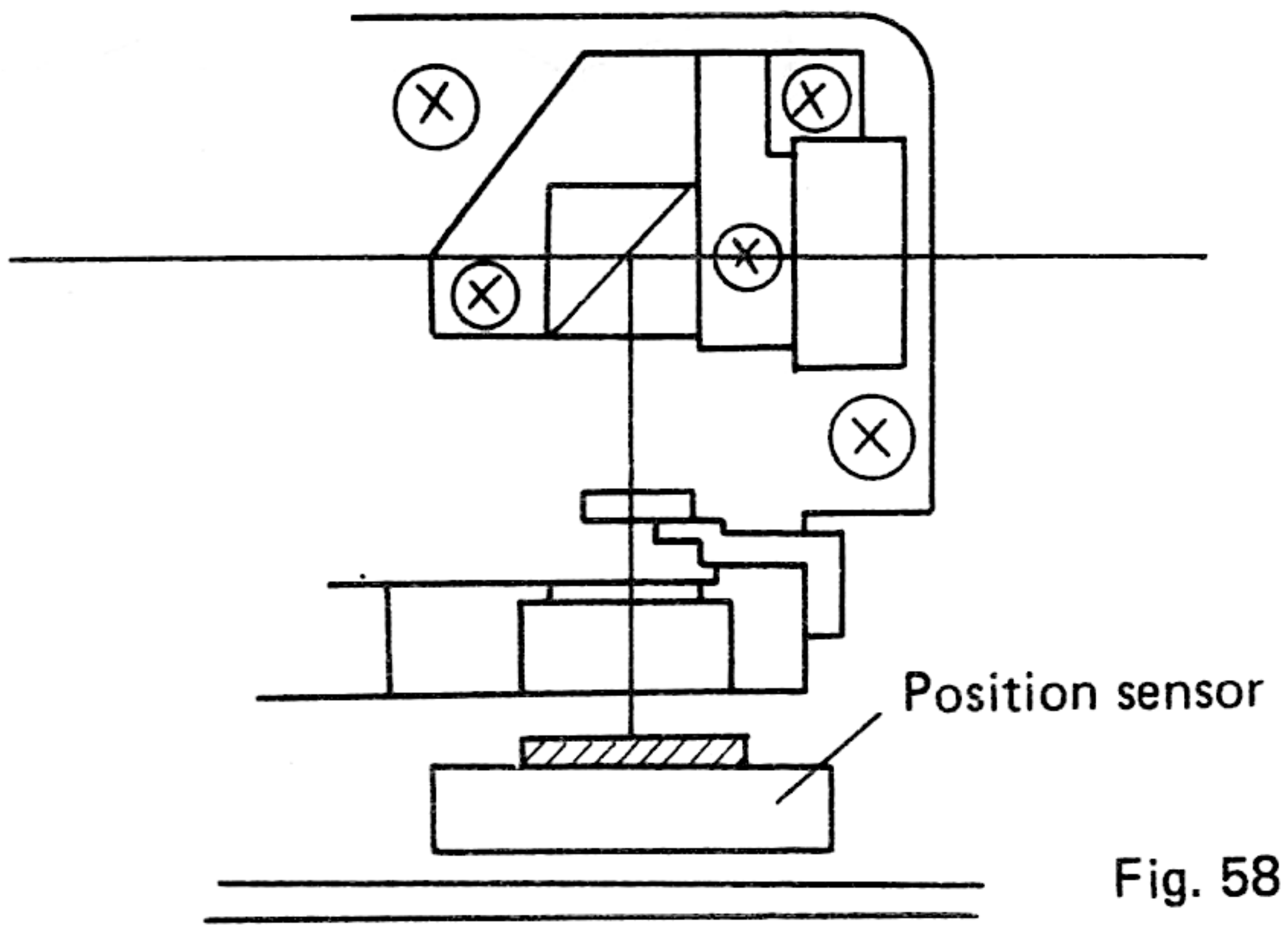


Fig. 58

13.5.4 Adjustment and fixing of the PD ass'y

1. Place the photo detector in its prescribed position, secure the head amplifier, and connect up to the operational amplifier jig connector.
2. Roughly adjust the position and angle of the photo detector so that all 3 beams arrive roughly in the center (observing the area through the tool scope).
3. Raise and lower the mobile reflection mirror to reduce focussing error to almost 0V. Then activate the reflecting mirror, and fine adjust the position of the photo detector so that the operational amplifier jig B1 is more or less equal to B3, and B2 similarly equal to B4. If it proves impossible to match the outputs, repeat step 13-5-3 (3).
4. At this time, record the converted distance from the tip of the objective lens to the base of the platform as based upon the reading of the mobile reflection mirror manipulator.

13.5.5 Pattern shorting, wiring, and clamping

Short circuit (with solder) 4 points on the head amplifier pattern, and connect the mirror transducer and focus motor to the head amplifier, clamping the wiring by means of the platform clamps. (Refer to the general platform ass'y diagram).

13.5.6 Mounting the head amplifier case

1. Solder section (A).
2. Press the insulator in against the head amplifier circuit board, and clamp down with the amplifier case top.

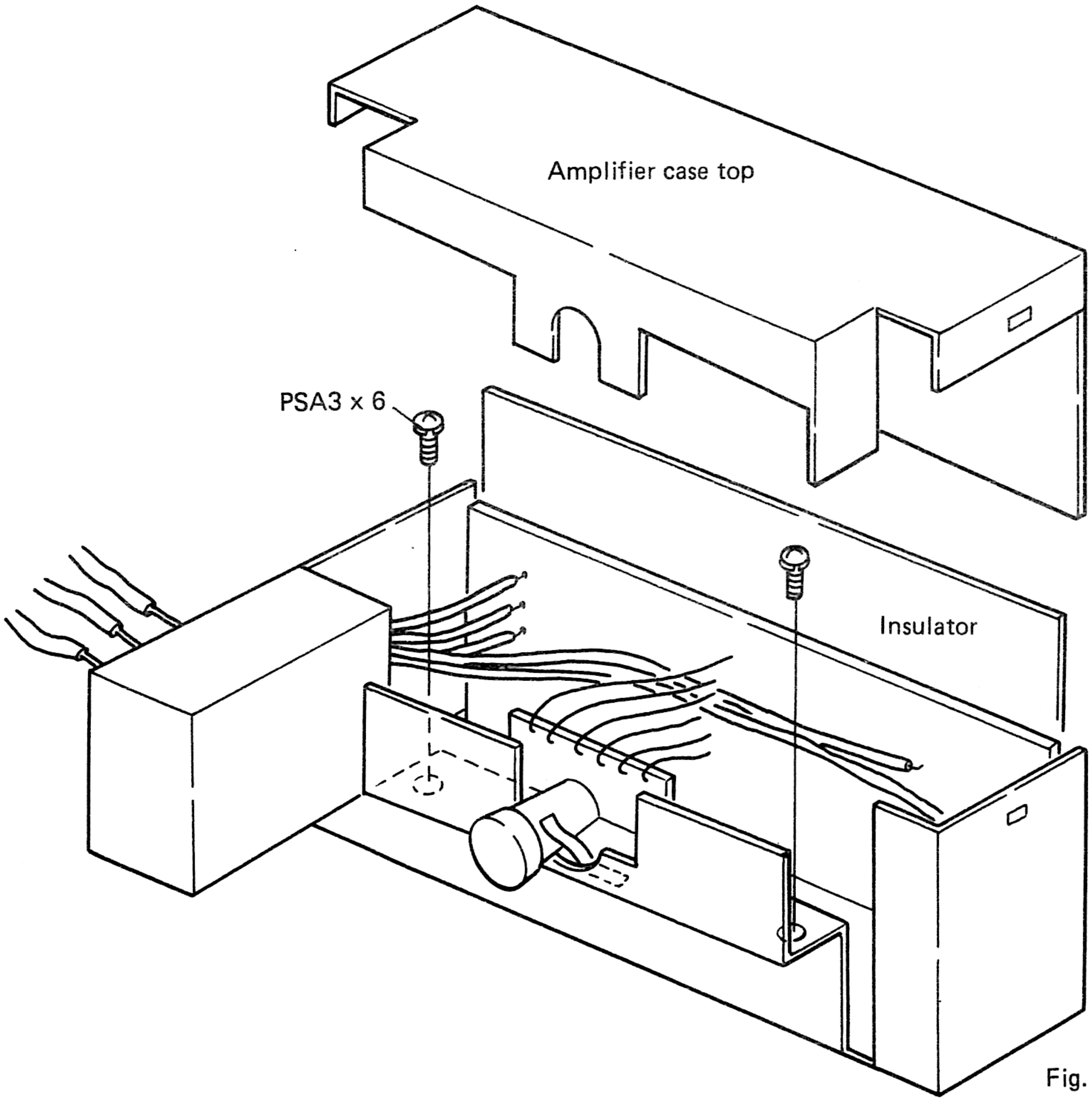


Fig. 59

13.5.7 Beam shutter amplifier case attachment

- Mount the focus mask approximately in the center in respect to the platform base.

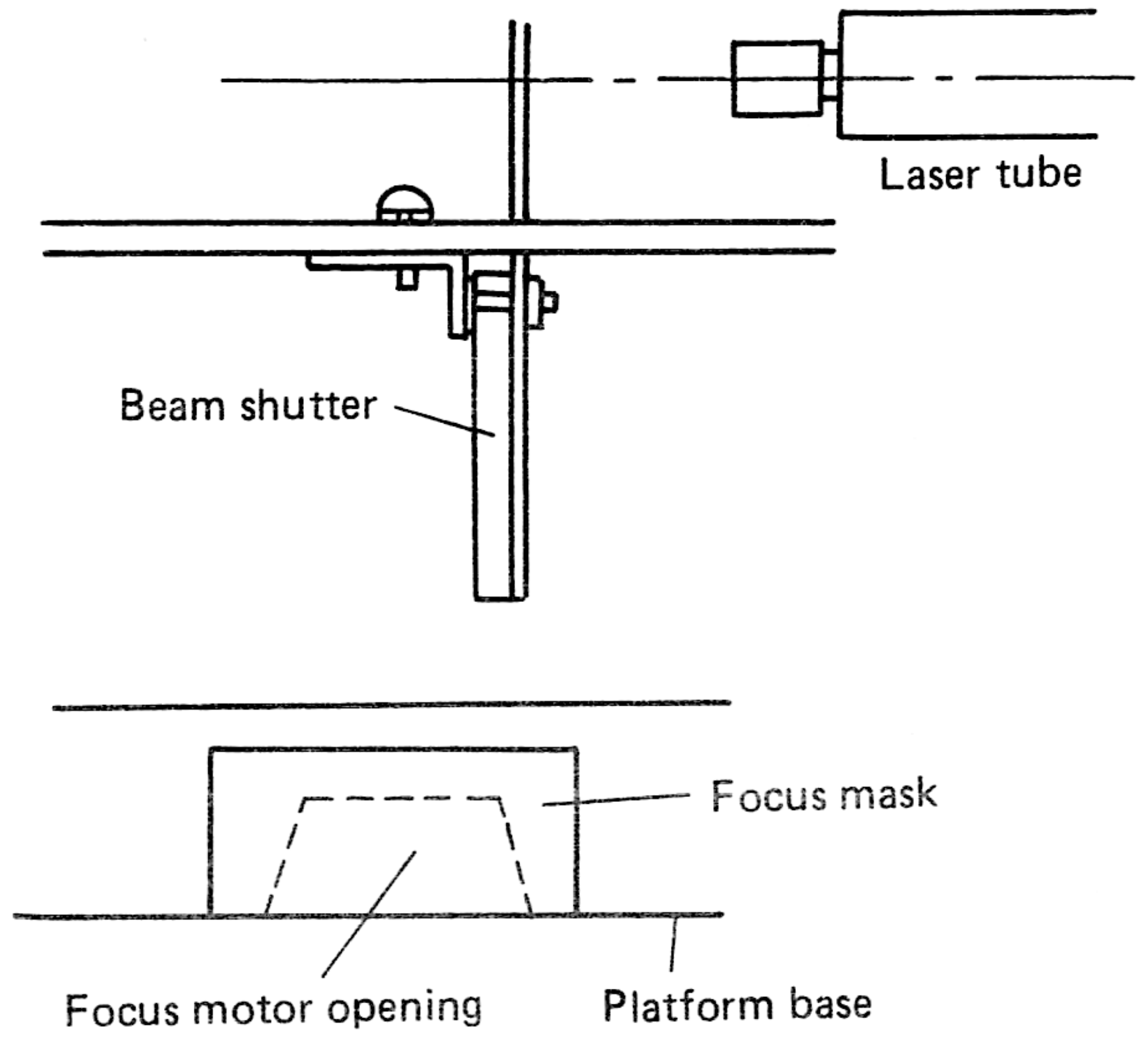


Fig. 60

13.6 MOUNTING THE PLATFORM IN THE DECK

13.6.1 Measure the relative dimensions of the 3 platform mounting posts (L, M, and N) and the spindle cup top (see the above diagrams). The ratio of these values to the amount of objective lens projection from the platform will then determine the thickness of the L, M, and N spacers.

Post height may be adjusted by washers to ensure that the distance from the flat disc surface to the top of the dummy platform equals: —

4 + E + dummy platform thickness − flat disc thickness.

Washer thickness should be determined by taking the average value of the flat disc thickness measured in 4 different directions. Note that carriage position is closest to the platform.

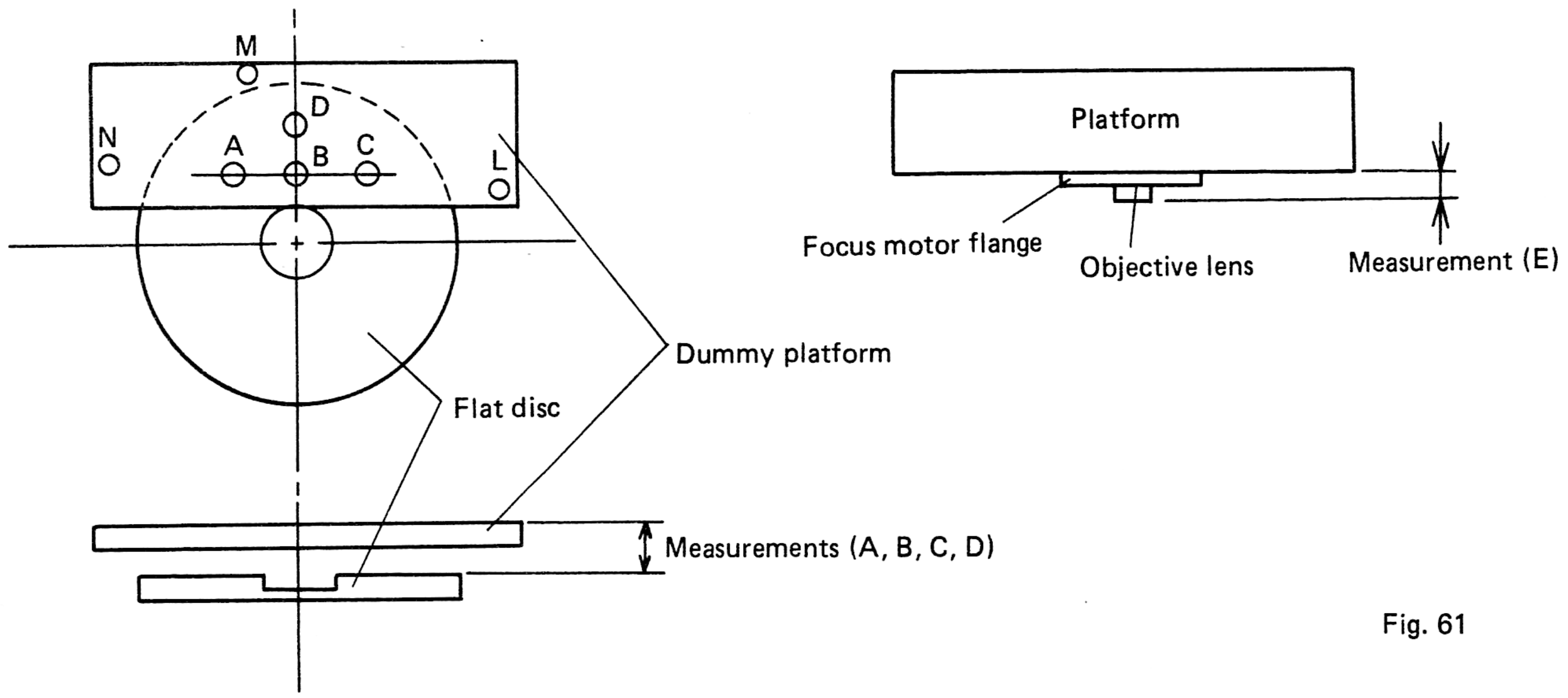
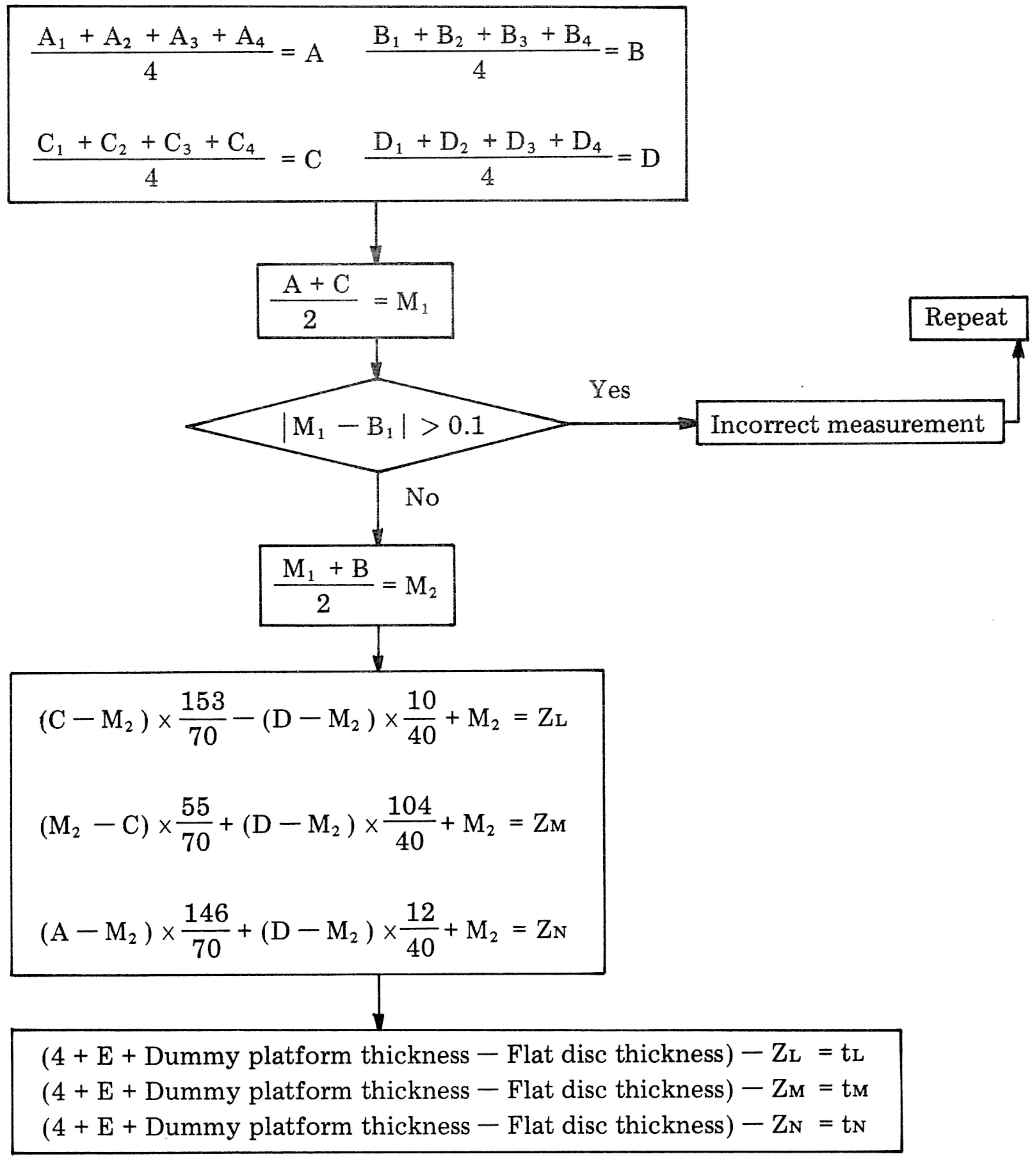


Fig. 61

* Calculations



$$\frac{A_1 + A_2 + A_3 + A_4}{4} = A \qquad \frac{B_1 + B_2 + B_3 + B_4}{4} = B$$

$$\frac{C_1 + C_2 + C_3 + C_4}{4} = C \qquad \frac{D_1 + D_2 + D_3 + D_4}{4} = D$$

$$\frac{A + C}{2} = M_1$$

$$|M_1 - B_1| > 0.1$$

$$\frac{M_1 + B}{2} = M_2$$

$$(C - M_2) \times \frac{153}{70} - (D - M_2) \times \frac{10}{40} + M_2 = Z_L$$

$$(M_2 - C) \times \frac{55}{70} + (D - M_2) \times \frac{104}{40} + M_2 = Z_M$$

$$(A - M_2) \times \frac{146}{70} + (D - M_2) \times \frac{12}{40} + M_2 = Z_N$$

$$(4 + E + \text{Dummy platform thickness} - \text{Flat disc thickness}) - Z_L = t_L$$

$$(4 + E + \text{Dummy platform thickness} - \text{Flat disc thickness}) - Z_M = t_M$$

$$(4 + E + \text{Dummy platform thickness} - \text{Flat disc thickness}) - Z_N = t_N$$

*where t_L, t_M, and t_N are the L, M, and N post spacer thicknesses.

13.7 PLATFORM POSITIONING AND GRATING ADJUSTMENT

13.7.1 Adjust the grating ass'y and focus offset control to obtain maximum tracking error in the vicinity of No. 40000 disc frame. (To obtain the optimum point during this adjustment, turn the adjustment screw back counterclockwise from the position of clearest picture and minimum tracking error, and stop at the 1st maximum point).

13.7.2 Adjust the grating ass'y while monitoring the tracking error in the vicinity of No. 100 disc frame. The peak level obtained should be less than −1dB (approx. −10%) in comparison to the maximum value obtained during the grating adjustment. If it does not, move the platform towards the disc connection, and repeat step 7-1 above.

13.7.3 Grating ass'y adjustment and fixing

If the above tracking error satisfies the specified rating, fix the platform into position, and fine adjust the grating ass'y in the vicinity of No. 10000 disc frame. Then tighten the screws and lock them with Screw-Tight.

13.7.4 1/4-wave plate ass'y adjustment

Monitor the RF signal during stop motion mode and closed tracking, and rotate the 1/4-wave plate to find the position with maximum RF signal level. Fix the plate in this position.

13.8 LIST OF JIGS EMPLOYED

- 2nd adjustment jig
- prism adjustment jig II
- 3rd optical axis jig
- reflection mirror jig
- cross-line jig
- transparent jig
- slitting jig
- tracking ass'y adjustment jig
- position sensor
- operational amplifier jig
- power supply protection cover
- power meter
- transformer jig (laser power supply)
- aging jig

13.9 DIAGRAMATIC OUTLINES OF MEASURING CIRCUITS

13.9.1 Position sensor

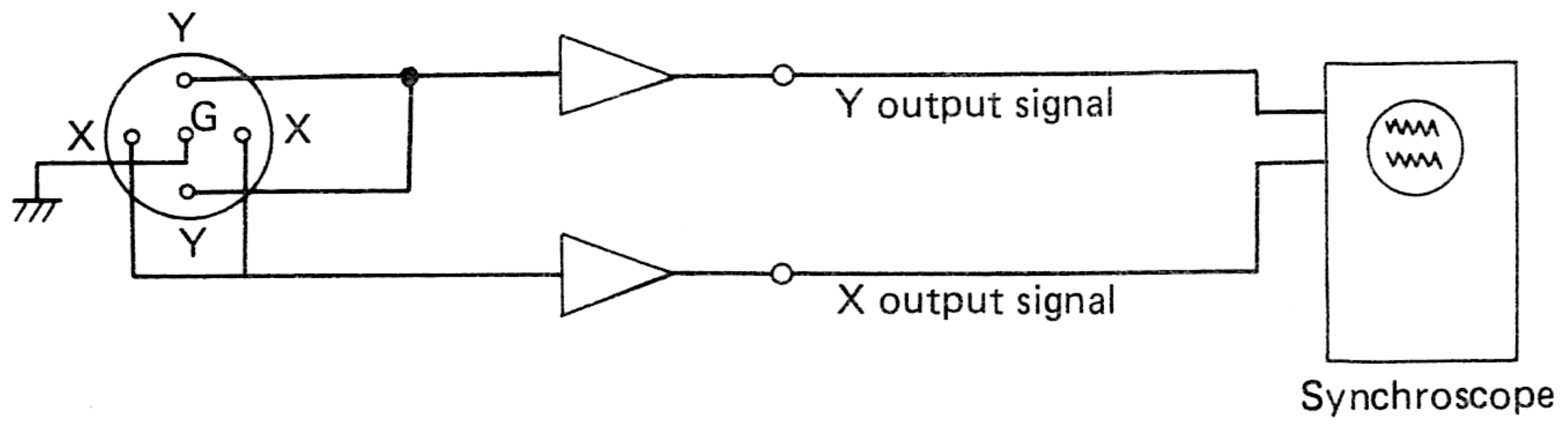


Fig. 62

13.9.2 Operational amplifier jig

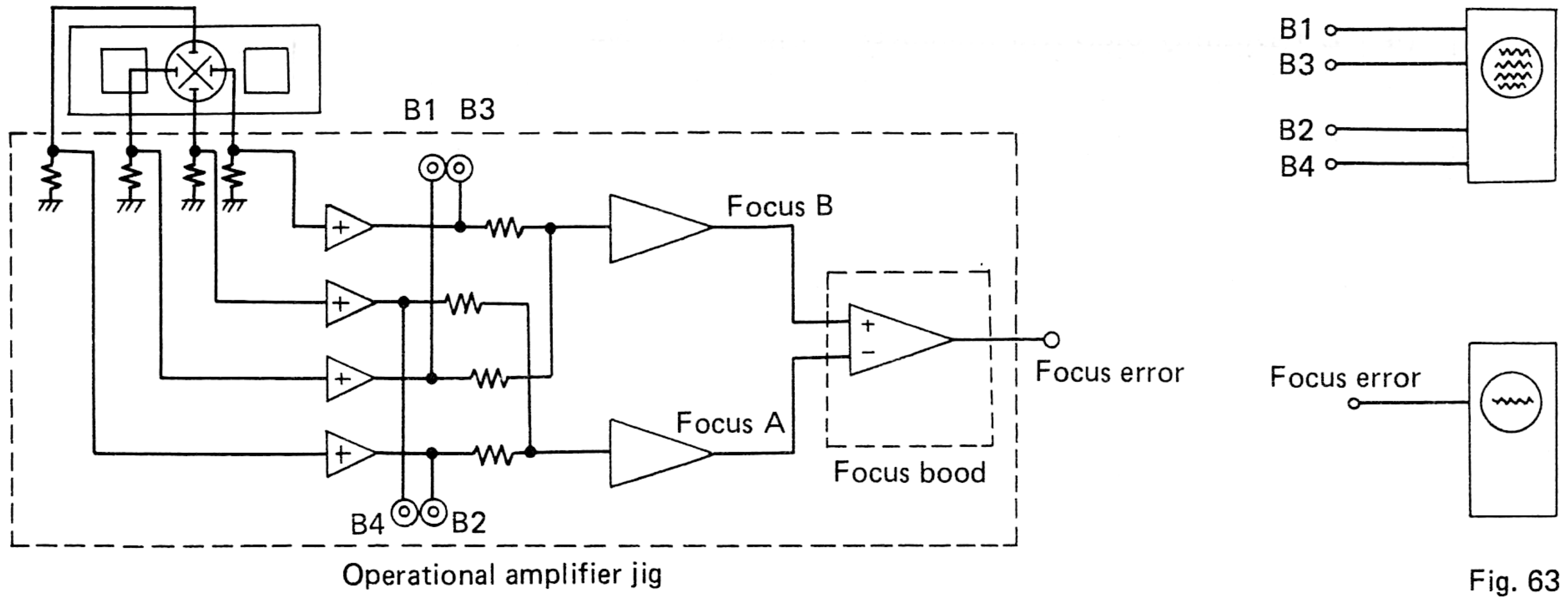


Fig. 63

13.9.3 Optical axis adjustment jig

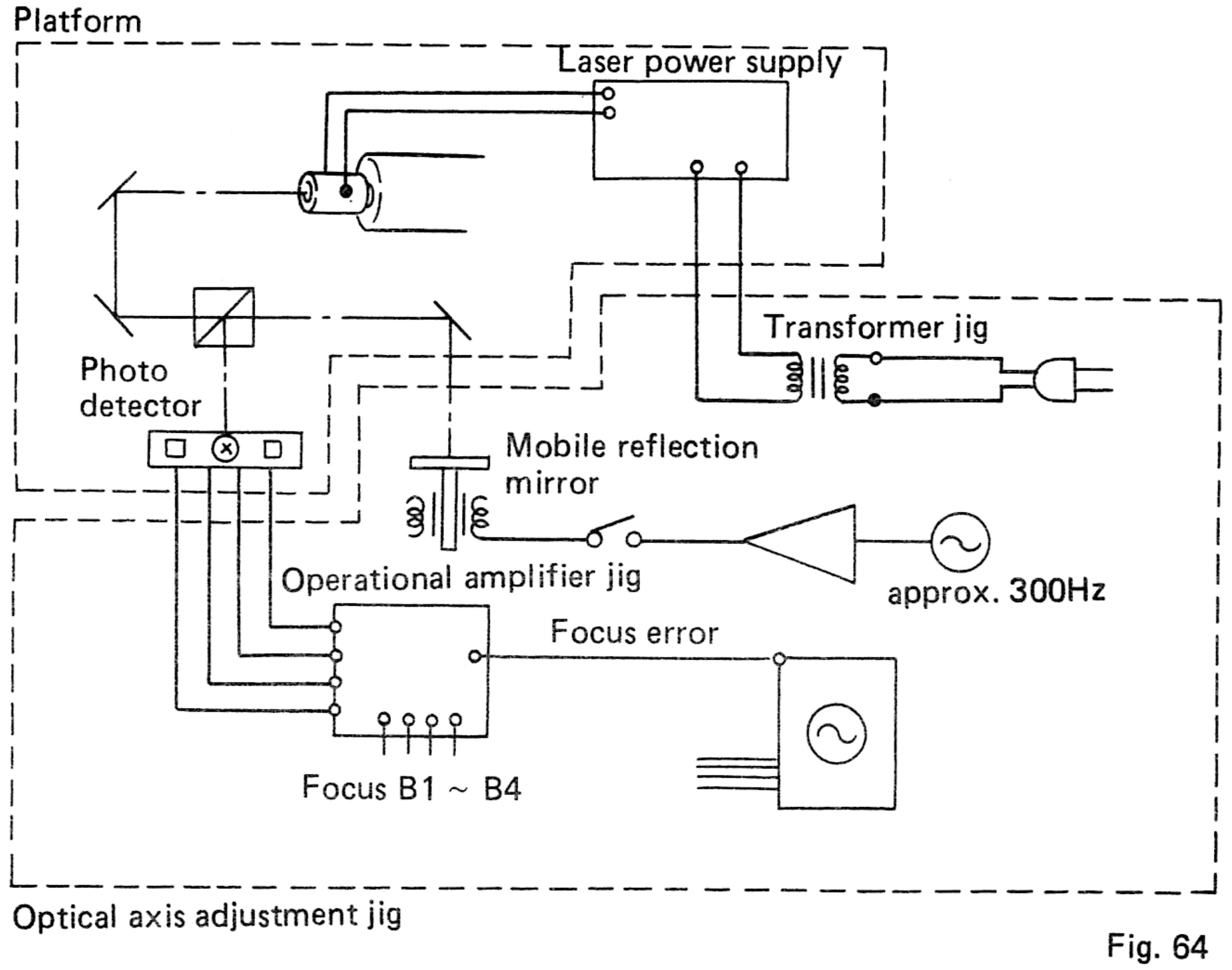


Fig. 64

13.9.4 Tracking ass'y adjustment jig

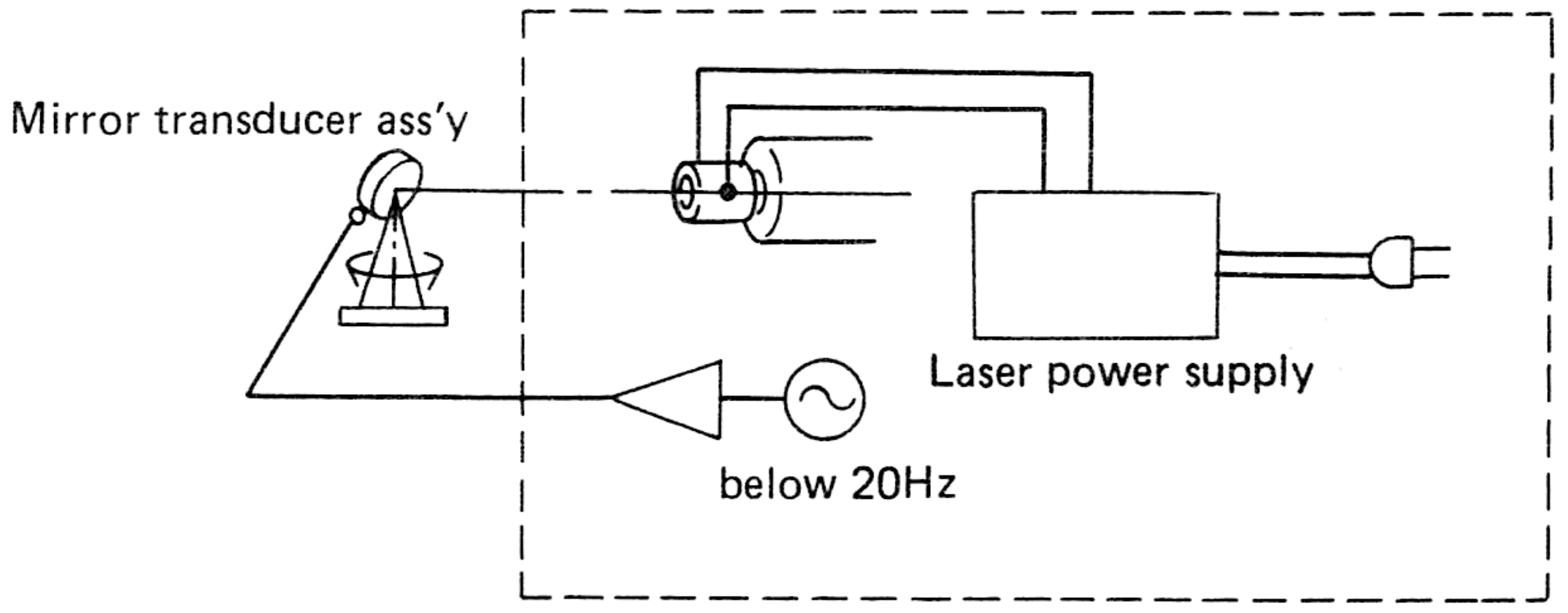


Fig. 65

13.9.5 Aging jig

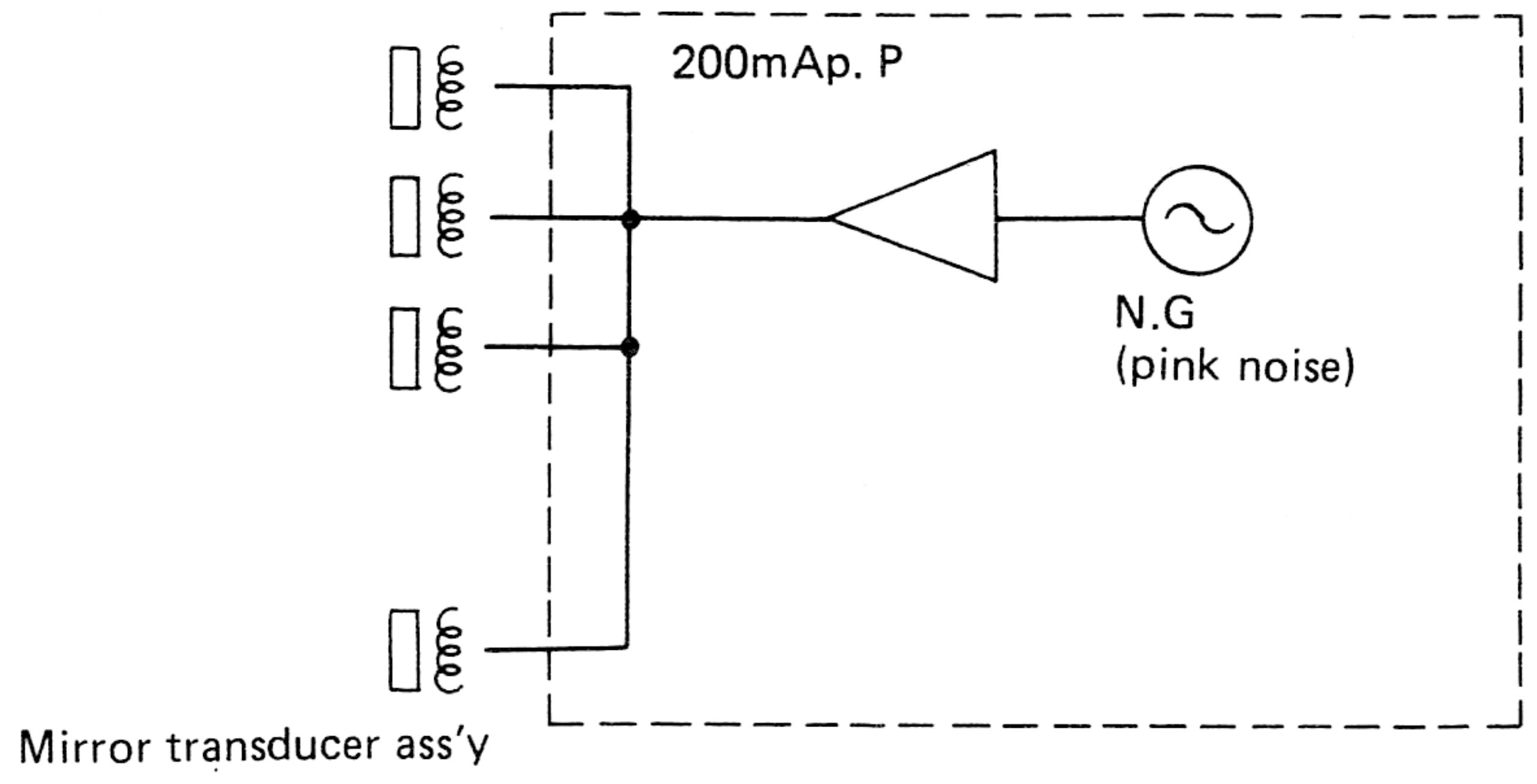
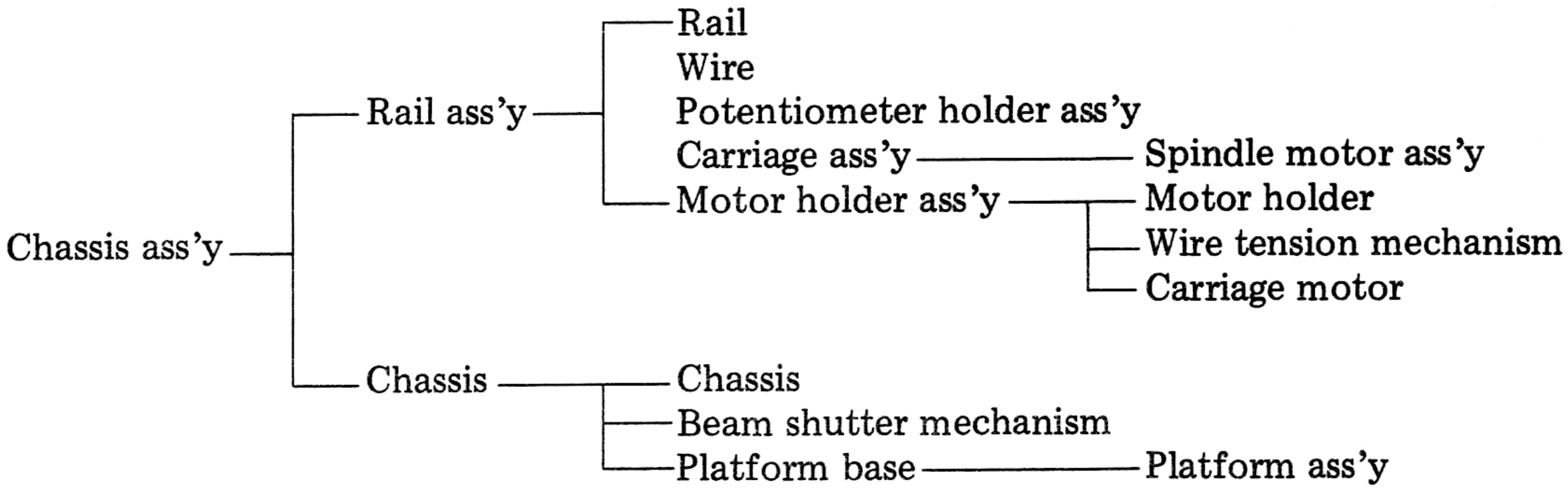


Fig. 66

14. MECHANISM DESCRIPTIONS

14.1 ASSEMBLY (AND DISASSEMBLY) OF MECHANICAL COMPONENT PARTS PLUS PRECAUTIONS

14.1.1 Mechanical component parts



14.1.2 Assembly (and disassembly) procedures

(1) Potentiometer holder assembly procedure
(2) Carriage assembly procedure
(3) Motor holder assembly procedure
(4) Chassis — beam shutter mechanism assembly procedure

14.1.3 Assembly and adjustment of ass'y parts

a. Rail ass'y

- Mount the potentiometer holder ass'y, carriage ass'y, and motor holder ass'y on the rail.
- Mount the spindle motor ass'y onto the carriage, adjusting the height and central position during the same procedure.

b. Wire stringing
String the wire and adjust wire tension.

c. Mount rail ass'y into the chassis ass'y
Insert the rail into the 2 designation positions in the chassis, and then tighten the screws.

d. Chassis wiring
Attach the spindle cord cover.

14.2 TROUBLESHOOTING

14.2.1 Carriage fails to move

a) Failure in carriage motor or electrical system.
— refer to relevant sections.

b) Failure due to wire

Causes:
- Wire damage or caulking loss.
- Wire disengaged from roller or pulley.
- Section A (see Fig. 67) slipped out of position, and metal plate becomes caught (loose wire).

Repair:
- Replace wire.
- Re-string the wire.
- Reinsert metal plate into guide hole.

c) Potentiometer burning

Repair:
- Replace potentiometer.

d) Roller burning

Repair:
- Replace roller.

e) Blind touches against potentiometer holder (see Fig. 68).

Repair:
- Readjust tightness of blind securing screw.

f) Spindle motor in contact with top blind (see Fig. 69).

Repair:
- Correct any bending or warping in the top blind.

g) Carriage stopper release overlooked

Repair:
- Release the carriage stopper, and check that carriage stopper operates smoothly under spring action.

14.2.2 Generation of abnormal sound

Same as 1) a), b), c), d), e), f) and g) above.

14.2.3 No picture due to beam output failure.

(Beam output fails to appear after closing the hood, and the carriage moves across to its prescribed position).

a) Beam shutter failure.

Causes:
1. i. Link not properly coupled.
2. ii. Faulty coupling between beam shutter hunter (E) and platform link.
3. iii. Laser shutter displacement too small.

Repair:
1. i. Make sure link is properly coupled.
2. ii. Insert pin properly into guide hole.
3. iii. Check tightness of the securing screw for the laser shutter mounting jigs at the position where the beam is known to appear.

14.2.4 Inter-lock and beam shutter fail to operate correctly

Problem:

Hood opened while picture shown on screen, but fails to close again properly.

Cause:

i. Hood lock malfunctioning.
ii. No. 1 microswitch not properly adjusted.

Repair:

i. Readjust inter-lock pin, inter-lock mounting jig, and hinges.
ii. Readjust microswitch on/off action.

Problem:

No response when PLAY button pressed.

Cause:

No. 2 microswitch not properly adjusted.

Repair:

Readjust No. 2 microswitch to ensure proper on/off action when hood is closed.

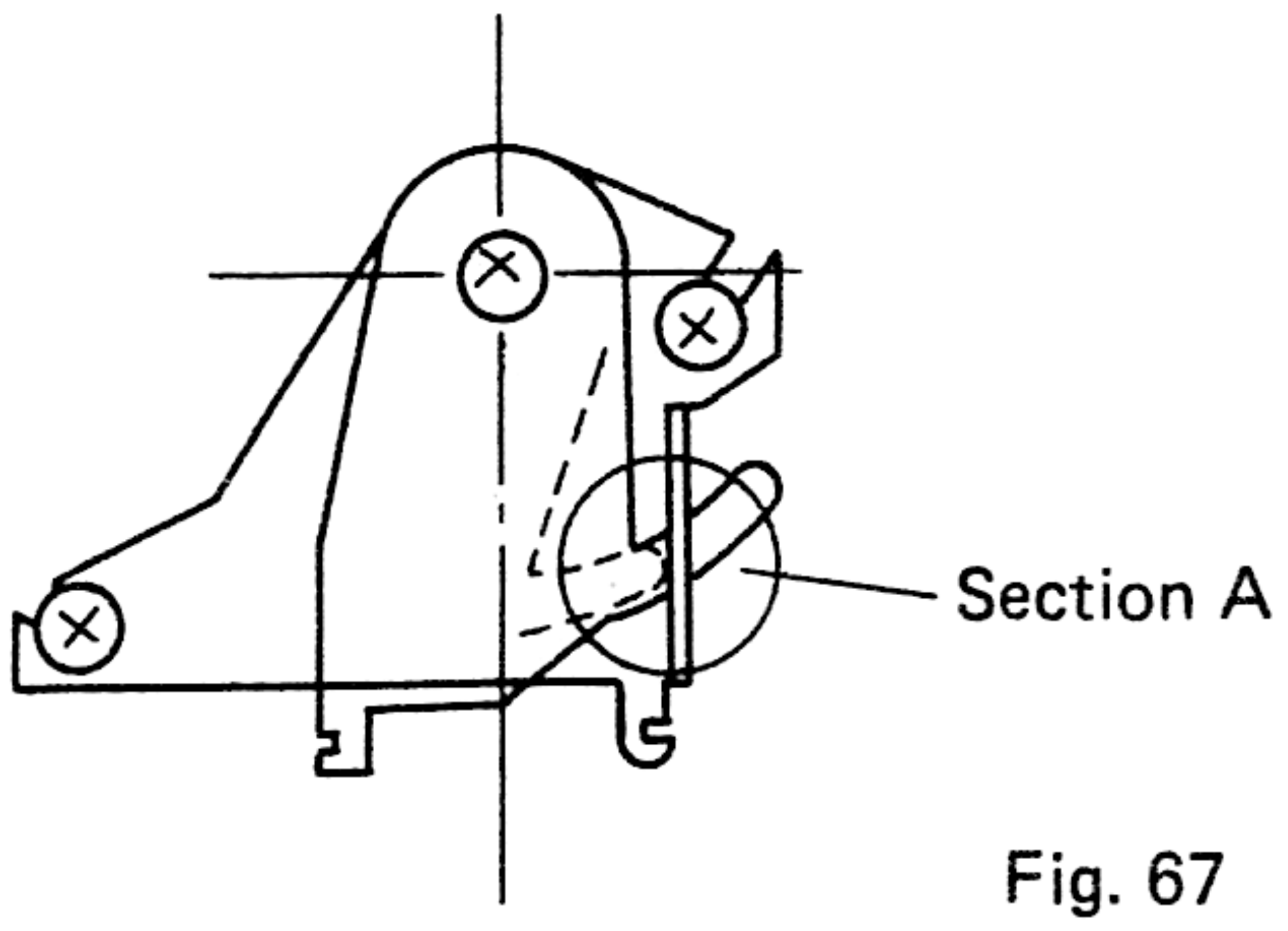


Fig. 67

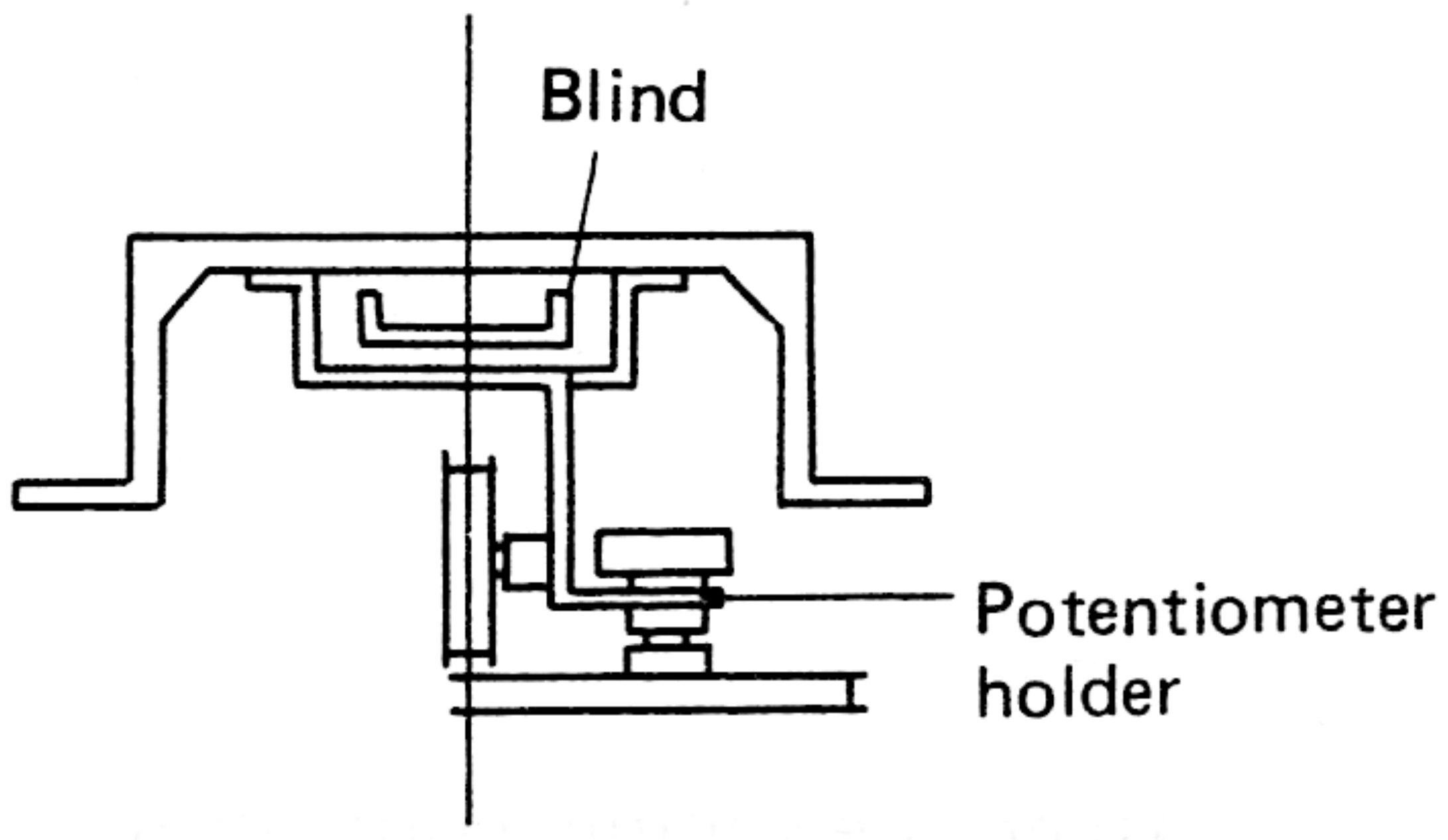


Fig. 68

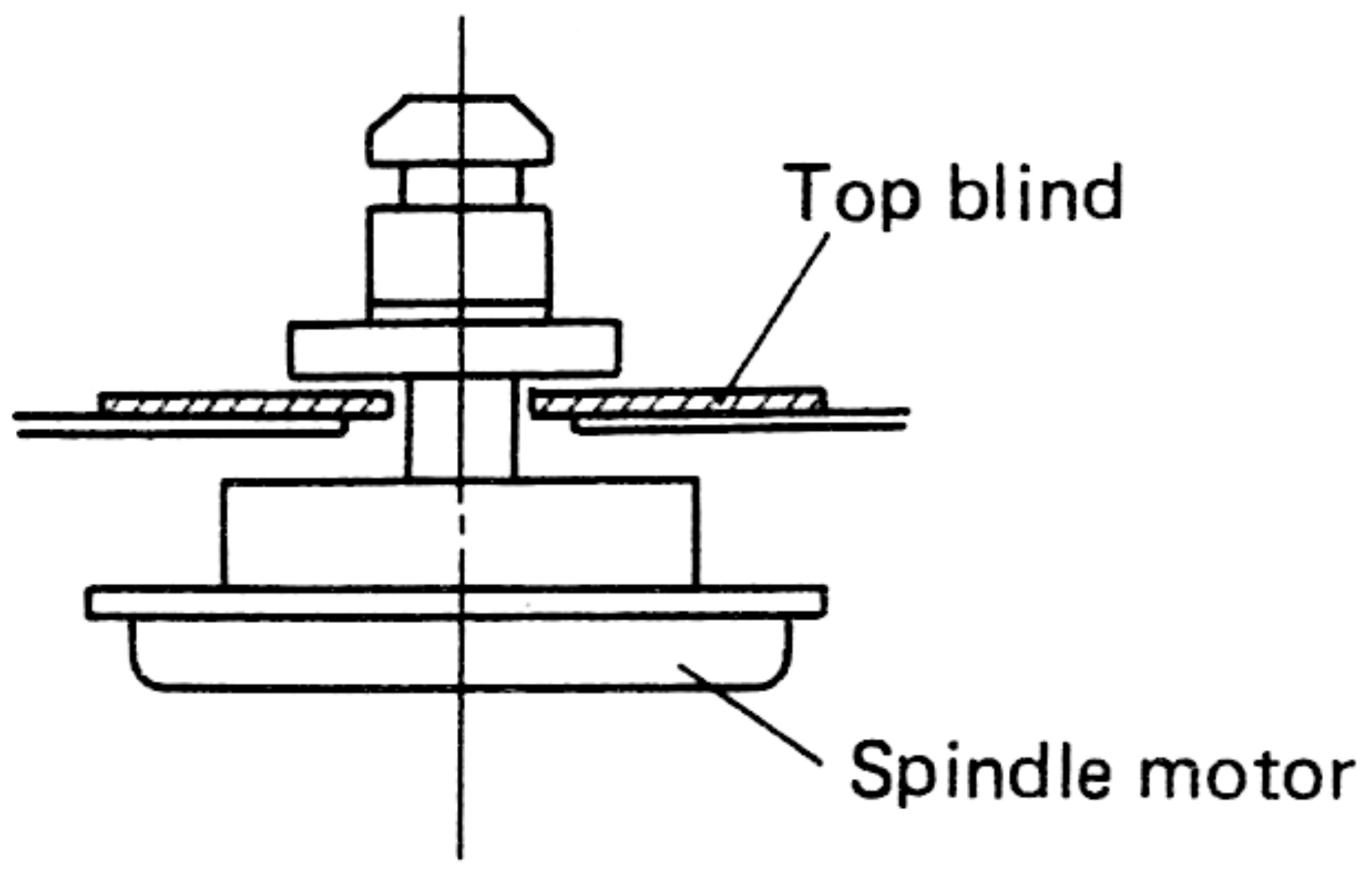


Fig. 69

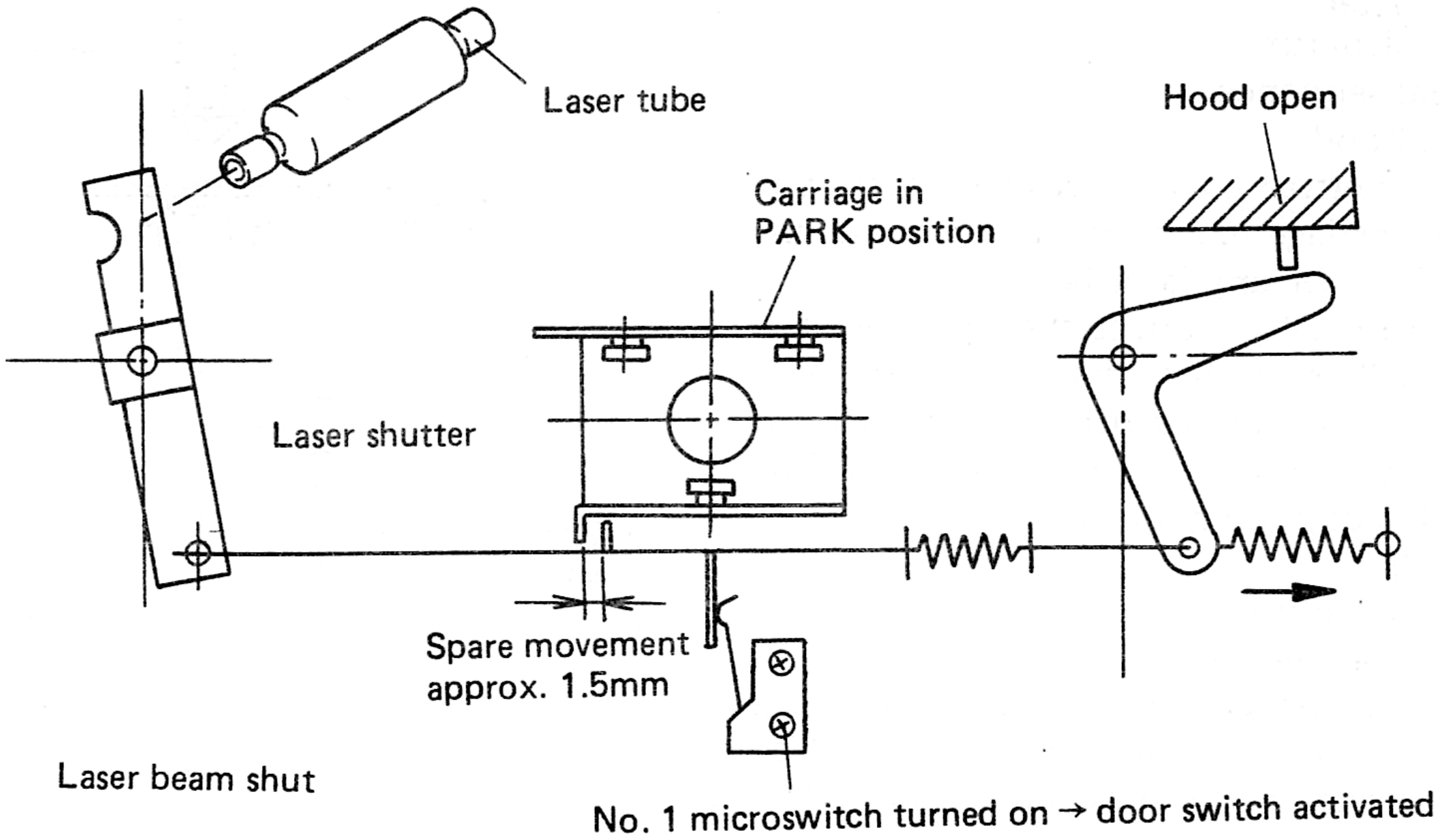

Laser tube
Hood open
Carriage in PARK position
Laser shutter
Spare movement approx. 1.5mm
Laser beam shut
No. 1 microswitch turned on → door switch activated

Fig. 70

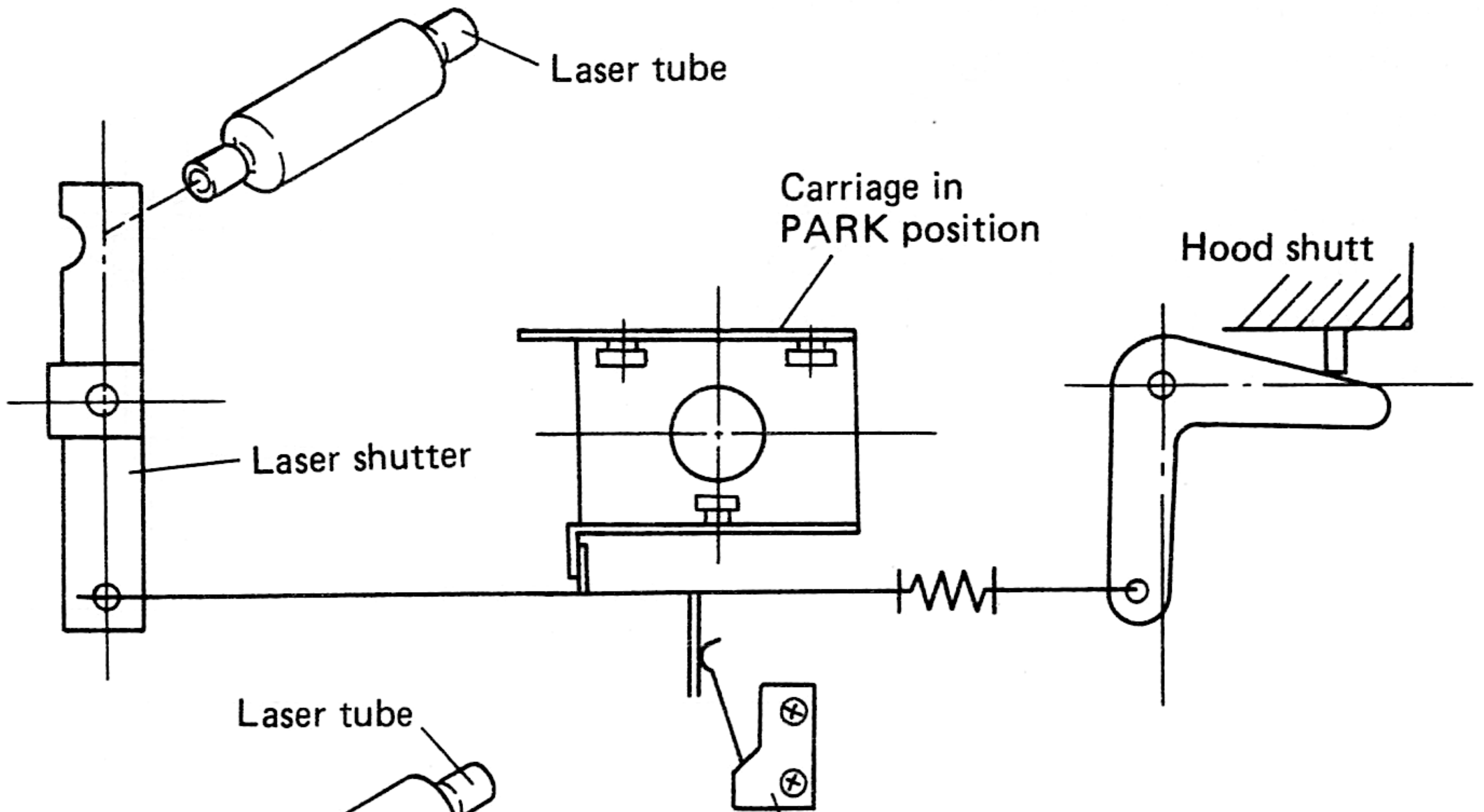

Laser tube
Carriage in PARK position
Hood shutt
Laser shutter
No. 1 microswitch turned on → door switch activated

Fig. 71

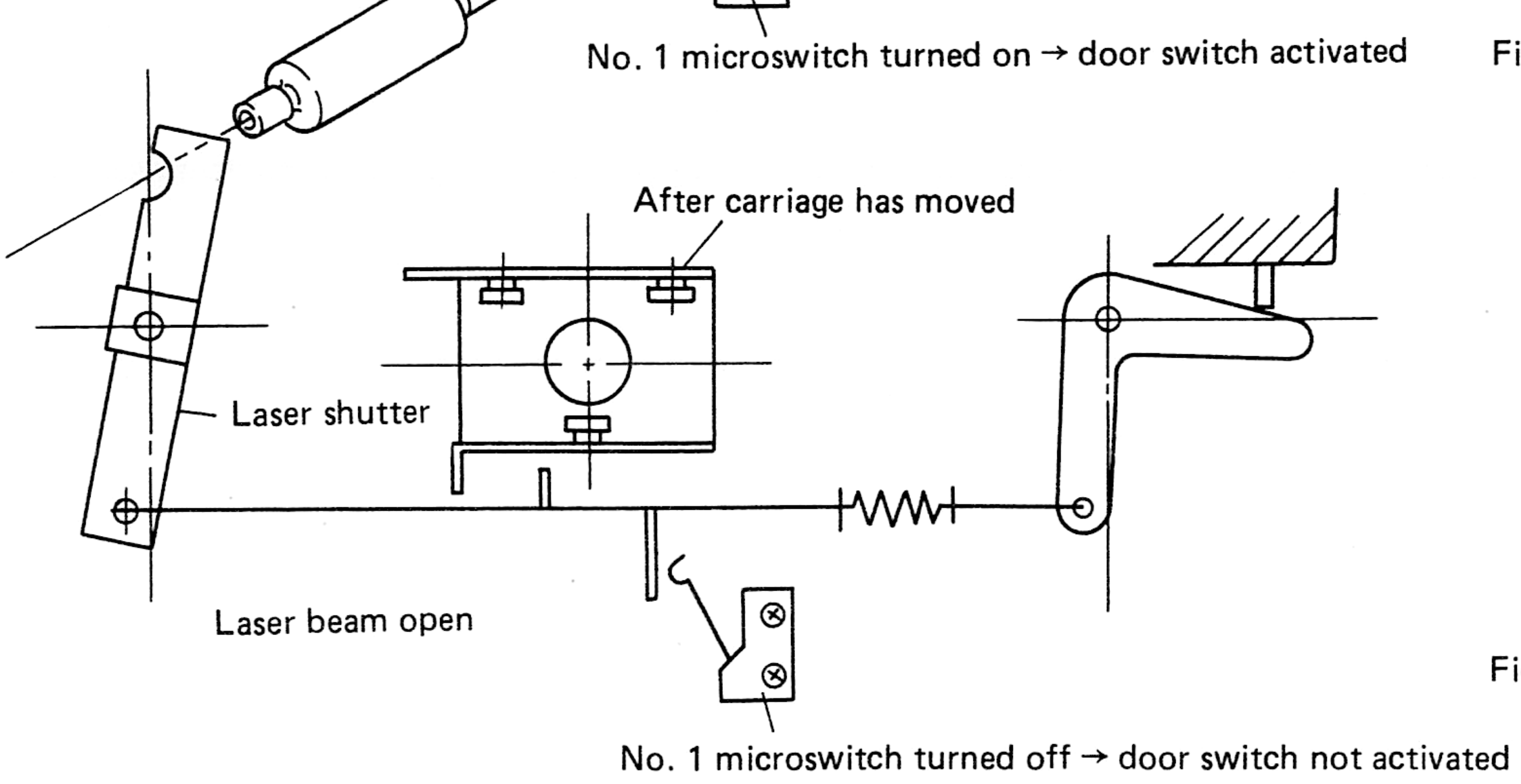


Fig. 72

14.3 BEAM SHUTTER AND INTER-LOCK MECHANISM OPERATION

14.3.1 Beam shutter

a) Outline of structure

b) Operational sequence:

1. Close the hood.
2. The laser shutter commences to rotate, but since the carriage blocks any link movement, there will not be any laser beam.
3. When the PLAY button is then pressed, the carriage will move out, and the laser beam appear. No. 1 microswitch turns off to prevent the door switch from activating, thereby locking the hood shut.

14.3.2 Inter-lock

a) Outline of structure

b) Operational sequence:

1. The hood is locked mechanically when it is closed. In this condition the door cannot be opened unless the door switch is pressed to activate the plunger.
2. And since the plunger is connected in series with No. 1 microswitch, the plunger will not move once the switch is turned off by the movement of the carriage.
3. No. 2 microswitch is turned on once the hood is closed, but note that the PLAY button will not function as long as the hood remains open.

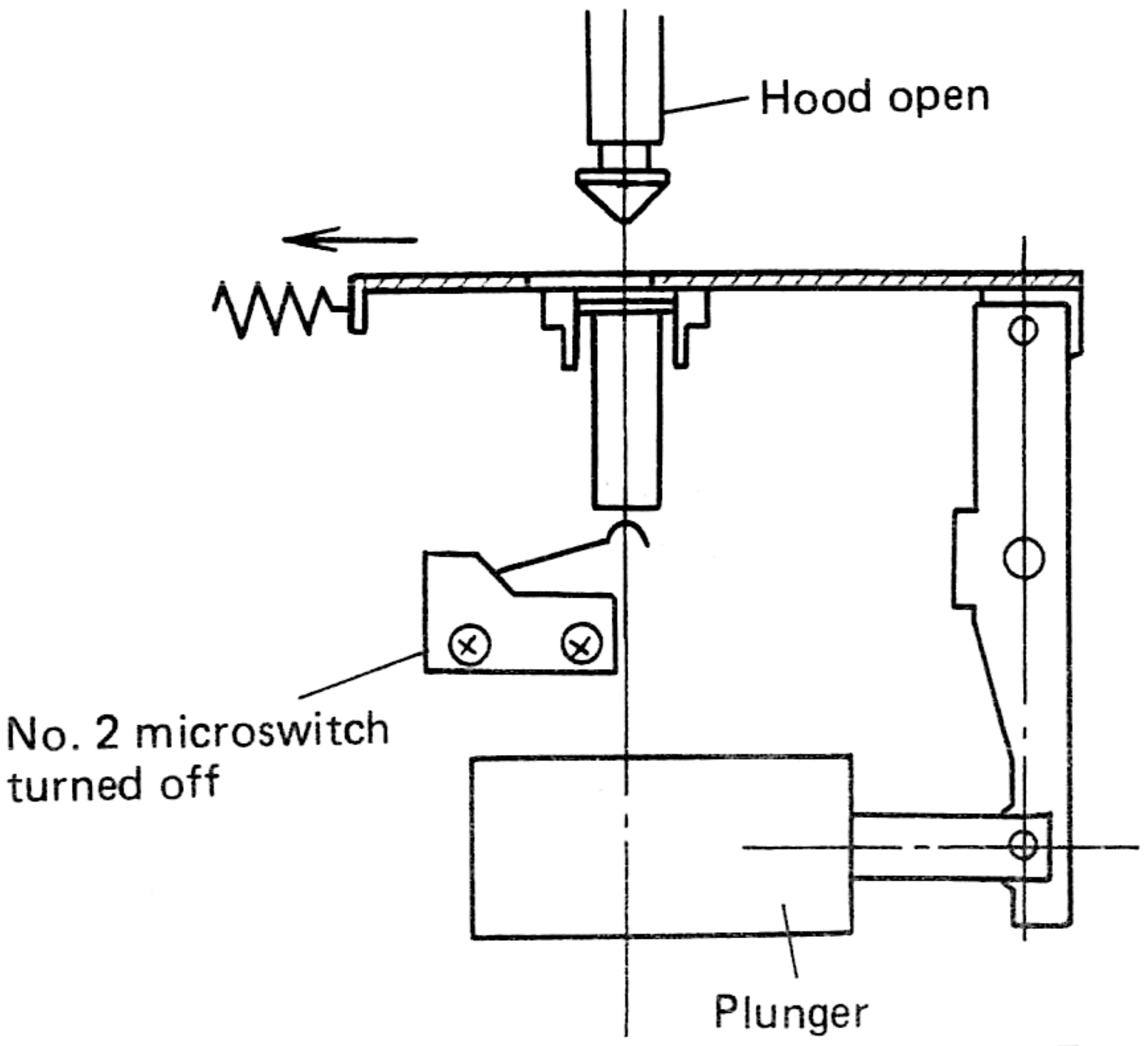


Fig. 73

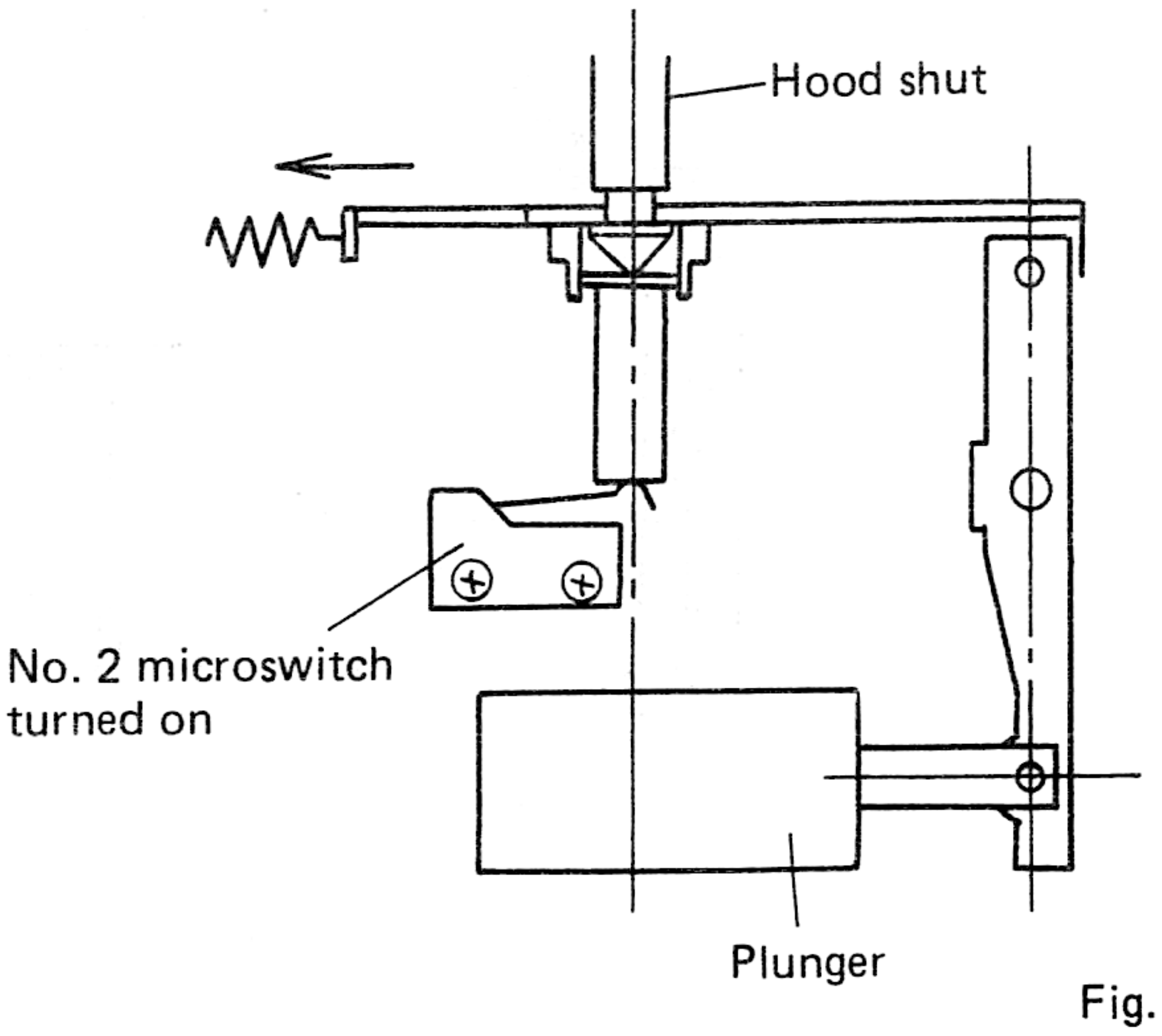


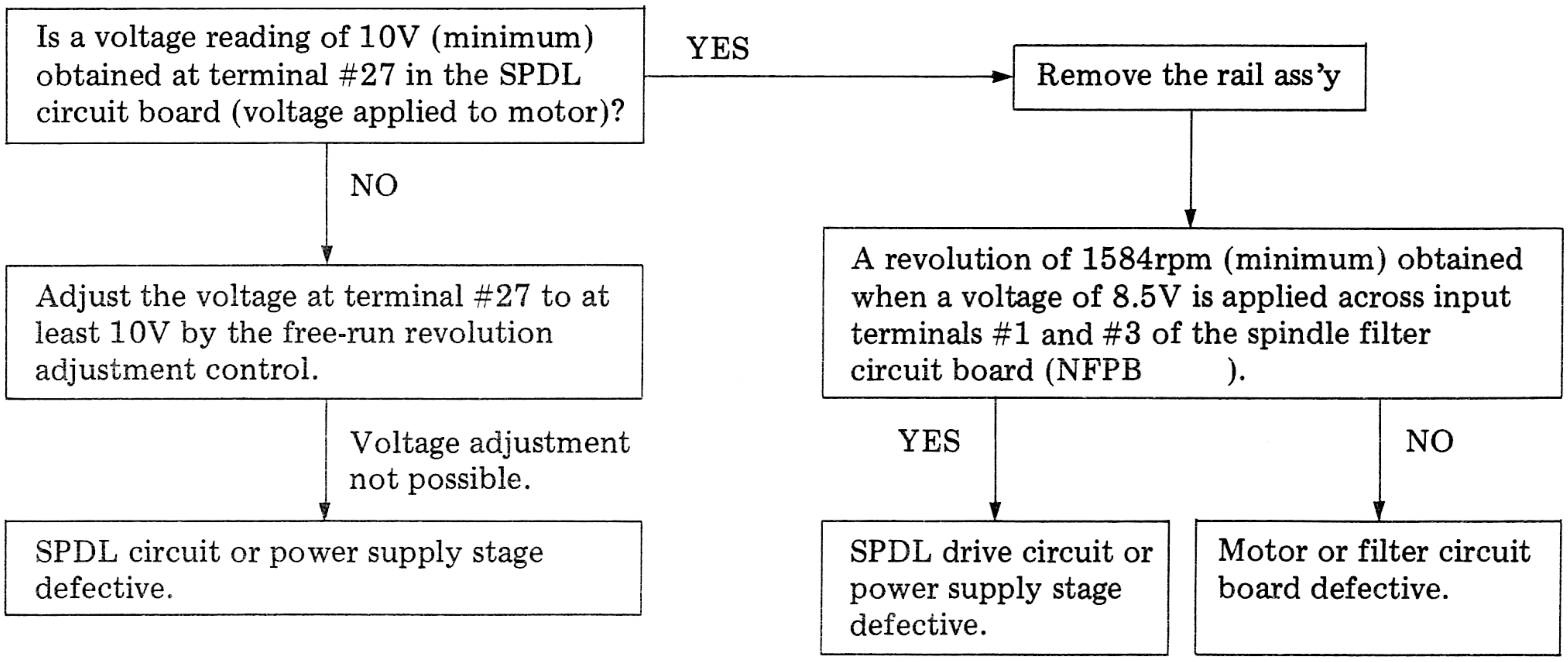
Fig. 74

Spindle Motor

14.4 SPINDLE MOTOR TROUBLESHOOTING

14.4.1 Specified rotational speed (1800rpm) not attained.

1. Set the control circuits to permit the motor to run freely (described elsewhere).
2. Mount a disc, and measure rpm by the strobescope.


Is a voltage reading of 10V (minimum) obtained at terminal #27 in the SPDL circuit board (voltage applied to motor)?
YES
Remove the rail ass'y
NO
Adjust the voltage at terminal #27 to at least 10V by the free-run revolution adjustment control.
A revolution of 1584rpm (minimum) obtained when a voltage of 8.5V is applied across input terminals #1 and #3 of the spindle filter circuit board (NFPB).
Voltage adjustment not possible.
YES
NO
SPDL circuit or power supply stage defective.
SPDL drive circuit or power supply stage defective.
Motor or filter circuit board defective.

14.4.2 Scraping noise generated from base of motor

Problem:

Slight amount of sound caused by brush and commutator rubbing.

If this sound is increased when a disc is mounted, the trouble is probably due to either of the following causes.

Causes:

- Wearing of brush and commutator.
- Commutator surface roughened by generation of sparking between brush and commutator.

Repair:

Replace motor.

Under normal operating conditions, the service life time of brush and commutator are 3000 and 8000 hours respectively.

14.4.3 A continuous rumbling noise generated

1. Generated when servo loop is on

Cause: brush "free-play" in the gap between brush holder.

Repair: although this does not constitute an actual defect, the motor should be replaced if the noise is considered to be serious.

2. Constant generation when motor operating

Cause: defective ball bearings (bearings damaged by wearing, shock, or foreign matter inclusions).

Repair: replace motor.

Ball bearing service life in this motor under normal operating conditions is at least 800,000 hours.

3. Occasional knocking noise generated

Cause: defective ball bearings.

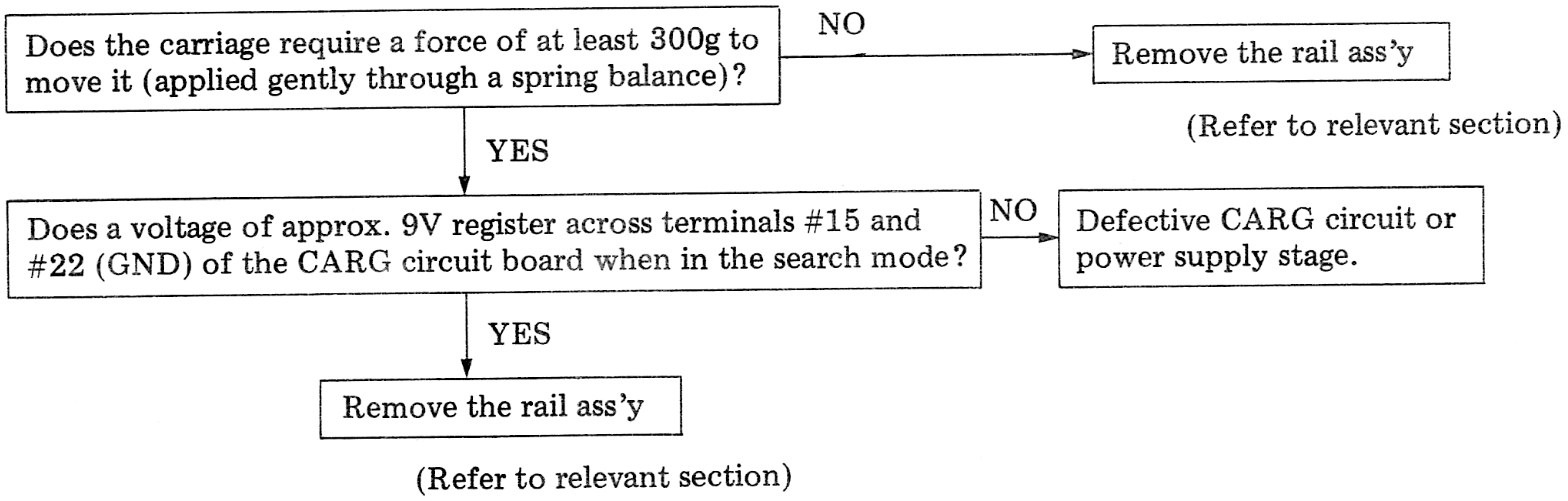
Repair: replace motor.

14.5 CARRIAGE MOTOR TROUBLESHOOTING

14.5.1 In normally assemblied condition

a. Carriage fails to move

- First check that the carriage lock screw is released.



Does the carriage require a force of at least 300g to move it (applied gently through a spring balance)?

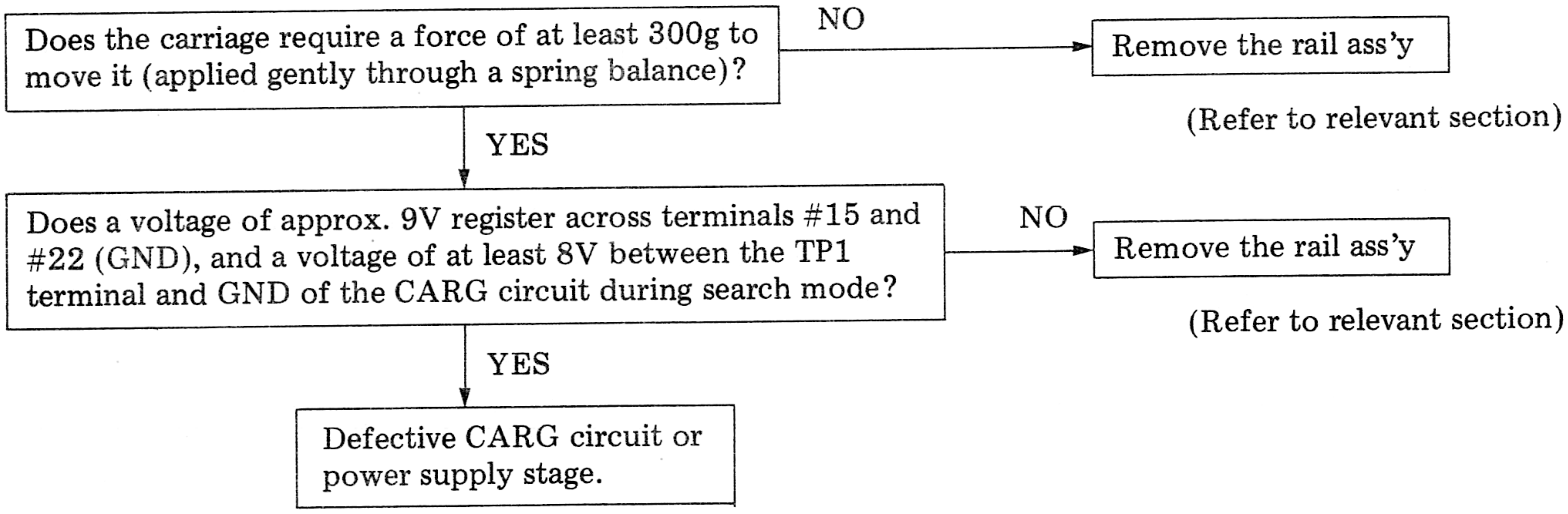
NO → Remove the rail ass'y (Refer to relevant section)

YES → Does a voltage of approx. 9V register across terminals #15 and #22 (GND) of the CARG circuit board when in the search mode?

NO → Defective CARG circuit or power supply stage.

YES → Remove the rail ass'y (Refer to relevant section)

b. Unstable carriage movement



Does the carriage require a force of at least 300g to move it (applied gently through a spring balance)?

NO → Remove the rail ass'y (Refer to relevant section)

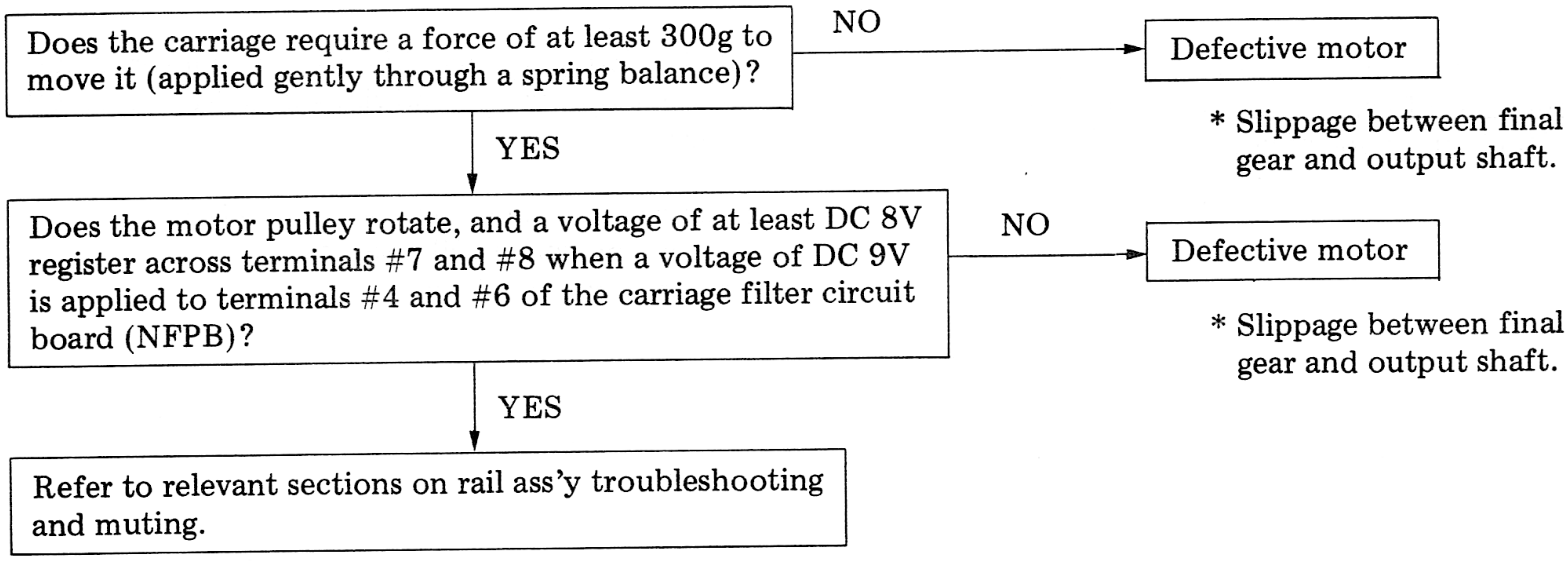
YES → Does a voltage of approx. 9V register across terminals #15 and #22 (GND), and a voltage of at least 8V between the TP1 terminal and GND of the CARG circuit during search mode?

NO → Remove the rail ass'y (Refer to relevant section)

YES → Defective CARG circuit or power supply stage.

14.5.2 As rail ass'y

- Check for possible severed or loose carriage wire and loose motor pulley securing screws.



Does the carriage require a force of at least 300g to move it (applied gently through a spring balance)?

NO → Defective motor

* Slippage between final gear and output shaft.

YES → Does the motor pulley rotate, and a voltage of at least DC 8V register across terminals #7 and #8 when a voltage of DC 9V is applied to terminals #4 and #6 of the carriage filter circuit board (NFPB)?

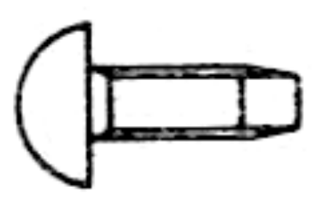
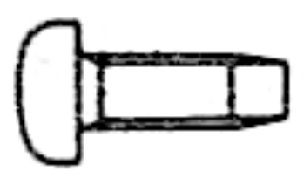
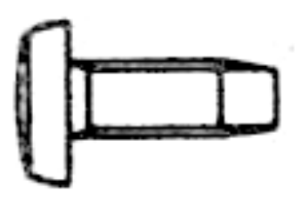
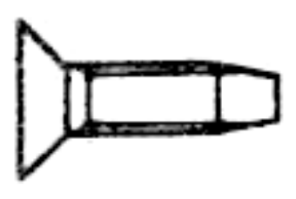
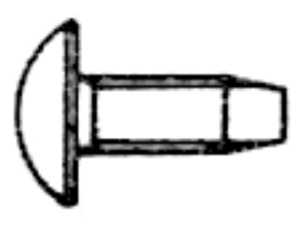
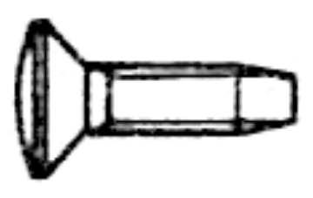
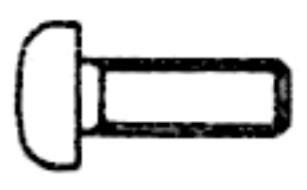
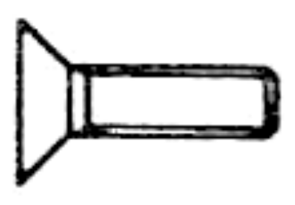
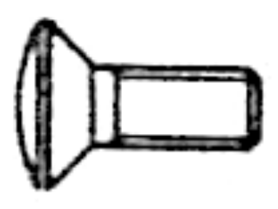
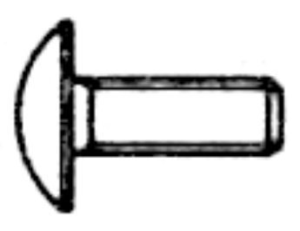
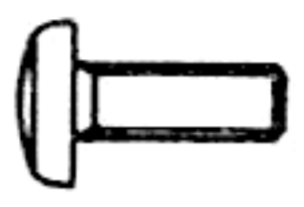
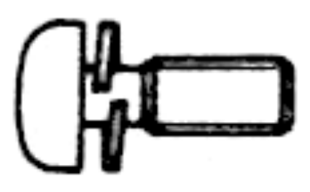
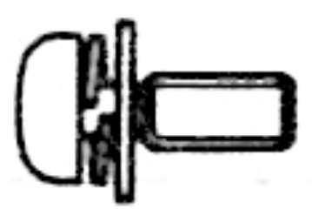
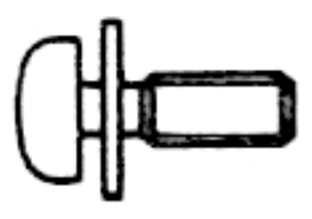
NO → Defective motor

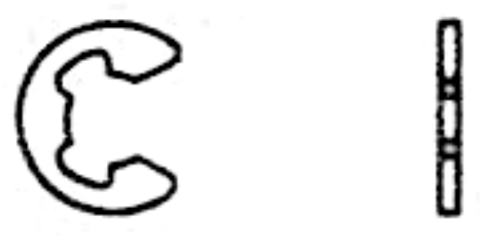
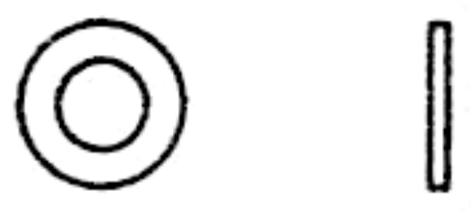
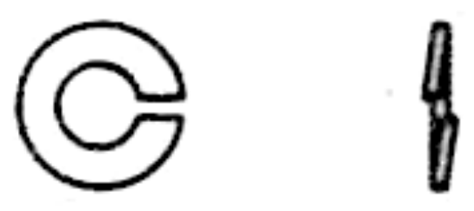
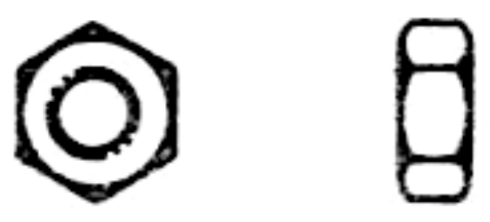
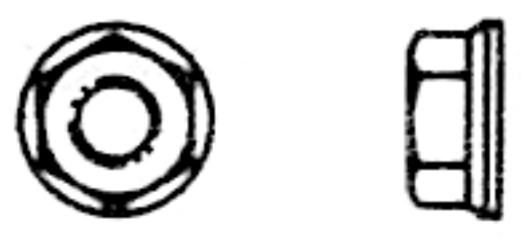
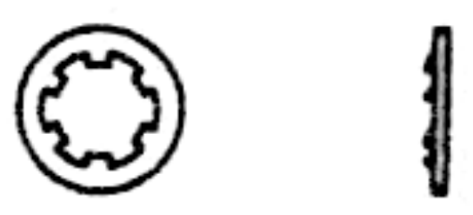
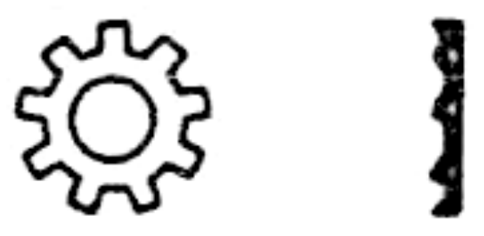
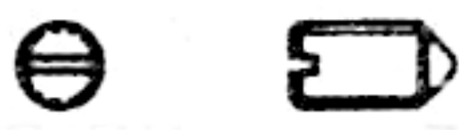
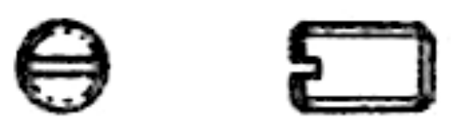
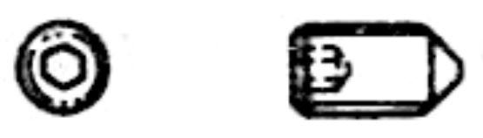
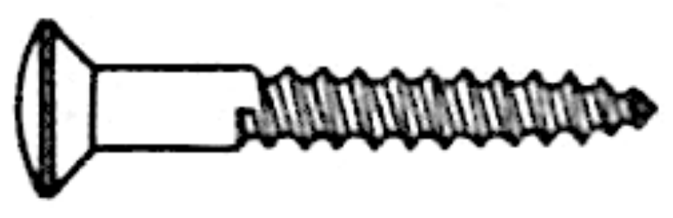
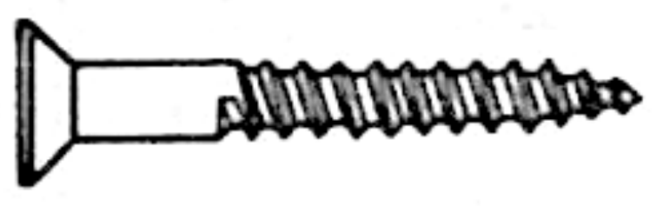
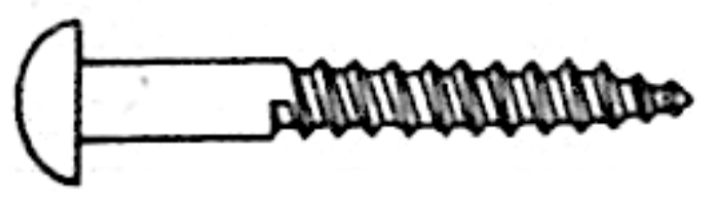
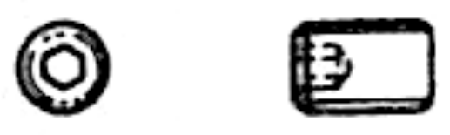
* Slippage between final gear and output shaft.

YES → Refer to relevant sections on rail ass'y troubleshooting and muting.

15. NOMENCLATURE OF SCREWS, WASHERS AND NUTS

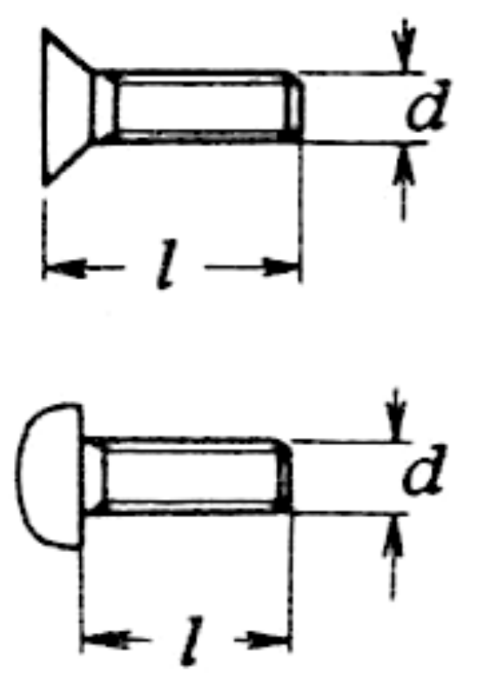
The following symbols stand for screws, washers and nuts as shown in exploded view.

Symbol	Description	Shape
RT	Brazier head taptite C screw VTZ 40 P080FZK	
PT	Pan head tapping screw	
BT	Binding head tapping screw	
CT	Countersunk head tapping screw	
TT	Truss head tapping screw	
OCT	Oval countersunk head tapping screw	
PM	Pan head machine screw	
CM	Countersunk head machine screw	
OCM	Oval countersunk head machine screw	
TM	Truss head machine screw	
BM	Binding head machine screw	
PSA	Pan head screw with spring lock washer	
PSB	Pan head screw with spring lock washer and flat washer	
PSF	Pan head screw with flat washer	

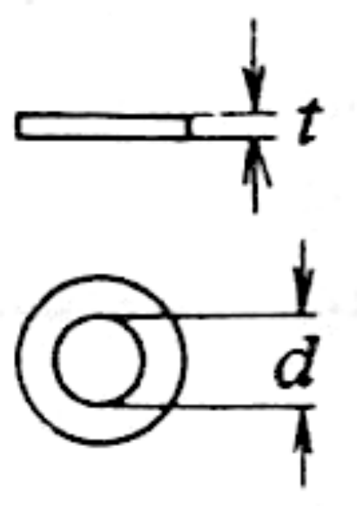
Symbol	Description	Shape
EW	E type washer	
FW	Flat washer	
SW	Spring lock washer	
N	Nut	
WN	Washer faced nut	
ITW	Internal toothed lock washer	
OTW	Outernal toothed lock washer	
SC	Slotted set screw (Cone point)	
SF	Slotted set screw (Flat point)	
HS	Hexagon socket headless set screw (Cone point)	
OCW	Oval countersunk head wood screw	
CW	Countersunk head wood screw	
RW	Round head wood screw	
HSF	Hexagon socket set screw (Flat point)	

EXAMPLE

PM · 3x8
- length in mm (*l*)
- diameter in mm (*d*)
- Symbol



FW · 9φx1^t
- thickness in mm (*t*)
- diameter in mm (*d*)
- Symbol



16. EXPLODED VIEW AND PARTS LIST

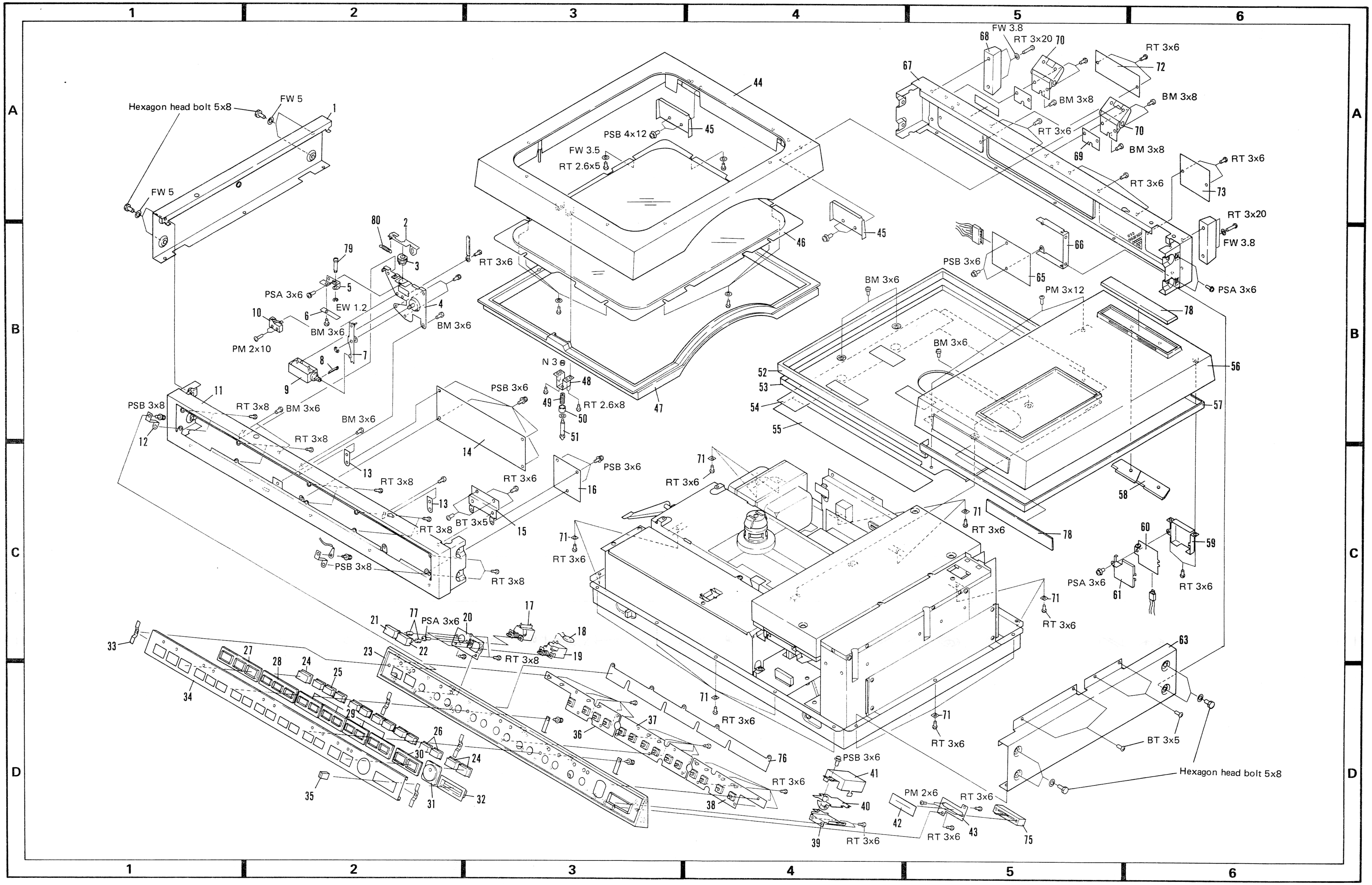
16.1 EXTERNAL

Parts List

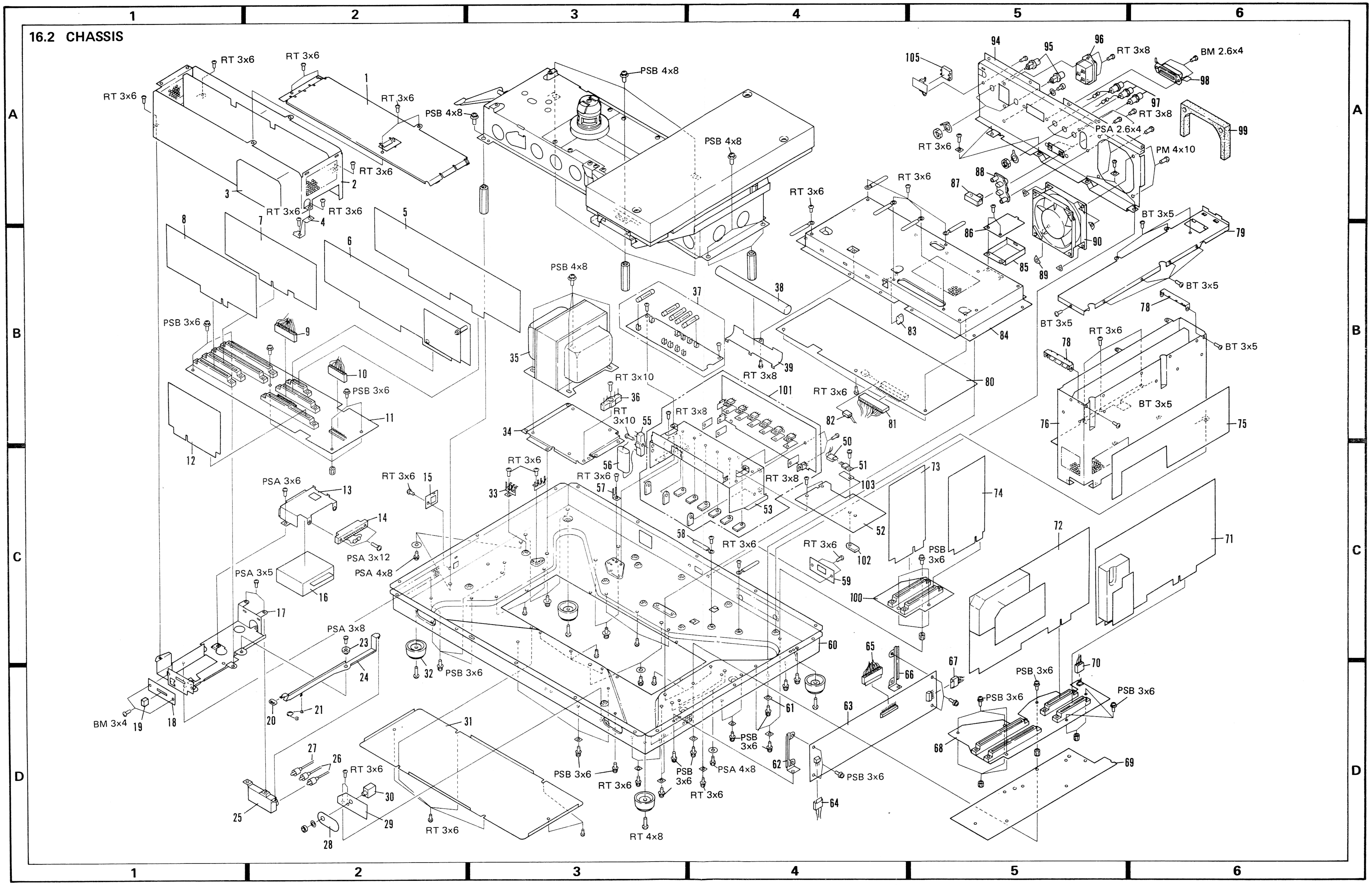
Key No.	Part No.	Description
1.	VNA-006	Side panel L
2.		Interlock
3.		Pin guide
4.		Interlock holder
5.		Door switch pin
6.	VBK-002	Door switch leaf
7.		Interlock link
8.		Pin
9.	VAC-003	Solenoid
10.	VSF-001	Microswitch
11.	VXA-022	Front panel assembly
12.		Earth spring A
13.		Plate B
14.	VWG-007	LMPD (Lamp driver board)
15.		Shield plate
16.	VWG-008	DADT (Data detector board)
17.	VSG-002	Door switch
⚠18.	VCG-002	Spark killer
⚠19.	VSA-001	Power switch
20.		Plate
21.	VAC-004	Push knob A/white
22.	VAC-005	Push knob B/blue
23.	VNK-007	Button case
24.	VAC-001	Key top A
25.	VAC-002	Key top B/white
26.	VAC-003	Key top C/blue
27.	VAP-001	Button gird A
28.	VAP-003	Button gird B
29.	VAP-002	Button gird C
30.	VAP-004	Button gird D
31.	VAP-008	I.R. filter
32.	VAP-005	Button gird E
33.		Plate
34.	VAH-001	Decoration panel
35.	VAC-006	Slide knob
36.	VWY-004	LMP1 (Lamp board 1)
37.	VWY-005	LMP2 (Lamp board 2)
38.	VWY-006	LMP3 (Lamp board 3)
39.		I.R. plate
40.	VWG-005	MIRB (Main infrated board)
41.		I.R. shield case A
42.		Mask
43.		Angle
44.	VNK-005	Hood
45.	VNE-079	Hinge plate
46.	VNK-008	Hood window
47.	VAP-006	Hood damper
48.	VNE-031	Interlock pin holder
49.	VBH-013	Interlock spring
50.	VNL-012	Interlock collar

- *Parts without part number cannot be supplied.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*

Key No.	Part No.	Description
51.	VLA-023	Interlock pin
52.	VAP-009	Rubber barrier
53.	VNA-003	Mechanical panel
54.	VEF-003	Shield sheet C
55.	VEF-002	Shield sheet B
56.	VXA-030-0	Top cover assembly
57.	VAP-007	Top cover belt
58.	VNL-001	Light acceptor
59.		Shield case A
60.	VWG-006	SIRB (Sub infrared board)
61.		Shield case B
62.		....
63.	VNA-007	Side panel R
64.		....
65.	VWV-004	ACOM (Audio compensator)
66.		Plate A
67.		Rear panel assembly
68.	VNL-002	Rear protector
69.	VNE-032	Hinge spacer
70.	VXA-031	Hinge assembly
71.	VBE-005	Nail washer
72.		Name plate A
73.		Name plate B
74.		....
75.	VCS-002	Slide volume
76.	VEF-001	Shield sheet A
77.	VBG-001	Knob spring
78.	VAM-002	Enblem
79.		Door switch pin
80.	VBH-010	Interlock holder spring


1
2
3
4
5
6
A
B
C
D
Hexagon head bolt 5x8
FW 5
1
FW 5
80
2
79
3
PSA 3x6
5
EW 1.2
4
10
6
BM 3x6
BM 3x6
PM 2x10
7
8
9
RT 3x6
44
PSB 4x12
45
FW 3.5
RT 2.6x5
46
45
47
N 3
48
49
RT 2.6x8
50
51
PSB 3x6
14
11
PSB 3x8
RT 3x8
BM 3x6
12
BM 3x6
RT 3x8
13
RT 3x8
13
RT 3x6
BT 3x5
15
16
PSB 3x6
RT 3x8
PSB 3x8
RT 3x8
68
FW 3.8
RT 3x20
70
67
RT 3x6
72
BM 3x8
BM 3x8
RT 3x6
70
69
BM 3x8
RT 3x6
RT 3x6
73
RT 3x20
FW 3.8
PSA 3x6
66
PSB 3x6
65
BM 3x6
PM 3x12
78
BM 3x6
52
53
54
55
56
57
71
RT 3x6
71
RT 3x6
78
58
71
RT 3x6
60
59
PSA 3x6
61
RT 3x6
71
RT 3x6
63
21
77
PSA 3x6
20
17
18
22
RT 3x8
19
33
27
28
24
25
23
34
29
26
30
24
35
31
32
71
RT 3x6
37
36
76
38
RT 3x6
PSB 3x6
41
40
39
RT 3x6
PM 2x6
42
RT 3x6
43
RT 3x6
75
71
RT 3x6
BT 3x5
Hexagon head bolt 5x8

16.2 CHASSIS


A
B
C
D
RT 3x6
RT 3x6
RT 3x6
RT 3x6
PSB 4x8
PSB 4x8
PSB 4x8
RT 3x6
RT 3x6
RT 3x6
RT 3x8
BM 2.6x4
RT 3x8
PSA 2.6x4
PM 4x10
RT 3x6
RT 3x6
RT 3x6
BT 3x5
BT 3x5
BT 3x5
BT 3x5
PSB 3x6
PSB 3x6
PSB 4x8
RT 3x8
RT 3x10
RT 3x10
RT 3x8
RT 3x6
RT 3x6
BT 3x5
RT 3x6
RT 3x6
RT 3x6
RT 3x8
PSA 3x6
PSA 3x12
PSA 4x8
PSA 3x5
RT 3x6
RT 3x6
PSB 3x6
PSA 3x8
PSB 3x6
PSB 3x6
PSB 3x6
PSB 3x6
BM 3x4
PSB 3x6
PSA 4x8
PSB 3x6
RT 3x6
RT 3x6
PSB 3x6
RT 3x6
PSB 3x6
RT 3x6
RT 4x8

Parts List of Chassis

- *Parts without part number cannot be supplied.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*

Key No.	Part No.	Description
1.		Shield cover
2.		Shield case
3.		Insulator
4.		Angle
5.	VWG-002	DSPL (Character display)
6.	VWW-004	MCPR (Micro precessor assembly)
7.	VWG-003	D & CR (Data & clock recovery)
8.	VWG-004	STPM (Stop motion)
9.		Connector
10.		Connector
11.	VWX-001	COMB (Control mother board)
12.	VWS-003	CARG (Carriage servo assembly)
13.		RF housing
14.	VKD-005	PC Board connector S 10p
15.		RF name plate
16.	VWL-001	RFMD (RF modulator)
17.		Base
18.		Name plate
19.	VAC-006	Antenna switch knob
20.		Rubber tube
21.	VBH-014	Antenna switch spring
22.		....
23.		Collar
24.		Lever
25.	VSH-003	Switch box
26.		Pin plug assembly B
27.		Pin plug assembly A
28.		Remote name plate
29.		Holder
30.	VKN-010	Remote control jack
31.		Bottom plate
32.	VNL-006	Foot
33.		4P earth lug terminal
34.		Plate
⚠35.	VTT-001/VTT-002	Power transformer
36.		....
37.	VWR-004	FFMP (Fuse & Focus motor protector)
38.	VEM-001/VEM-007	Ni-Cd Dry battery
39.		Holder
40.		....
50.		Housing assembly G
51.	2SD 635	Transistor
52.		Heat sink
53.		Heat sink
54.		....
55.		2P terminal

Key No.	Part No.	Description
56.	VCG-010	Capacitor
57.		2P earth lug terminal
58.	VNF-005	Cord cramper
59.		Name plate
60.		Buttom plate assembly
61.	VBE-005	Nail washer
62.		Angle
63.	VWV-003	AUDB (Audio board assembly)
64.		Connector
65.		Connector
66.		Angle
67.		Connector
68.	VWX-003	CLMB (VTBC & Spindle mother board)
69.	VEF-007	Shield sheet G
70.		Connector
71.	VWW-002	SPDL (Spindle servo assembly)
72.	VWW-003	VTBC (Video time base corrector)
73.	VWS-002	TRKG (Tracking servo assembly)
74.	VWS-001	FOCS (Focus servo assembly)
75.		Insulator
76.		Shield case
77.		....
78.	VNE-051	PCB holder
79.		Shield cover
80.	VWV-002	VDEM (Video demodulator)
81.		Connector
82.		Connector
83.		Rubber tube
84.		Case
85.		Case
86.	VWR-003	CUST (Current stabilizer)
87.	VSH-002	Slide switch
88.	VKB-001	2P pin jack
89.	VNE-052	Fan motor nut
90.	VXM-005	Fan motor
91.		....
92.		....
93.		
94.		Rear terminal board
95.	VKN-008	F-type connector
⚠96.	VKP-001	3P inlet
97.	VKN-007	BNC connector
98.	VKN-009	Receptacle
99.	VED-004	Fan motor cushion
100.	VWX-002	FTMB (Focus & tracking mother board)
101.	VWR-001	SYPS (System power supply)
102.	VKH-001	Transistor socket
103.	VEC-002	Mica insulator
104.	VSG-001	Switch

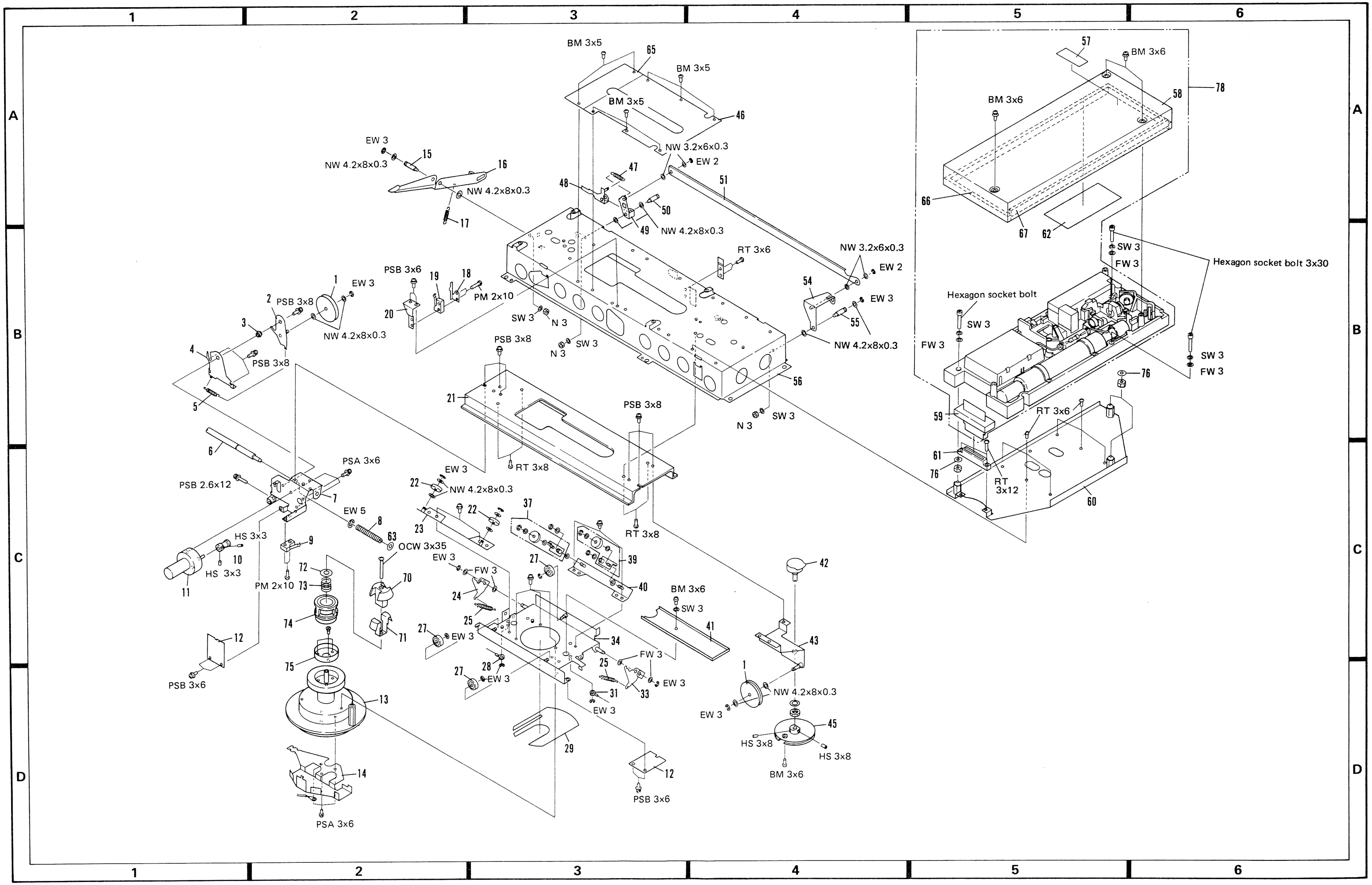
16.3 CARRIGE

Parts List

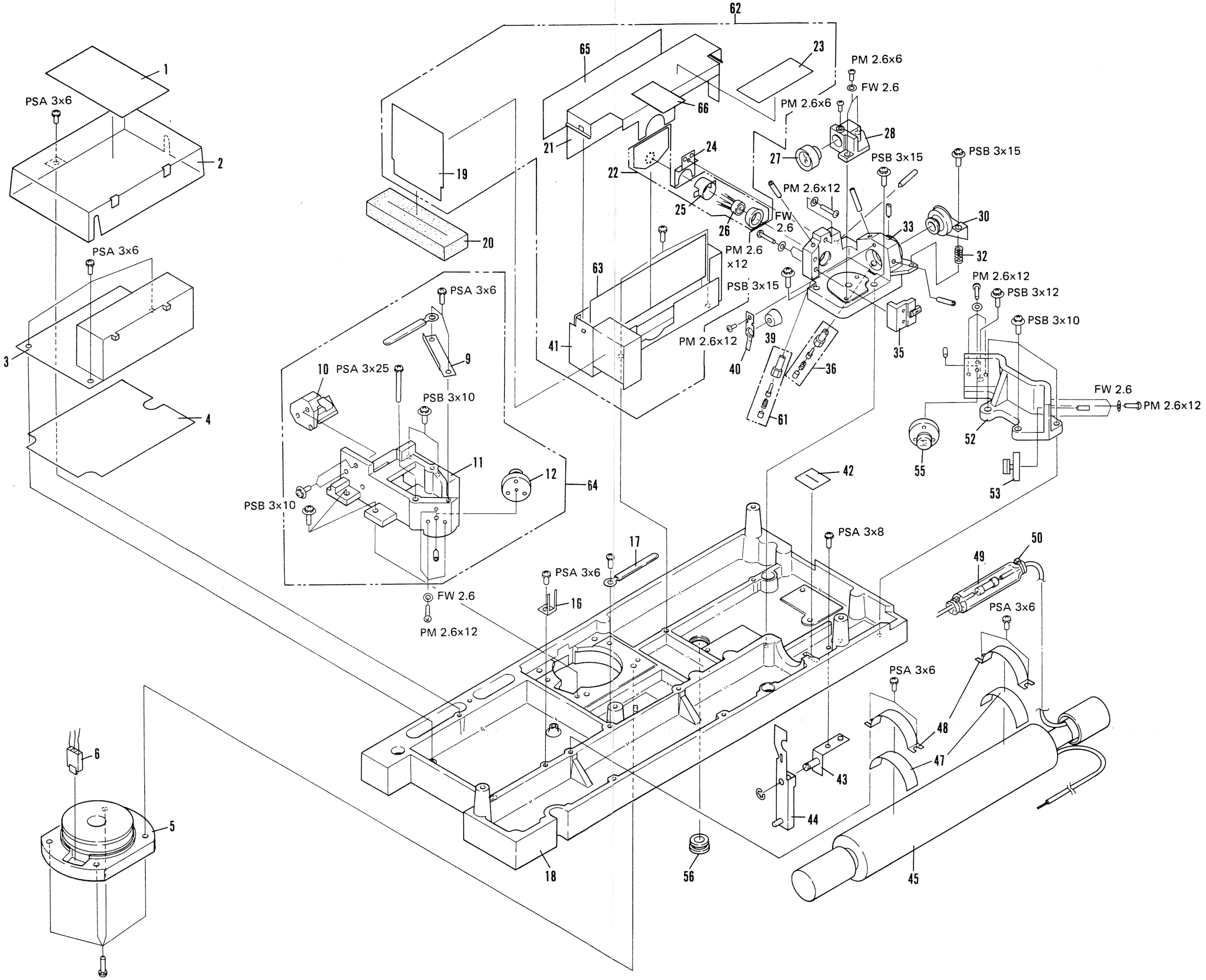
- *Parts without part number cannot be supplied.*

Key No.	Part No.	Description
1.	VNL-009	Wire roller
2.		Plate
3.		Collar
4.		Plate
5.	VBH-006	Wire roller spring
6.		Carriage stopper
7.		Motor holder
8.		Spring
9.	VSF-001	Microswitch
10.	VLA-018	Motor pulley
11.	VXM-002	Carriage motor
12.	VWY-003	NFPB (Noise filter printed board)
13.	VXM-006	Spindle motor assembly
14.		Cord cover
15.		Pin
16.		Beam shutter link A
17.	VBH-008	Beam shutter spring A
18.	VBK-005	Microswitch leaf
19.	VSF-001	Microswitch
20.		Plate
21.		Rail
22.	VNL-007	Lead roller A
23.		Plate
24.		Angle
25.	VBH-017	Carriage spring
26.		....
27.	VXA-019	Lead roller
28.		....
29.		Spacer
30.		....
31.	VXA-020	Wire
32.		....
33.		Angle
34.		Carriage assembly
35.		....
36.		....
37.	VXA-008	Roller arm R assembly
38.		....
39.	VXA-009	Roller arm L assembly
40.		Plate
41.	VNA-014	Blind
42.	VCS-001	Potentiometer
43.		Angle
44.		....
45.	VNL-010	Potentiometer pulley
46.	VNA-012	Top blind A
47.	VBH-009	Beam shutter spring B
48.		Beam shutter link B
49.		Beam shutter link C
50.		Pin

Key No.	Part No.	Description
51.		Beam shutter link D
52.		....
53.		....
54.		Beam shutter link E
55.		Pin
56.		Chassis
57.		Caution label
58.		PF cover
59.		PFCB
60.		Base
61.	VKD-006	P.C. Board connector
62.		Amp barrier B
63.		Washer
64.		....
65.	VNA-013	Top blind B
66.	VEC-006	Cover packing L
67.	VEC-007	Cover packing S
70.	VNL-015-0	Stopper
71.	VNL-014-0	Retainer
72.	VNE-080	Washer
73.	VBH-020	Spring
74.	VXX-002	Clamper
75.	VXX-003	Rubber plate assembly
76.	VBE-006	Height adjust washer 0.1 mm
	VBE-007	Height adjust washer 0.2 mm
	VBE-008	Height adjust washer 0.5 mm
	VBE-009	Height adjust washer 1.0 mm
77.		....
78.	VGX-012	Platform assembly


1
2
3
4
5
6
A
B
C
D
BM 3x5
65
BM 3x5
BM 3x5
46
NW 3.2x6x0.3
EW 2
51
47
48
50
49
NW 4.2x8x0.3
EW 3
15
NW 4.2x8x0.3
16
NW 4.2x8x0.3
17
57
BM 3x6
78
58
BM 3x6
66
67
62
SW 3
FW 3
Hexagon socket bolt 3x30
Hexagon socket bolt
SW 3
FW 3
SW 3
FW 3
76
59
RT 3x6
61
76
RT
3x12
60
RT 3x6
NW 3.2x6x0.3
EW 2
54
EW 3
55
NW 4.2x8x0.3
56
PSB 3x6
19
18
20
PM 2x10
SW 3
N 3
PSB 3x8
SW 3
N 3
1
EW 3
2
PSB 3x8
NW 4.2x8x0.3
3
4
PSB 3x8
5
21
PSB 3x8
SW 3
N 3
RT 3x8
6
PSA 3x6
PSB 2.6x12
7
EW 3
22
NW 4.2x8x0.3
23
22
37
RT 3x8
EW 5
8
63
OCW 3x35
HS 3x3
9
10
HS 3x3
11
PM 2x10
72
73
74
70
71
EW 3
FW 3
24
25
27
27
39
40
42
BM 3x6
SW 3
41
43
34
27
EW 3
12
PSB 3x6
75
13
28
EW 3
27
FW 3
25
EW 3
31
33
EW 3
1
NW 4.2x8x0.3
EW 3
45
HS 3x8
HS 3x8
BM 3x6
29
12
PSB 3x6
14
PSA 3x6

16.4 PLATFORM



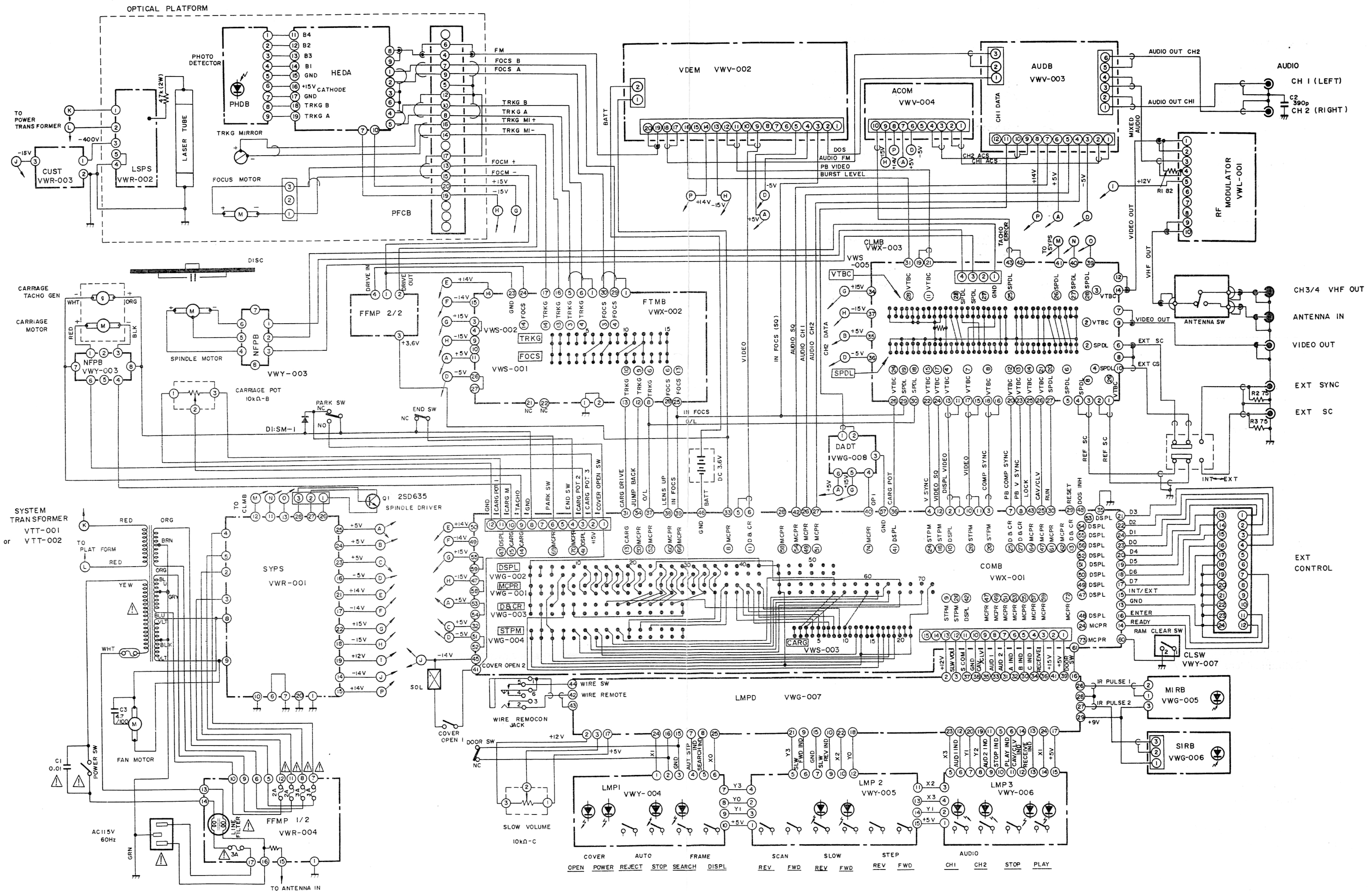
Parts List of Platform

- *Parts without part number cannot be supplied.*

Key No.	Part No.	Description
1.	VRW-002	Voltage label
2.	VNH-005	Power supply cover
3.	VWR-002	Laser power supply
4.	VEC-008	Barrier
5.	VXV-002	Focus motor
6.		Housing assembly
7.		....
8.		....
9.		Plate
10.	VXT-003	Mirror transducer
11.		Base
12.	VGX-004	Mirror L assembly
13.		....
14.		....
15.		....
16.		2P earth terminal
17.	VNF-005	Cord clamper
18.		Base
19.		PFCB
20.	VEC-005	Connector packing
21.		Head amp case top
22.		PHDB
23.		Cushion label
24.		PD plate
25.		PD sleeve
26.	F4001	Photo diode
27.	VGX-006	¼ wave plate assembly
28.	VGX-005	Prism assembly
29.		....
30.	VGX-009	Grating assembly
31.		....
32.	VBH-002	Arm spring
33.	VNT-004	Optical support
34.		....
35.	VGX-010	Sylindlical lens assembly
36.	VGX-008	DG nut assembly
37.		....
38.		....
39.	VGX-007	DG lens assembly
40.	VLA-011	DG stopper
41.		Head amp case
42.	VED-007	Shutter mask
43.		Laser shutter stey
44.		Laser shutter assembly
45.	VGN-004/VGN-005	Laser tube
46.		....
47.	VED-003	Tube cushion
48.	VNE-008	Tube holder
49.	VDM-001	Insulator tube
50.	VEC-004	Binder
51.		....
52.	VNT-003	Fixed mirror base
53.	VGX-002	Mirror S assembly
54.		....
55.	VGX-002	Mirror S assembly
56.	VEB-003	Cap mask
57.		....
58.		....
59.		....
60.		....
61.	VGX-011	PD nut assembly
62.	VWW-001	Head amp assembly
63.		HEDA (Head amp)
64.	VGX-003	Tracking assembly
65.	VEF-005	Shield sheet E

17. SCHEMATIC DIAGRAM, P.C. BOARD PATTERNS AND PARTS LIST

17.1 CONNECTION DIAGRAMS



NOTE:

- *When ordering resistors, first convert resistance values into code form as shown in the following examples.*

Ex. 1 *When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J = 5%, and K = 10%).*

560Ω——56 ×10^1——561 .... RD¼PS $\boxed{5}\boxed{6}\boxed{1}$ *J*
47kΩ——47 ×10^3——473 .... RD¼PS $\boxed{4}\boxed{7}\boxed{3}$ *J*
0.5Ω——0R5 .... RN2H $\boxed{0}\boxed{R}\boxed{5}$ *K*
1Ω——010 .... RS1P $\boxed{0}\boxed{1}\boxed{0}$ *K*

Ex. 2 *When there are 3 effective digits (such as in high precision metal film resistors).*

5.62kΩ 562 × 10^1 5621.......... RN¼SR $\boxed{5}\boxed{6}\boxed{2}\boxed{1}$ *F*

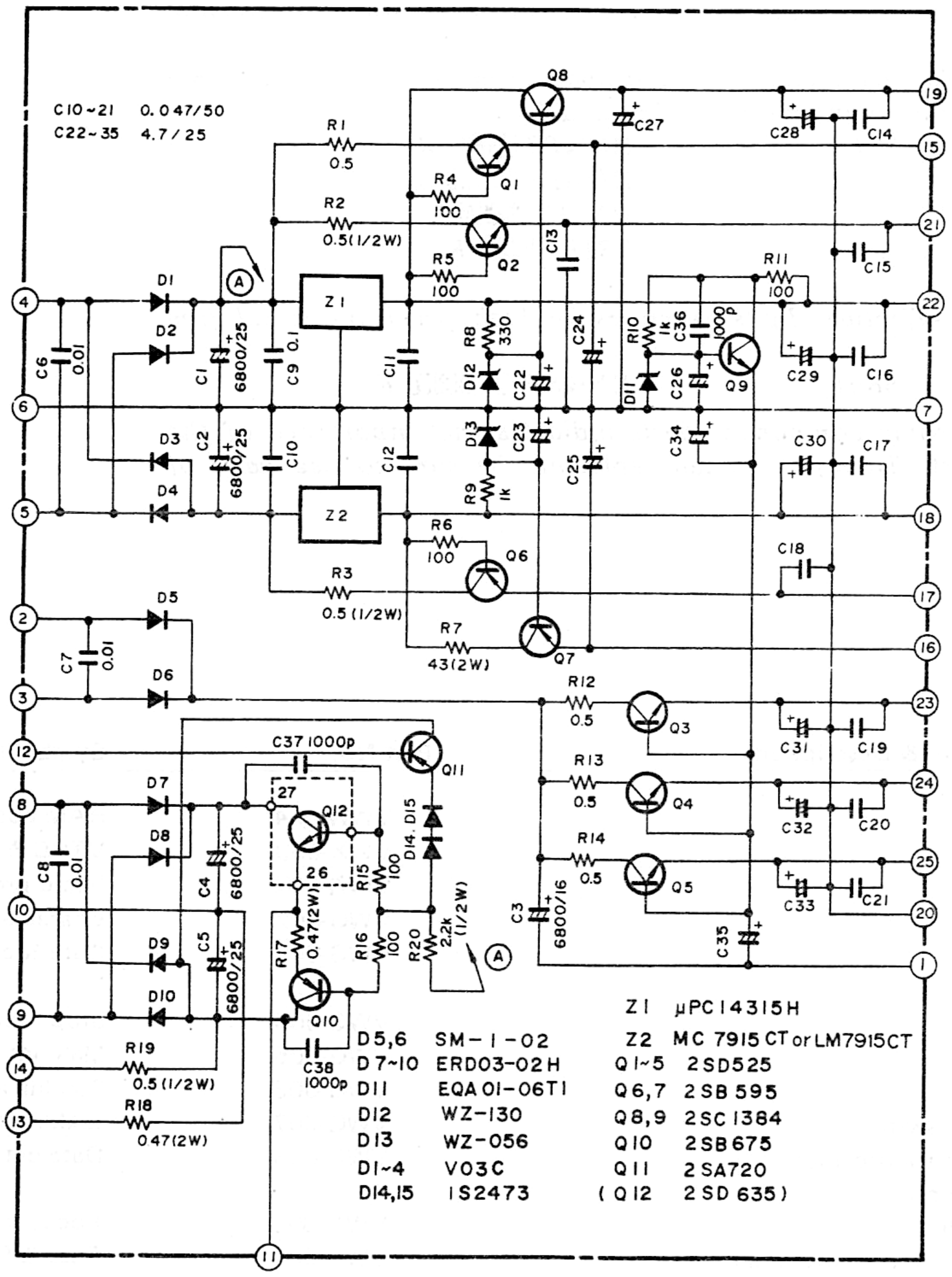
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*

Miscellaneous Parts

Part No.	Symbol & Description
VCG-002	C1
CCDSL391K 50	C2
VCG-010	C3
RD¼PS 820J	R1
RD¼PS 750J	R2, R3
2SD635	Q1
⚠ VSA-001	Power switch
⚠ VTT-001 or VTT-002	Power transformer
VXM-005	Fan motor
⚠ VKP-001	3P inlet
VXM-006	Spindle motor assembly
VXM-002	Carriage motor
VWR-001	System power supply assembly
VWR-002	Laser power supply assembly
VWR-003	Current stabilizer assembly
VWW-001	Head amplifier assembly
VWW-001	Platform connector board assembly
VWW-001	Photo detector board assembly
VWY-004	LAMP board 1 assembly
VWY-005	LAMP board 2 assembly
VWY-006	LAMP board 3 assembly
VWX-001	Control mother board assembly

Part No.	Symbol & Description
VWW-004	RAM board assembly
VWX-003	VTBC & SPDL mother board assembly
VWW-004	Micro processor assembly
VWG-002	Character display assembly
VWG-003	Data & clock recovery assembly
VWG-004	Stop motion assembly
VWG-005	Main infrared board assembly
VWG-006	Sub infrared board assembly
VWG-007	LAMP driver board assembly
VWG-008	Data detector board assembly
VWX-002	Focus & tracking mother board assembly
VWR-004	Fuse & focus motor protector assembly
VWY-003	Noise filter printed board assembly
VWV-003	Audio board assembly
VWV-002	Video demodulator assembly
VWV-004	Audio compensator assembly
VWS-001	Focus servo assembly
VWS-002	Tracking servo assembly
VWS-003	Carriage servo assembly
VWW-003	Video & time base corrector-A assembly
VWW-002	Spindle servo assembly

17.2 SYSTEM POWER SUPPLY ASSEMBLY (VWR-001) (SYPS)



Parts List

SEMICONDUCTORS

Part No.	Symbol & Description
μPC14315H	Z1
MC7915CT	Z2
(LM7915CT)	
2SA720-R or Q	Q11
2SD525-Y or O	Q1–Q5
2SB595-Y or O	Q6, Q7
2SC1384-R or Q	Q8, Q9
2SB675	Q10
1S2473	D14, D15
SM-1-02	D5, D6
ERD03-02H	D7–D10
V03C	D1–D4
EQA01-06TI	D11
WZ-130	D12
WZ-056	D13

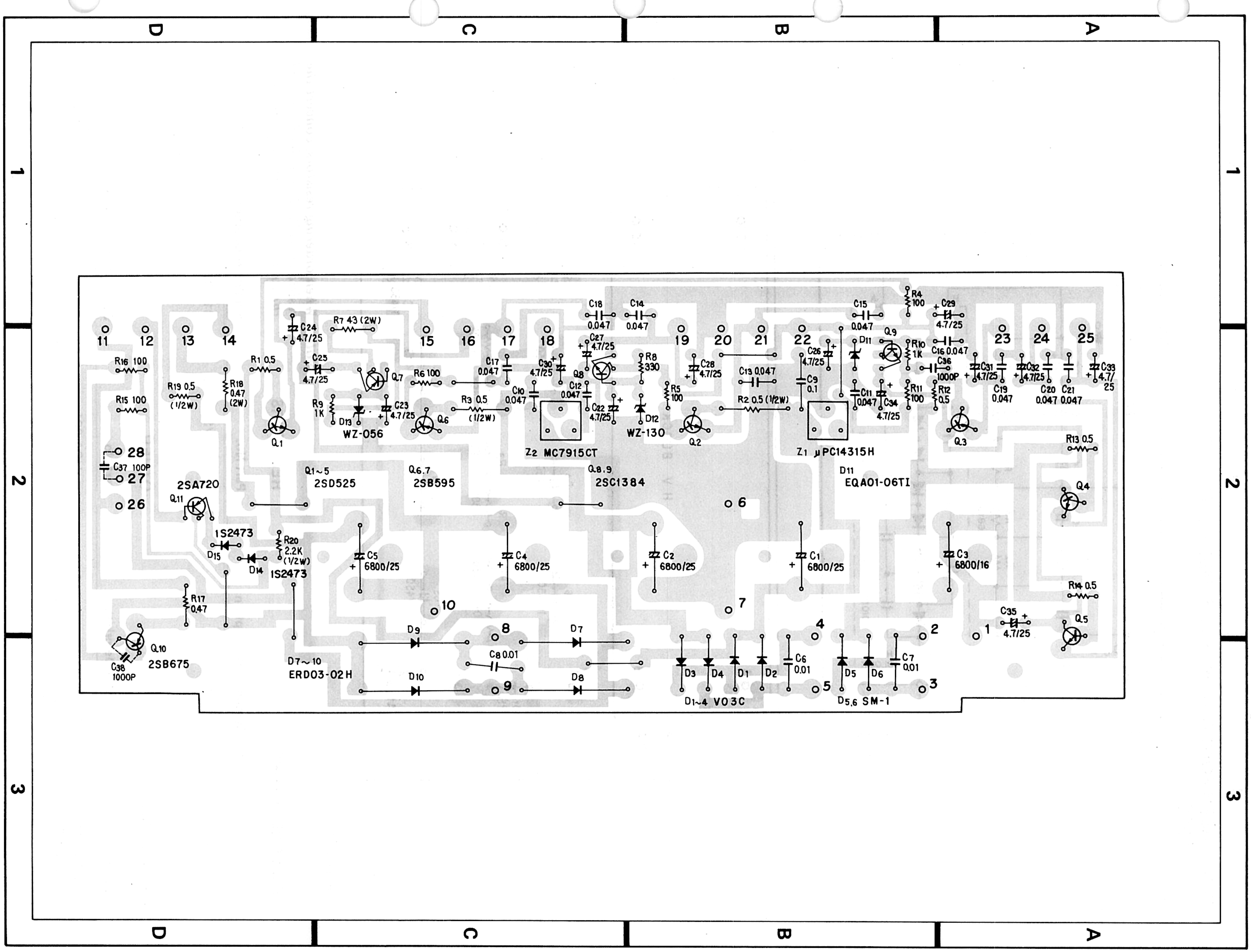
CAPACITORS

Part No.	Symbol & Description
VCH-001	C1, C2, C4, C5
VCH-002	C3
VCG-002	C6–C8
CKDYF 104Z 50	C9
CKDYF 473Z 50	C10–C21
CKDYB102K 50	C36, C37, C38
CEA 4R7P 25	C22–C35

Note: *When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.*

RESISTORS

Part No.	Symbol & Description
RD¼VS □R5J	R1, R4–R6, R8–R16, R20
RD½PS □R5J	R2, R3, R19
VCN-001	R17, R18
VCN-002	R7


D
C
B
A
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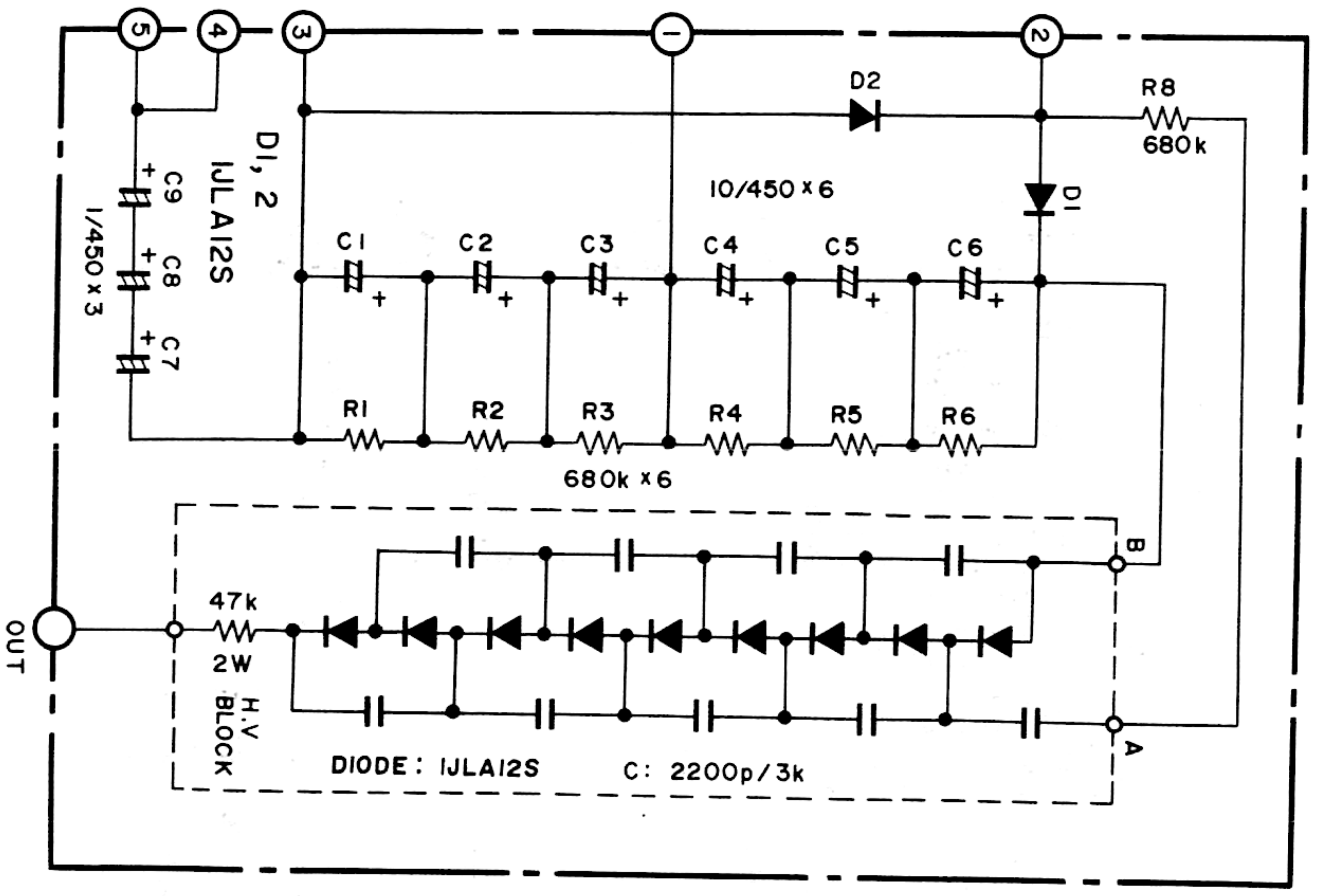
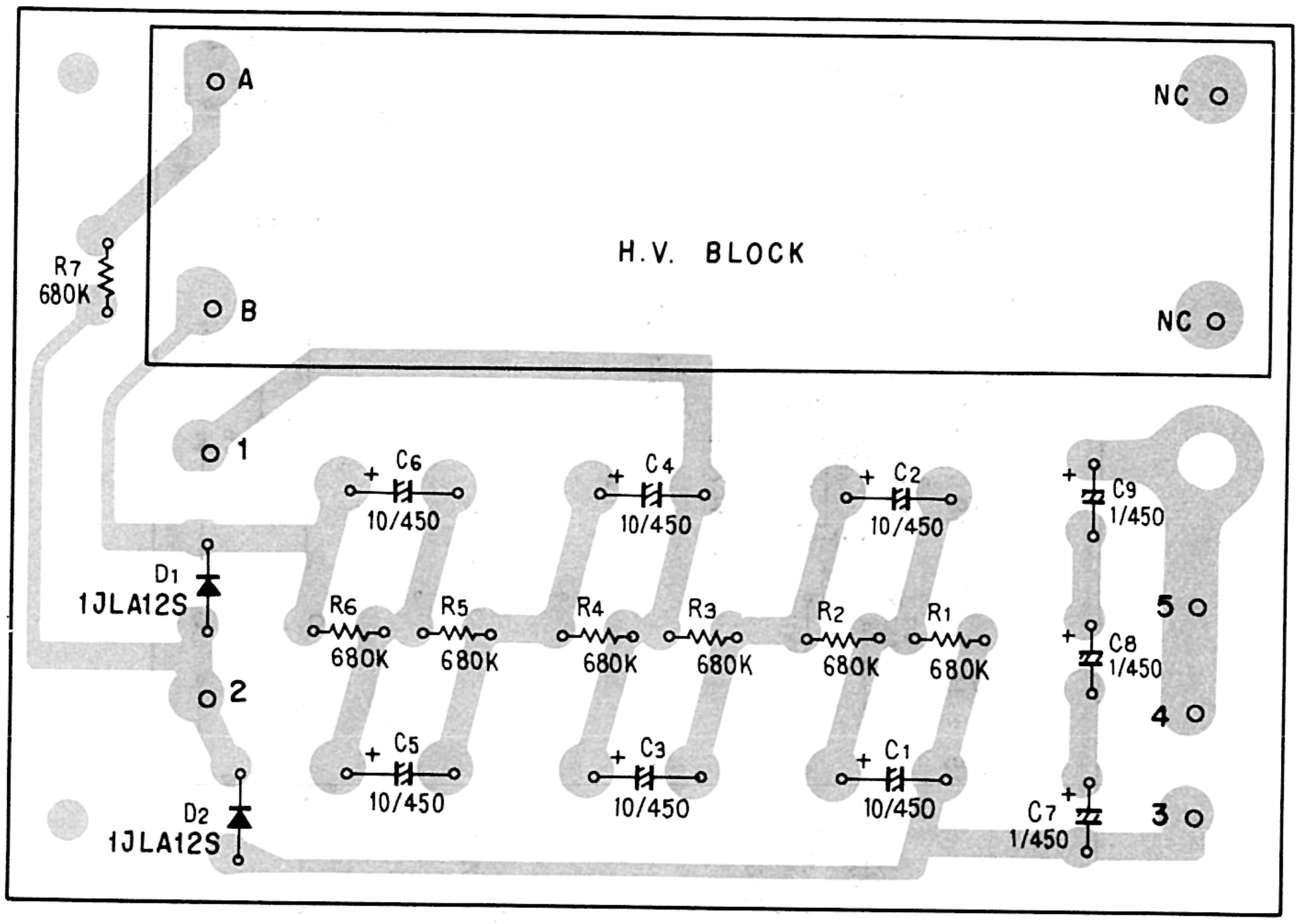
18
19
20
21
22
23
24
25
26
27
28
1
2
3
4
5
6
7
8
9
10
R16 100
R15 100
R19 0.5 (1/2W)
R18 0.47 (2W)
R1 0.5
C24 4.7/25
C25 4.7/25
R7 43 (2W)
Q7
R9 1K
D13
C23 4.7/25
WZ-056
Q6
R6 100
R3 0.5 (1/2W)
C17 0.047
C10 0.047
C30 4.7/25
C18 0.047
C14 0.047
C27 4.7/25
Q8
C12 0.047
C22 4.7/25
R8 330
D12
WZ-130
R5 100
C28 4.7/25
C13 0.047
R2 0.5 (1/2W)
C26 4.7/25
C9 0.1
C15 0.047
D11
Q9
R4 100
C29 4.7/25
R10 1K
C16 0.047
C36 1000P
C11 0.047
C34 4.7/25
R11 100
R12 0.5
C31 4.7/25
C19 0.047
C32 4.7/25
C20 0.047
C21 0.047
C33 4.7/25
Q1
Q2
Q3
Z2 MC7915CT
Z1 μPC14315H
C37 100P
2SA720
Q11
Q1~5 2SD525
Q6.7 2SB595
Q8.9 2SC1384
D11 EQA01-06TI
R13 0.5
Q4
1S2473
D15
R20 2.2K (1/2W)
D14
1S2473
C5 6800/25
C4 6800/25
C2 6800/25
C1 6800/25
C3 6800/16
R14 0.5
R17 0.47
Q10
C38 1000P
2SB675
D7~10 ERD03-02H
D9
D7
C8 0.01
D10
D8
D3
D4
D1
D2
C6 0.01
D1~4 V03C
D5
D6
C7 0.01
D5,6 SM-1
C35 4.7/25
Q5

17.3 LASER POWER SUPPLY ASSEMBLY (VWR-002) (LSPS)





Parts List

Note: When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

SEMICONDUCTORS

Part No.	Symbol & Description
1JLA12S	D1, D2

RESISTORS

Part No.	Symbol & Description
RD¼VS □□□J	R1–R7

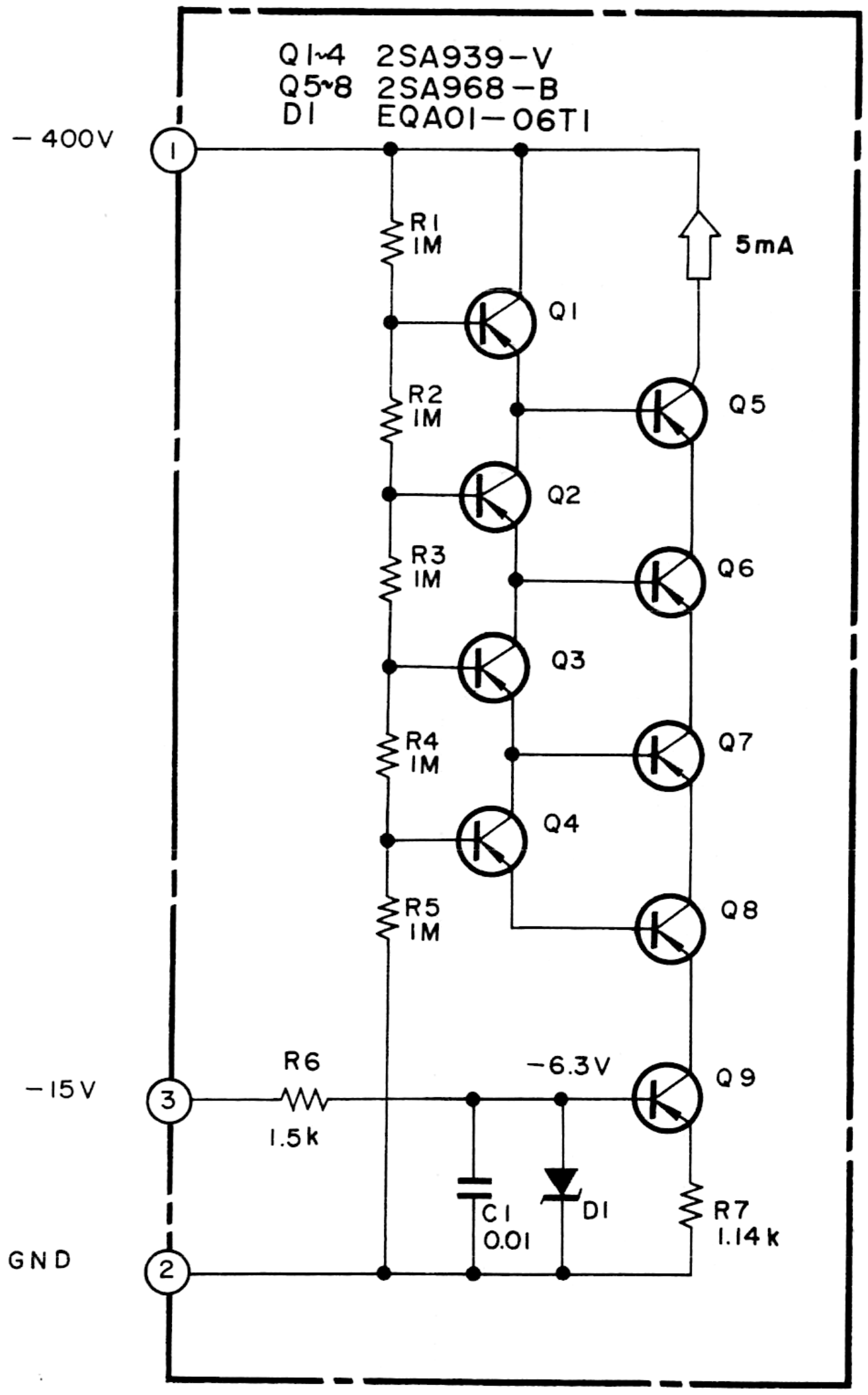
CAPACITORS

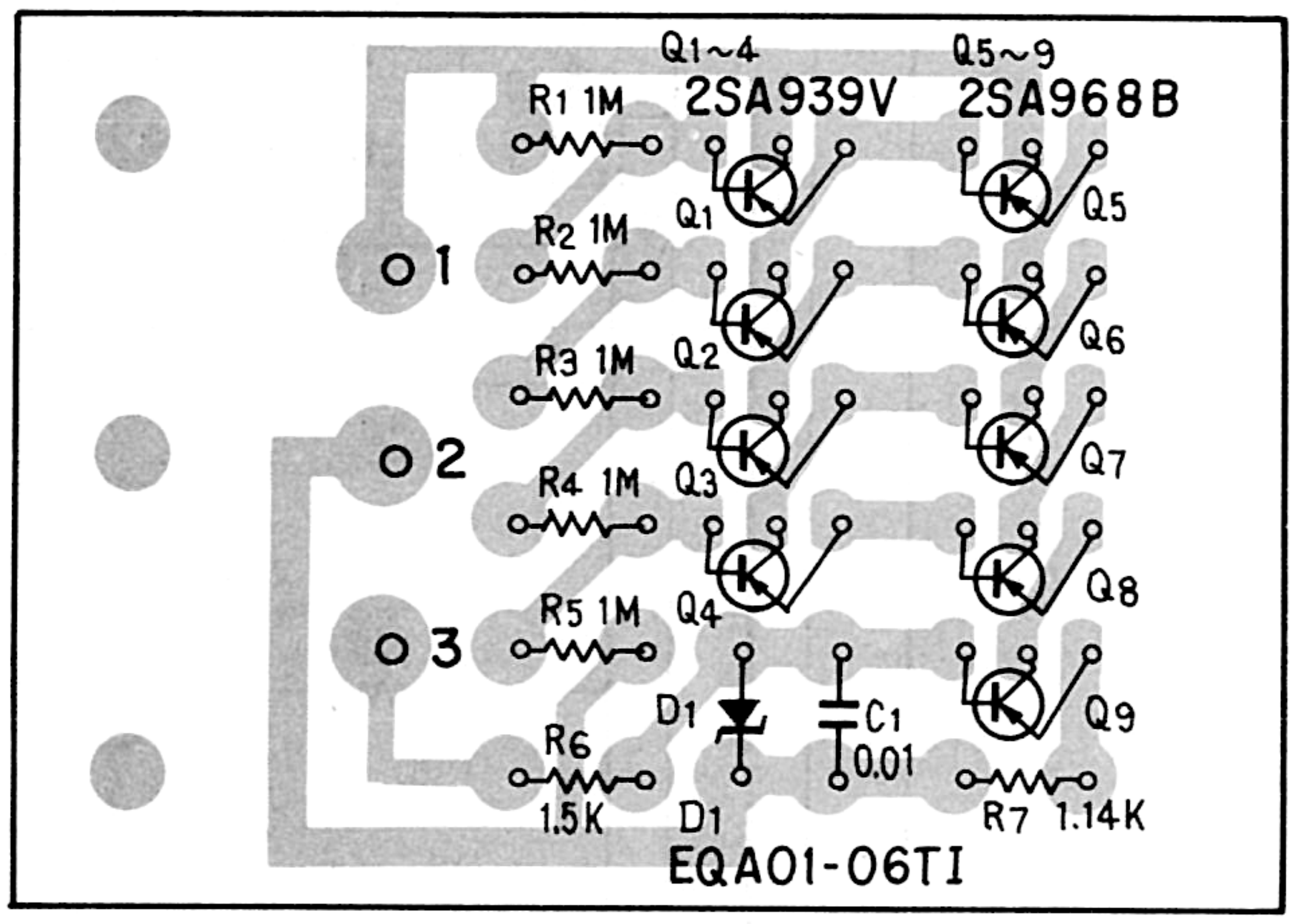
Part No.	Symbol & Description
VCH-003	C1–C6
CEA 010P 450	C7–C9

OTHER

Part No.	Symbol & Description
VCA-001	

17.4 CURRENT STABILIZER ASSEMBLY (VWR-003) (CUST)





Parts List

Note: When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

SEMICONDUCTORS

Part No.	Symbol & Description
2SA939-V or B	Q1–Q4
2SA968B-O or Y	Q5–Q9
EQA01-06TI	D1

RESISTORS

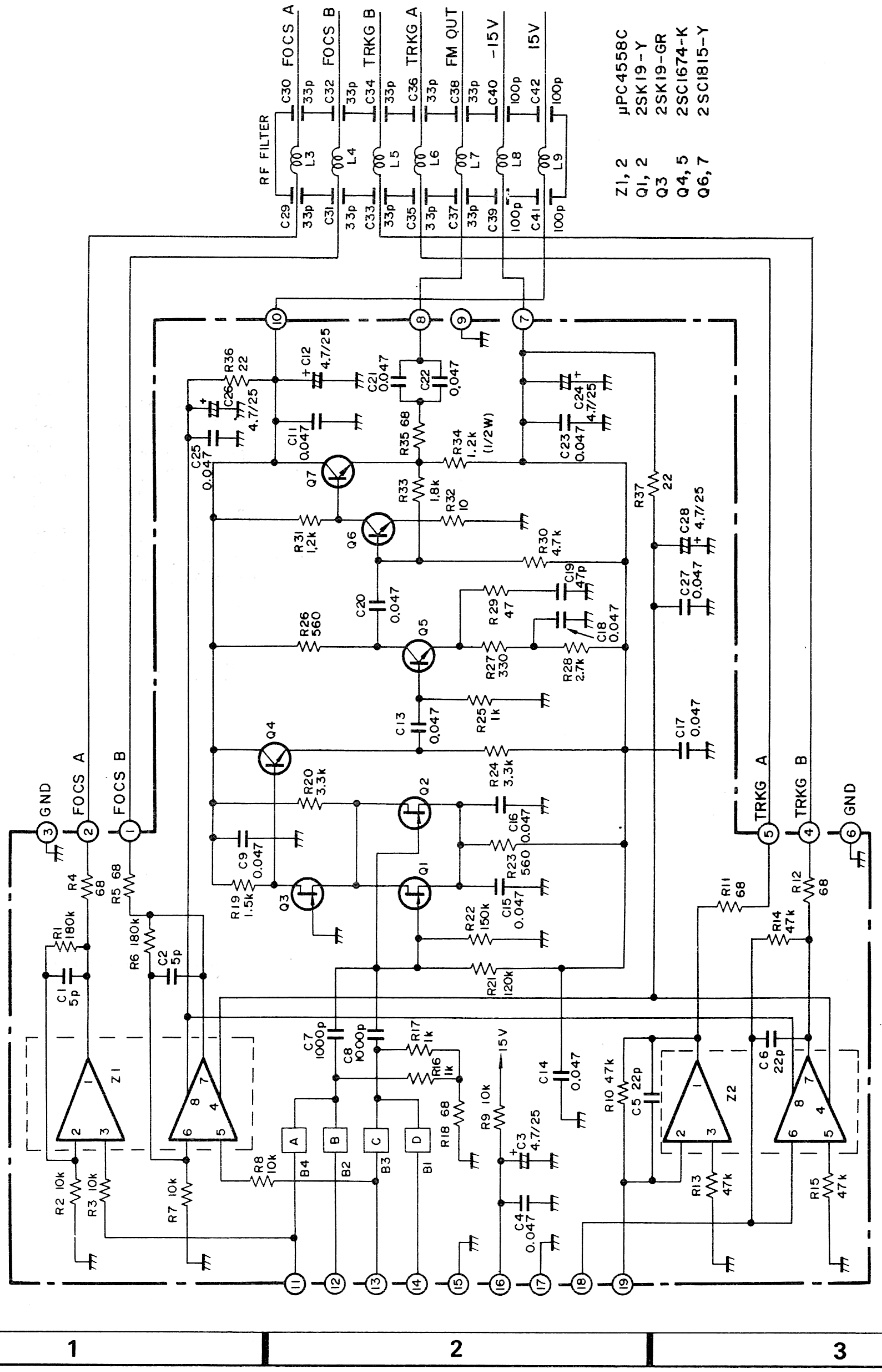
Part No.	Symbol & Description
RD¼VS □□□J	R1–R6
RN¼PR □□□□ F	R7

CAPACITORS

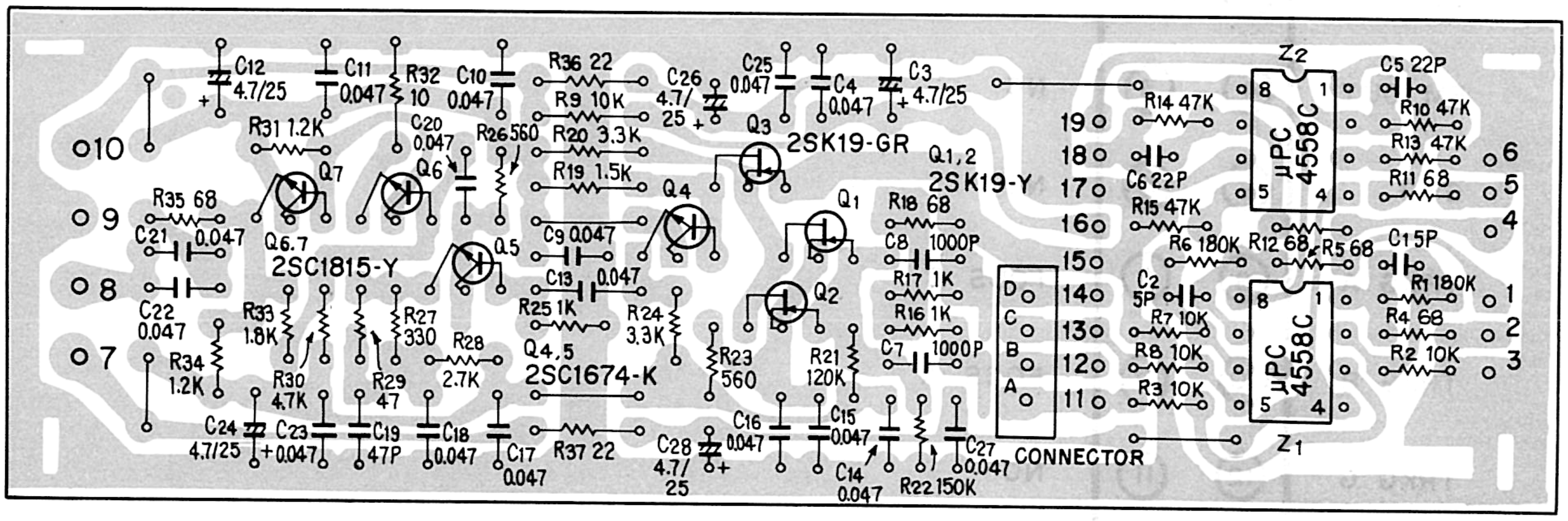
Part No.	Symbol & Description
CKDYF 103Z 50	C1

17.5 HEAD AMP ASSEMBLY (HEDA)

NOTE:
VWW-001 consists of HEDA, PFCB and PHDB assembly.
HEDA assembly on page 132.
PFCB assembly on page 134.
PHDB assembly on page 135.



Z1, 2	μPC4558C
Q1, 2	2SK19-Y
Q3	2SK19-GR
Q4, 5	2SC1674-K
Q6, 7	2SC1815-Y



Parts List

SEMICONDUCTORS

Part No.	Symbol & Description
μPC4558C	Z1, Z2
2SK19TM-Y	Q1, Q2
2SK19TM-GR	Q3
2SC1674-K	Q4, Q5
2SC1815-Y	Q6, Q7

CAPACITORS

Part No.	Symbol & Description
CEA 4R7P 25	C3, C12, C24, C28
CKDYB 102K 50	C7, C8
CCDSL 220J 50	C5, C6
CCDSL 050C 50	C1, C2
CQSH 470J 50	C19
VCG-003	C4, C9–C11, C13–C18, C20–C23, C25, C27

Note: *When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.*

RESISTORS

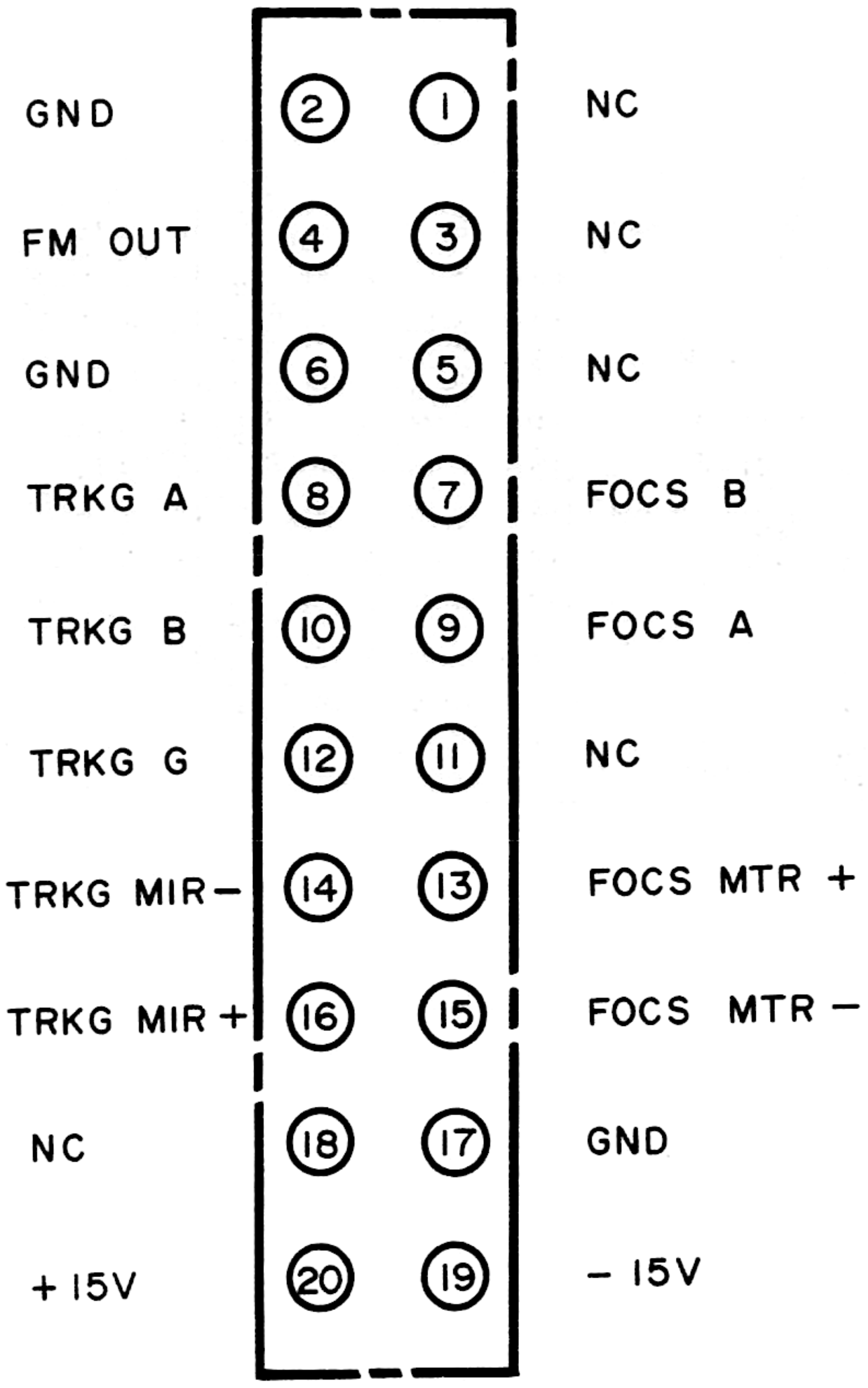
Part No.	Symbol & Description
RD¼VS □□□J	R1–R33, R35–R37
RD½VS □□□J	R34

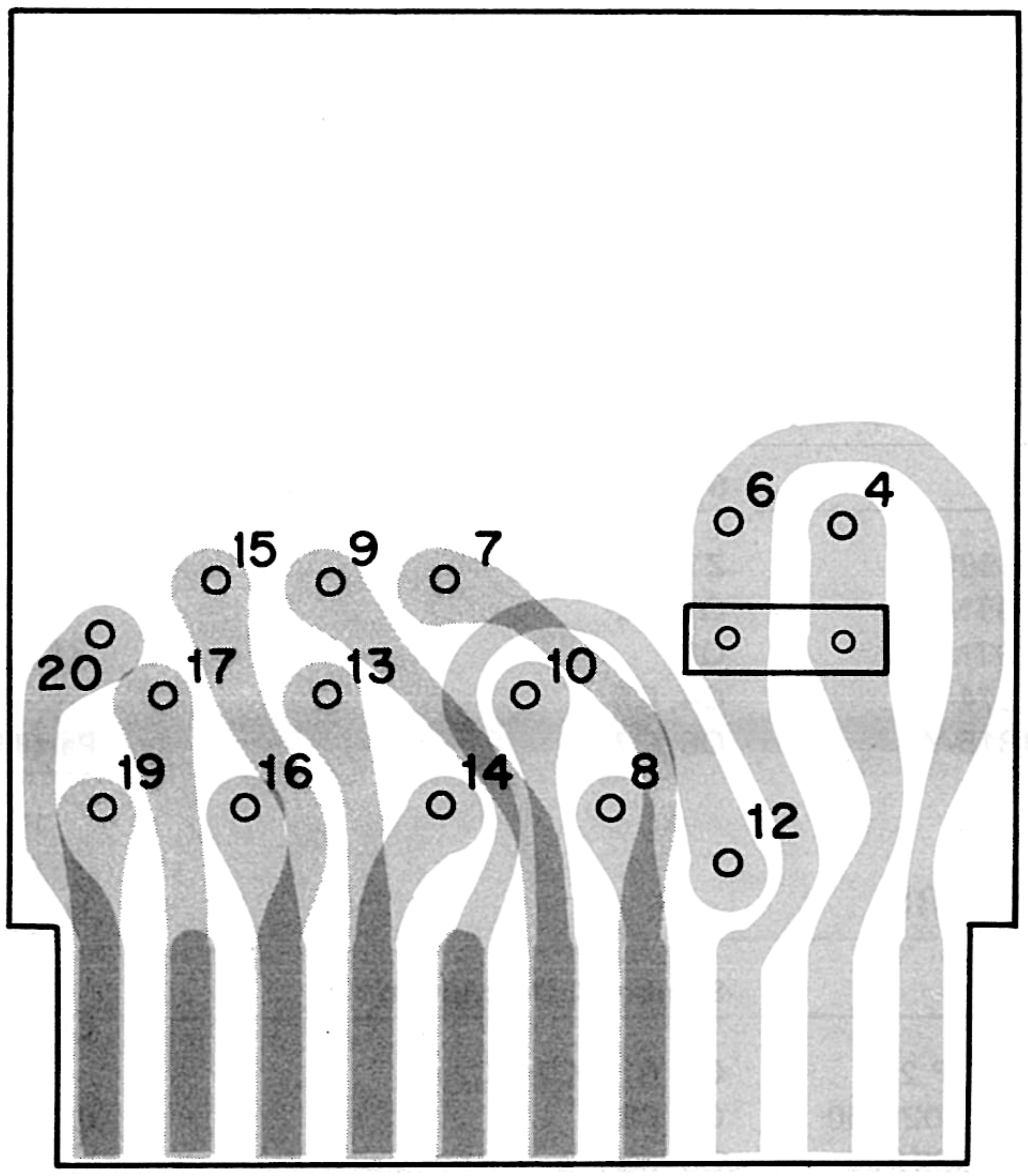
COILS AND TRANSFORMERS

Part No.	Symbol & Description	
VTF-011	L3–L9	Filter

17.6 PLATFORM CONNECTOR BOARD ASSEMBLY (PFCB)

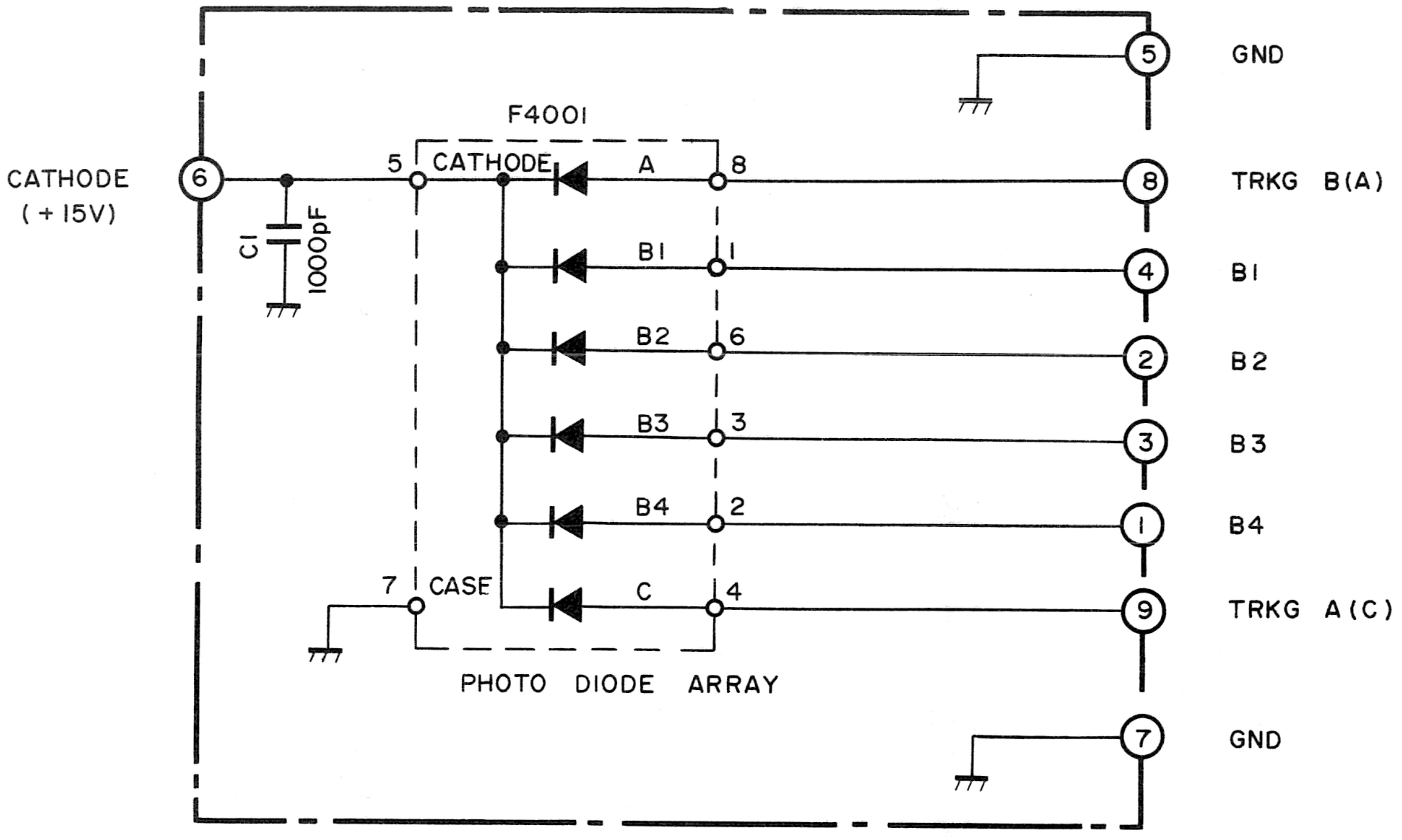
NOTE:
VWW-001 consists of HEDA, PFCB and PHDB assembly.
HEDA assembly on page 132.
PFCB assembly on page 134.
PHDB assembly on page 135.

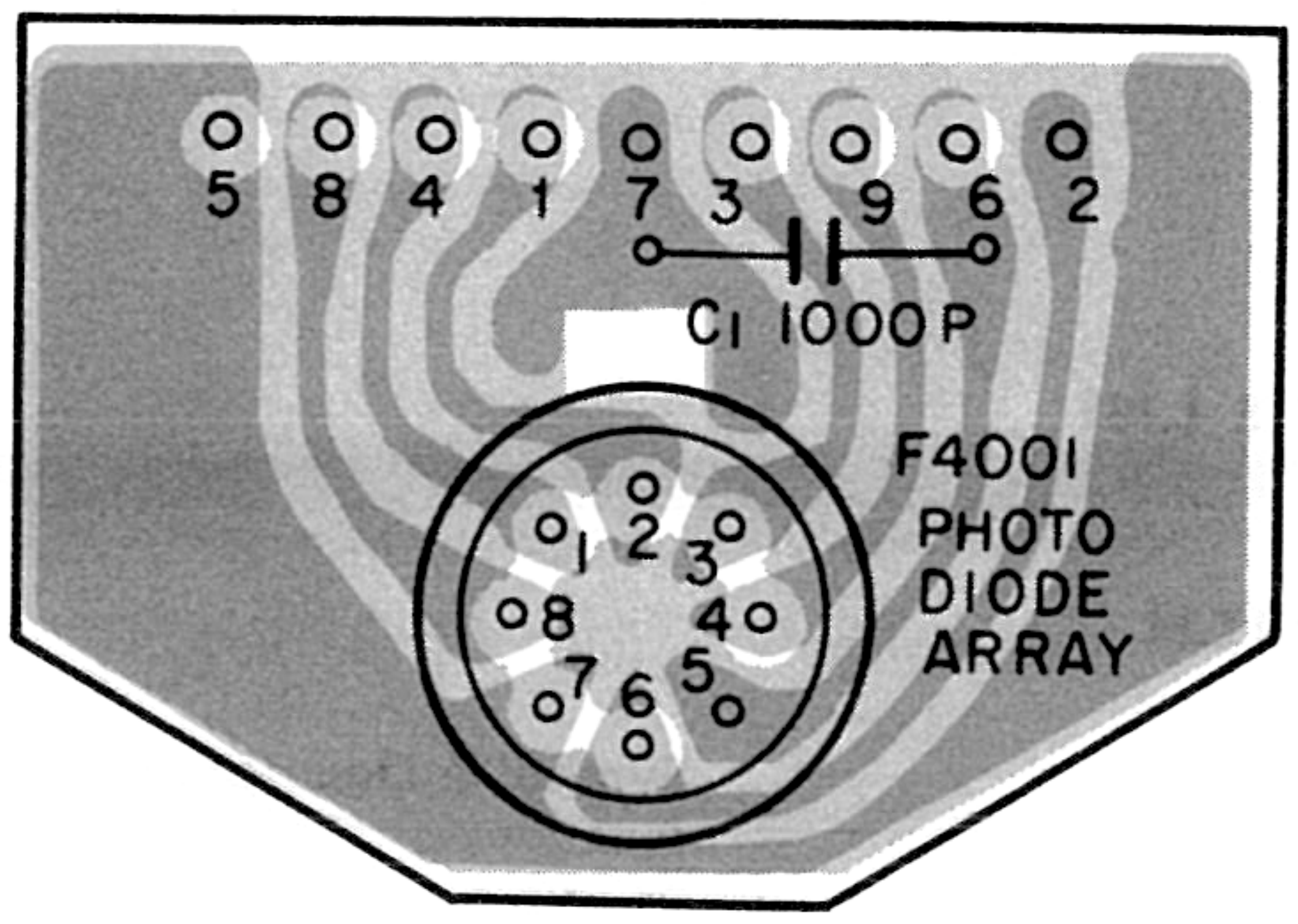




17.7 PHOTO DETECTOR BOARD ASSEMBLY (PHDB)

NOTE:
VWW-001 consists of HEDA, PFCB and PHDB assembly.
HEDA assembly on page 132.
PFCB assembly on page 134.
PHDB assembly on page 135.



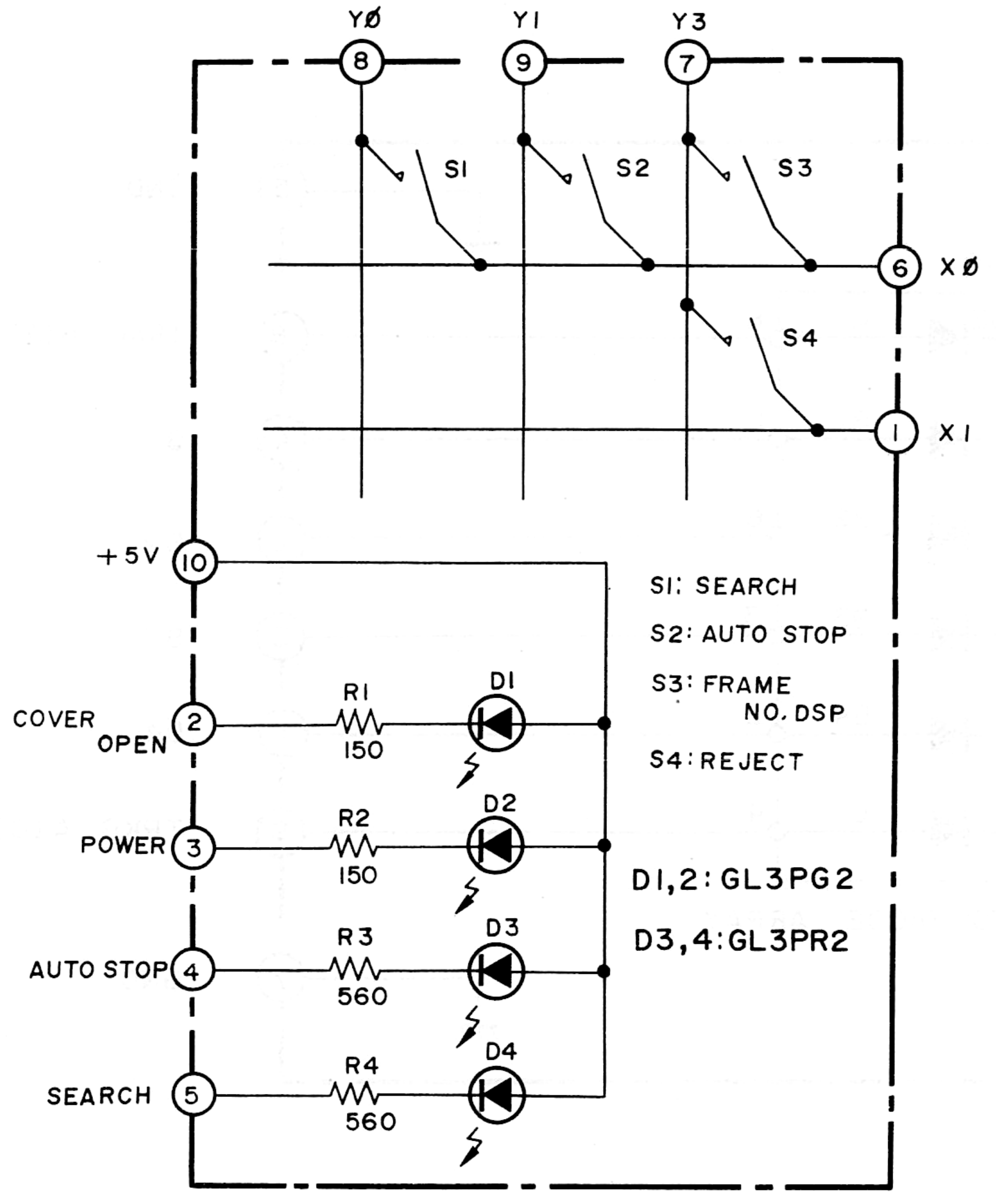


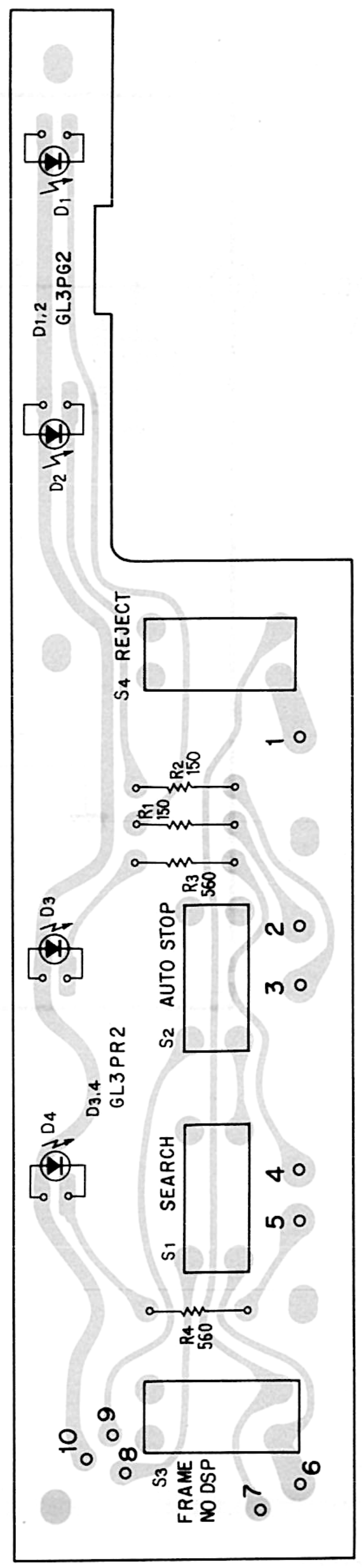
Parts List

CAPACITORS

Part No.	Symbol & Description
CKDYB 102K 50	C1

17.8 LAMP BOARD 1 ASSEMBLY (VWY-004) (LMP 1)





Parts List

SWITCH

Part No.	Symbol & Description
VSG-001	S1–S4

SEMICONDUCTORS

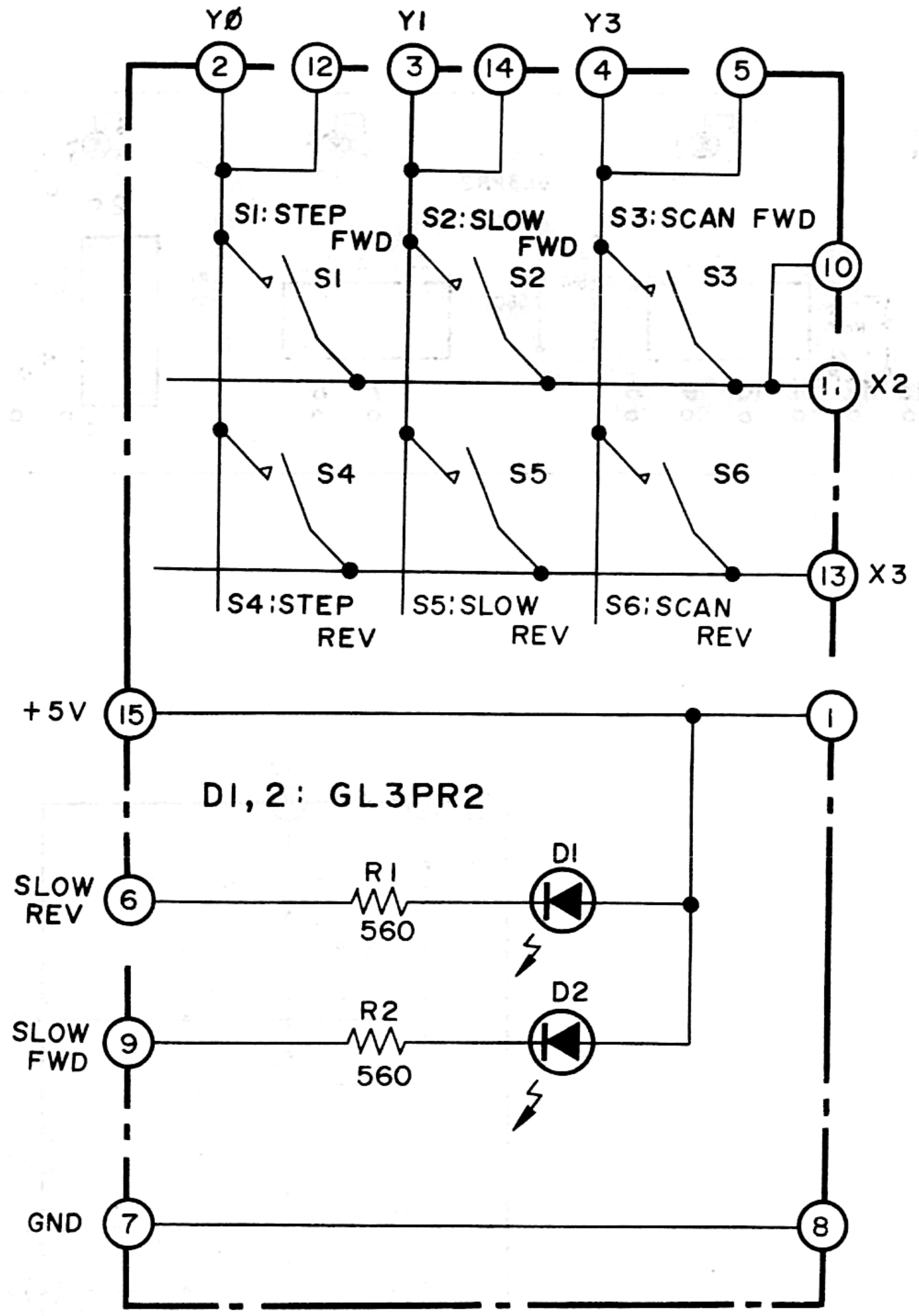
Part No.	Symbol & Description
GL-3PG2	D1, D2
GL-3PR2	D3, D4

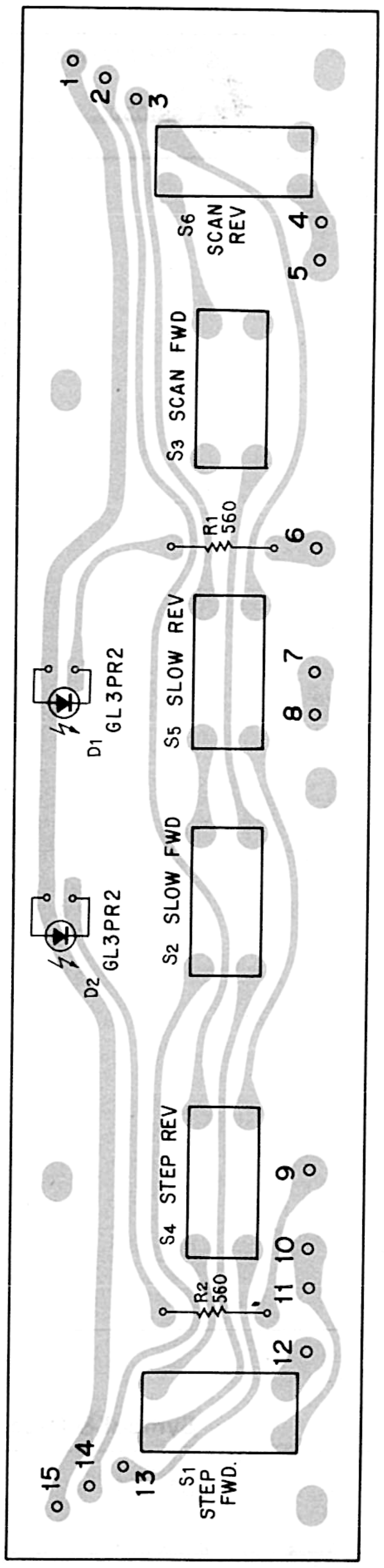
Note: When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

RESISTORS

Part No.	Symbol & Description
RD¼PS □□□J	R1–R4

17.9 LAMP BOARD 2 ASSEMBLY (VWY-005) (LMP 2)





Parts List

SEMICONDUCTORS

Part No.	Symbol & Description
GL-3PR2	D1, D2

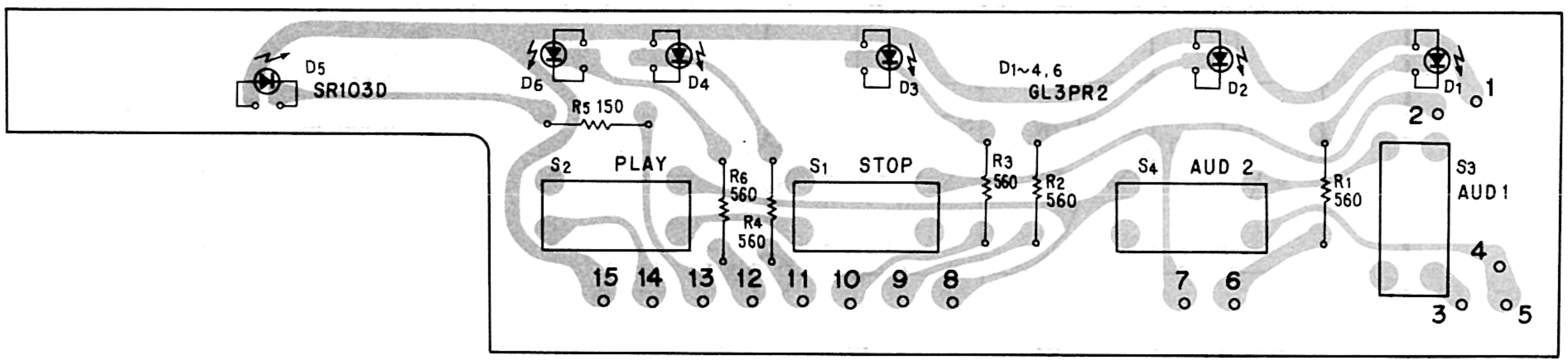
RESISTORS

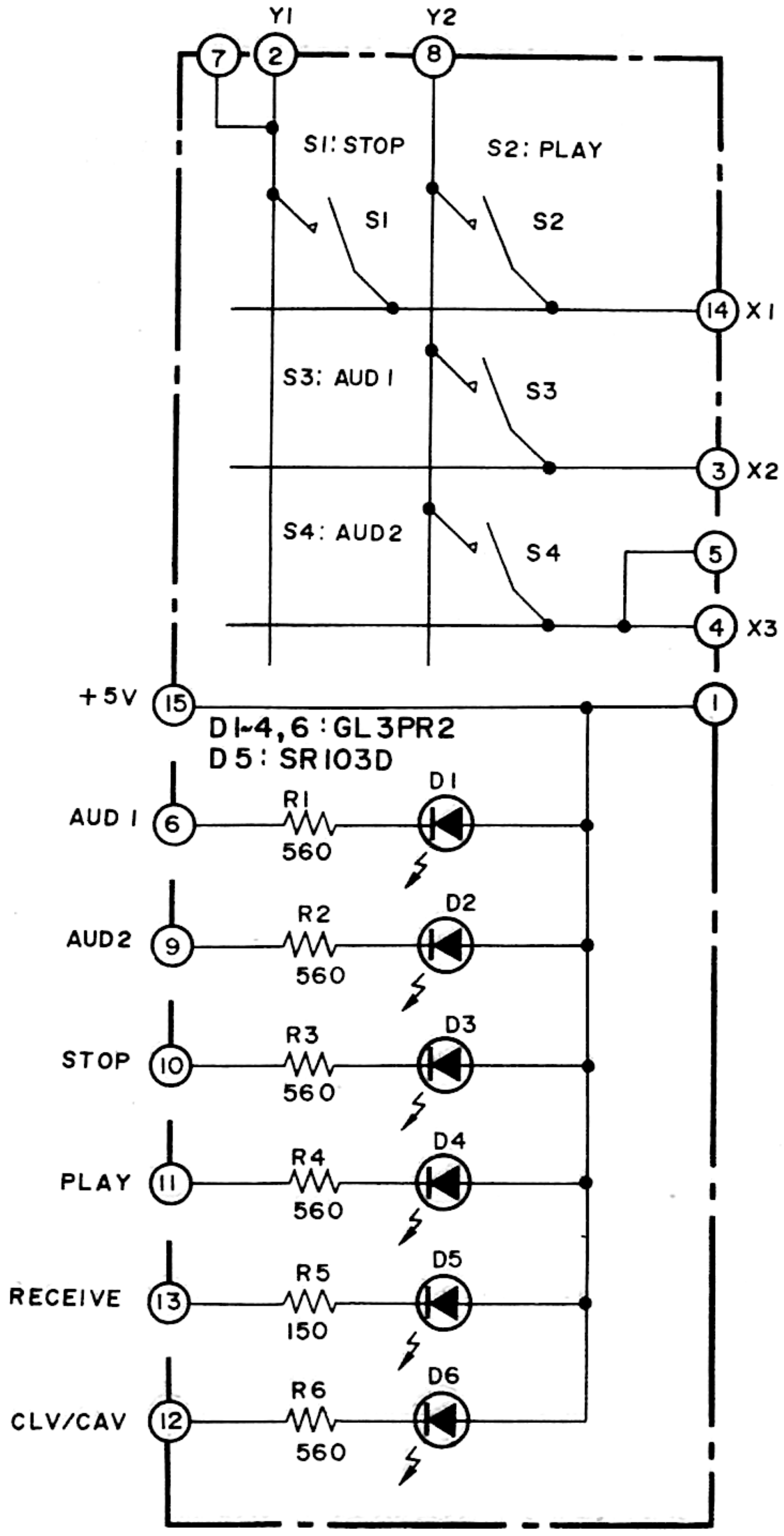
Part No.	Symbol & Description
RD¼PS □□□J	R1, R2

SWITCH

Part No.	Symbol & Description
VSG-001	S1 – S6

17.10 LAMP BOARD 3 ASSEMBLY (VWY-006)
(LMP 3)





Parts List

SWITCH

Part No.	Symbol & Description
VSG-001	S1–S4

SEMICONDUCTORS

Part No.	Symbol & Description
GL-3PR2	D1–D4, D6
SR-103D	D5

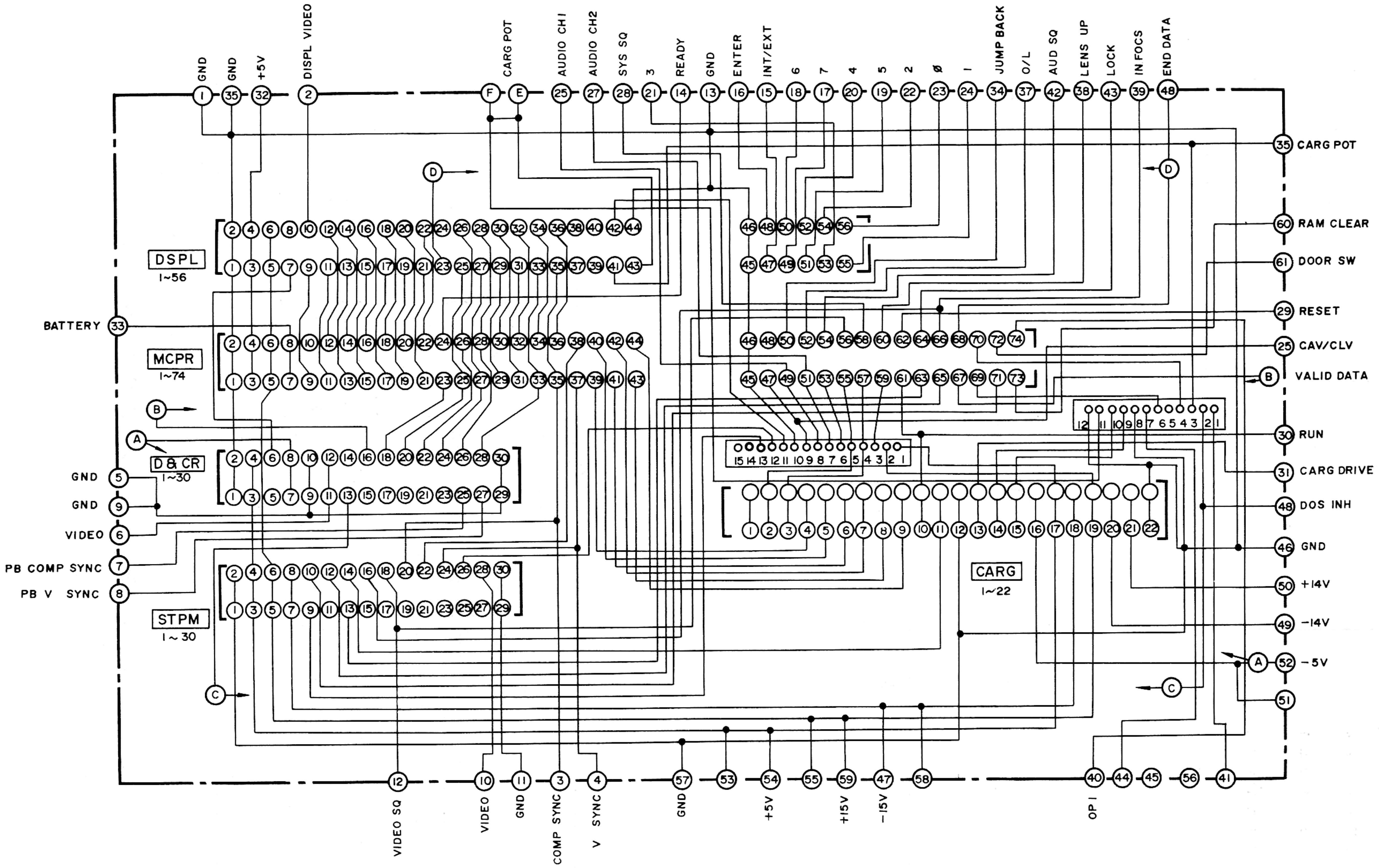
Note: *When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.*

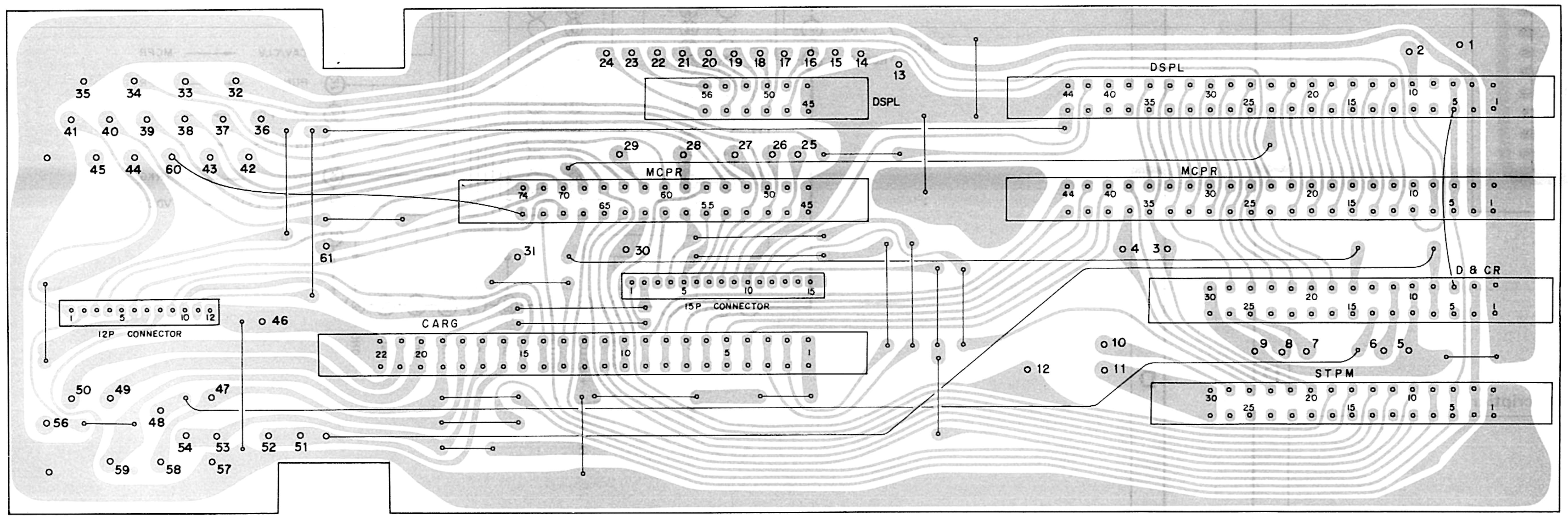
RESISTORS

Part No.	Symbol & Description
RD¼PS □□□J	R1–R6

1 2 3 4 5 6

17.11 CONTROL MOTHER BOARD ASSEMBLY (VWX-001) (COMB)





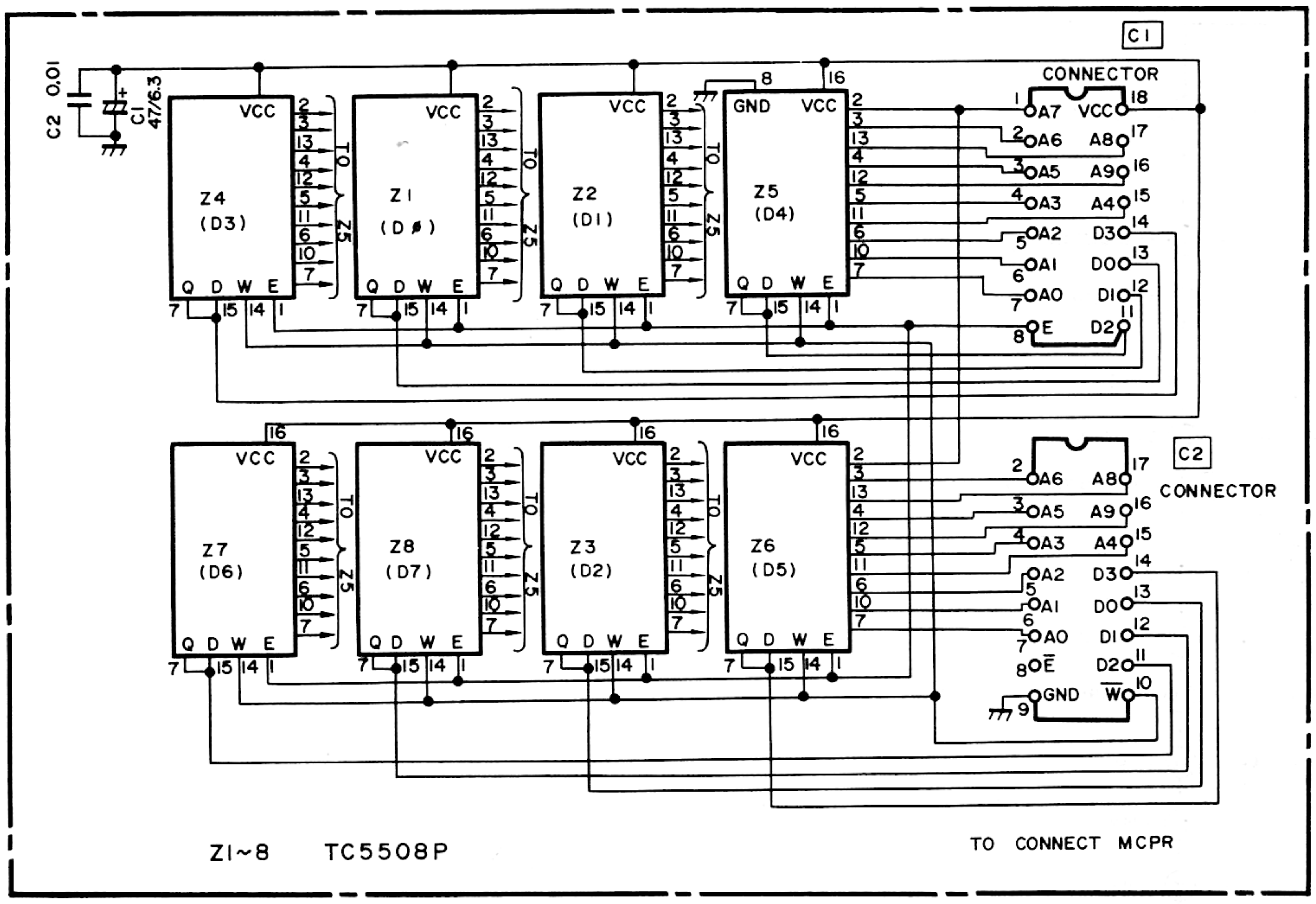
A B C D

1 2 3 4 5 6

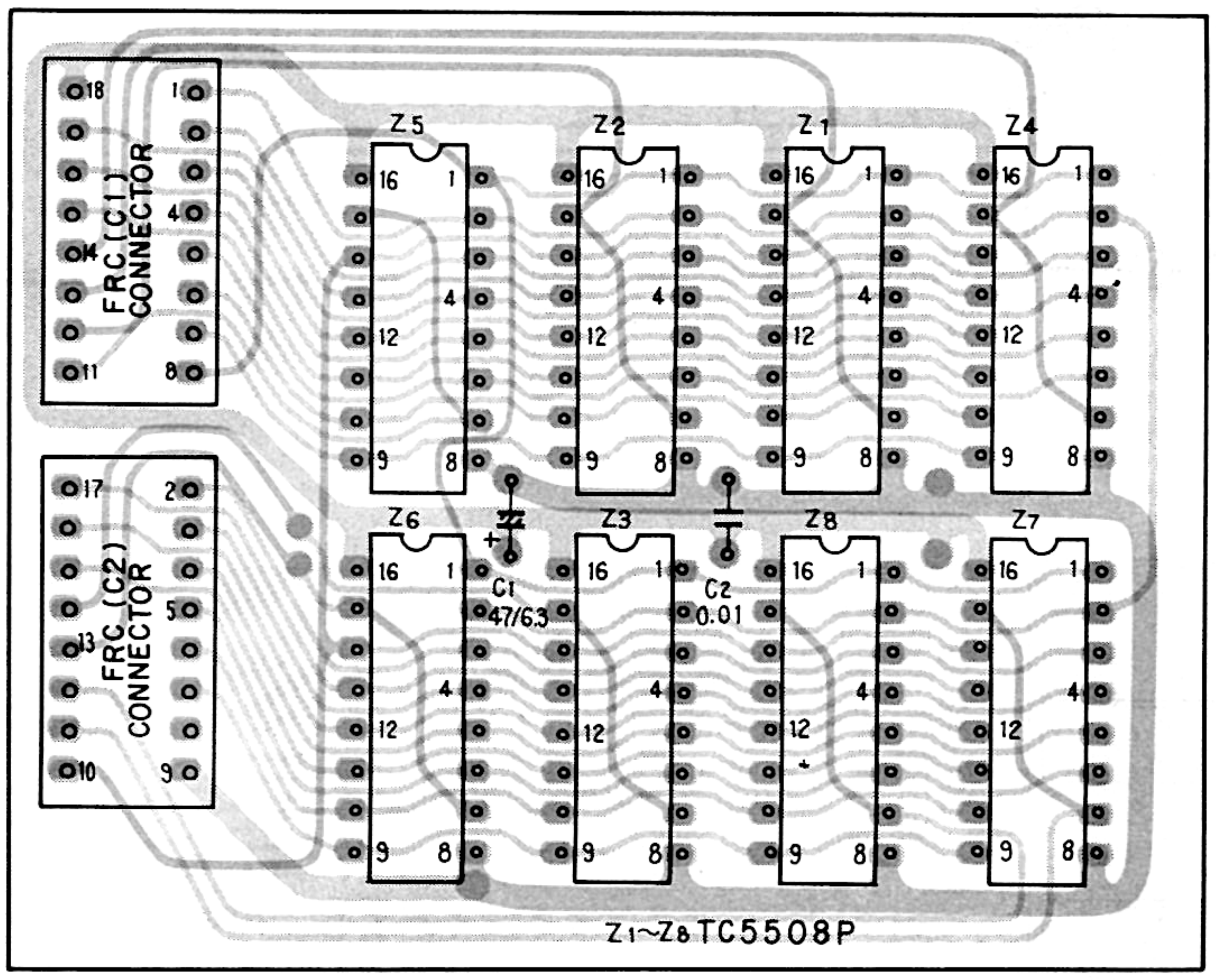
17.12 RAM BOARD ASSEMBLY (RAMB)

NOTE:
VWW-004 consists of MCPR assembly, RAMB assembly.
MCPR assembly on page 145.

A



B



C

Parts List

SEMICONDUCTORS

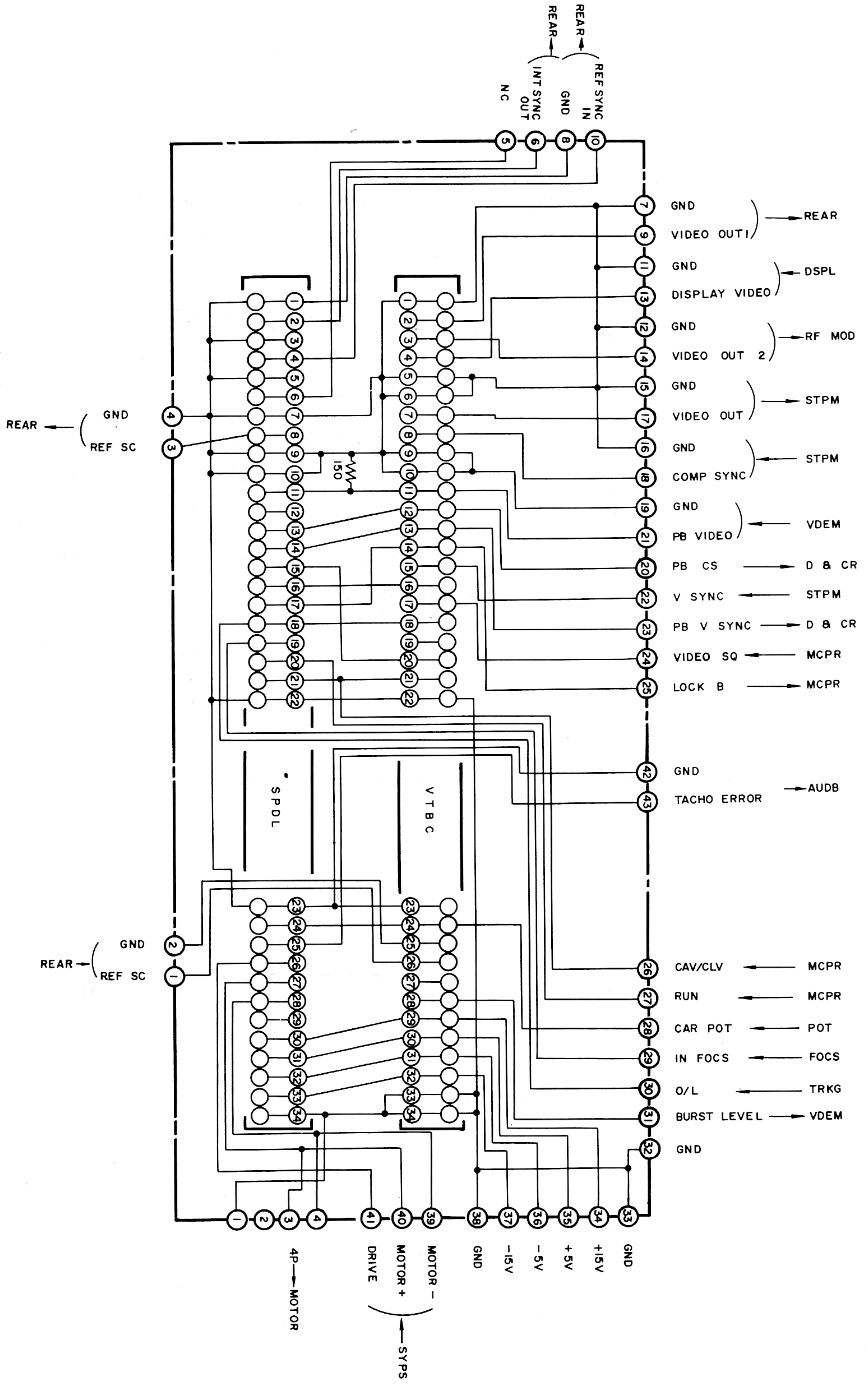
Part No.	Symbol & Description
TC5508P	Z1–Z8

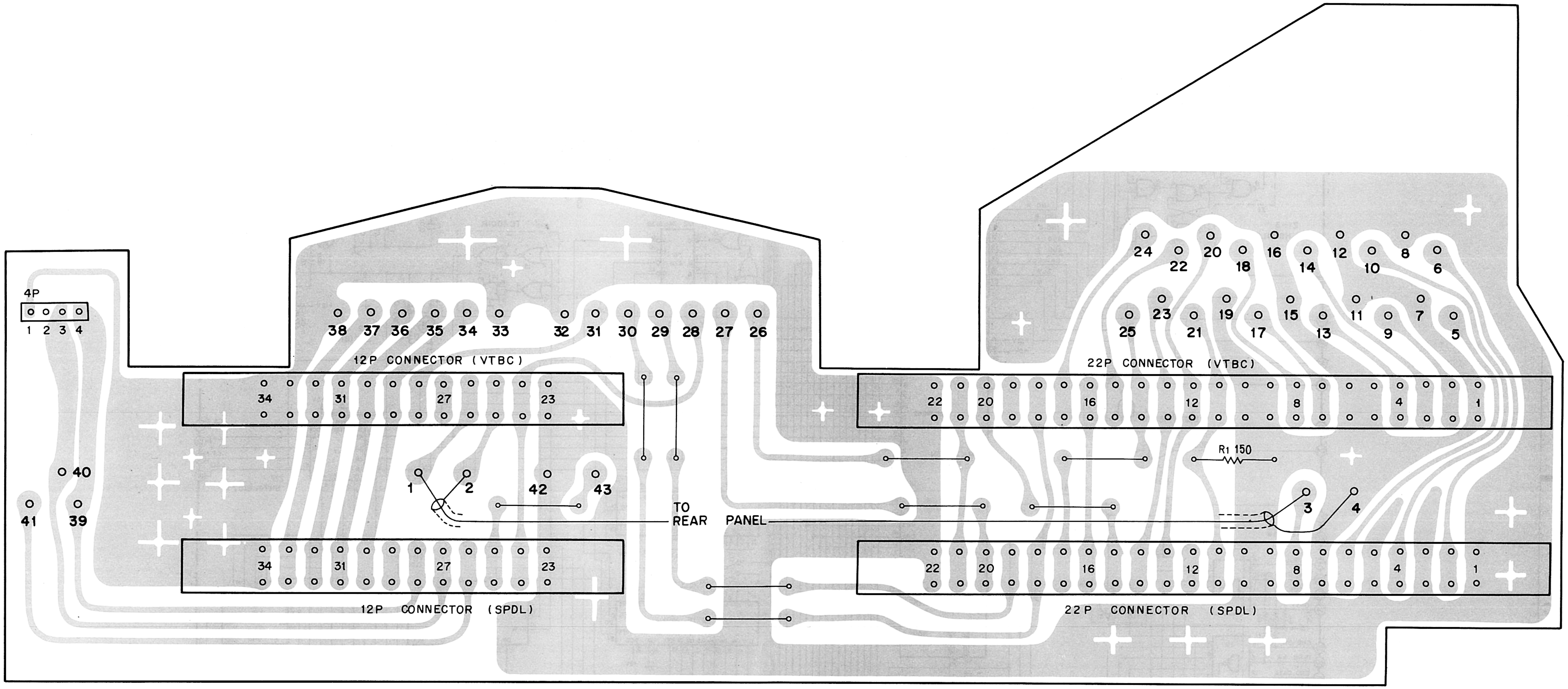
CAPACITORS

Part No.	Symbol & Description
CSZAH 470M 6R3	C1
CKDYF 103Z 25	C2

D

17.13 VTBC & SPDL MOTHER BOARD ASSEMBLY (VWX-003) (CLMB)





Part List

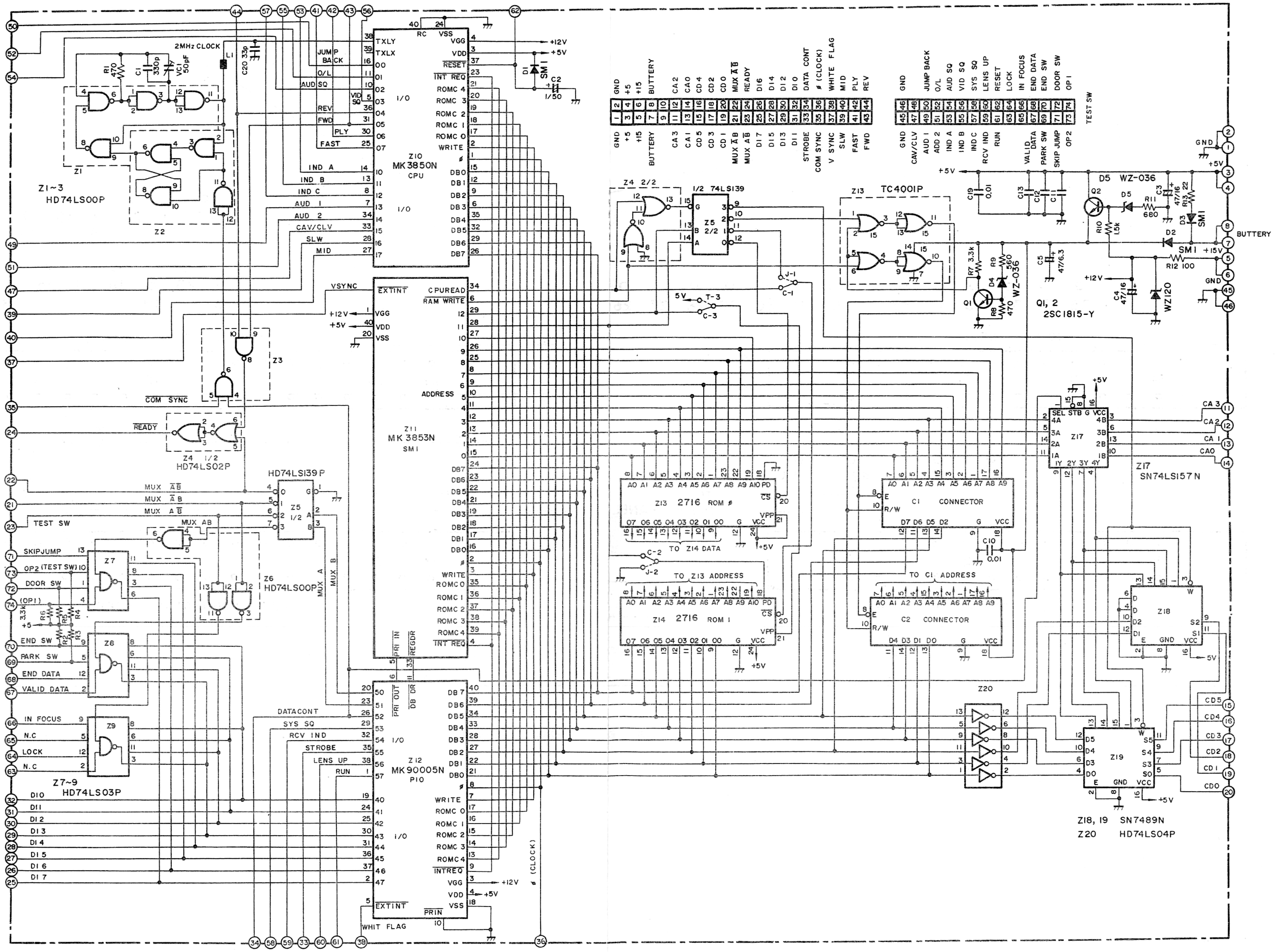
Note: When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

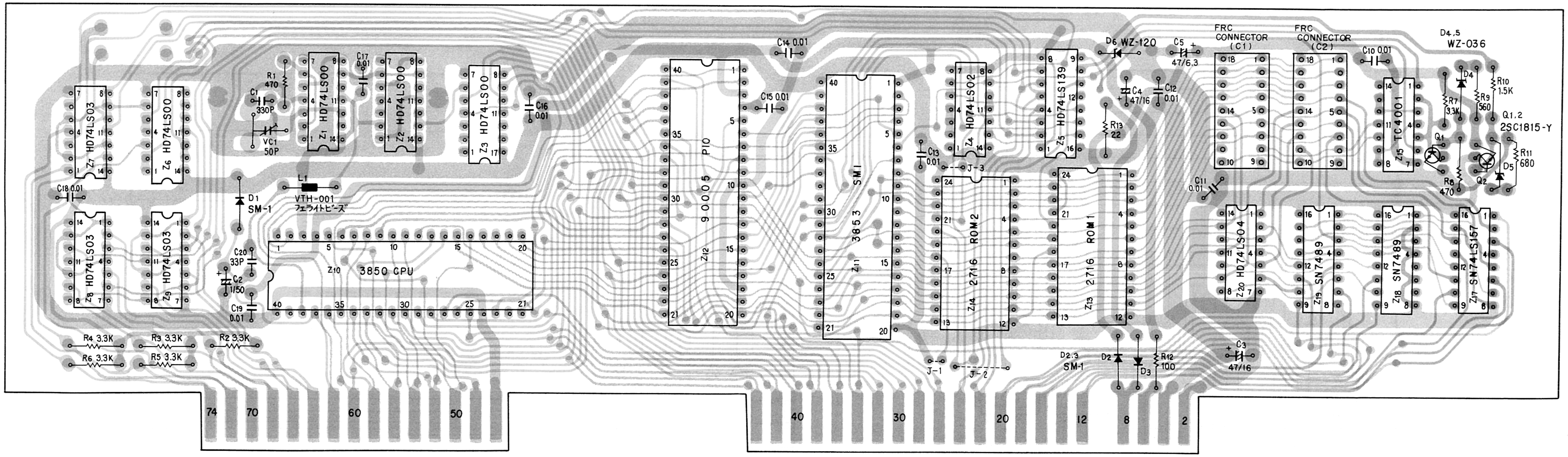
RESISTORS

Part No.	Symbol & Description
RD¼PS □□□J	R1

17.14 MICRO PROCESSOR ASSEMBLY (MCPR)

NOTE:
VWW-004 consists of MCPR assembly, RAMB assembly.
RAMB assembly on page 141.





Parts List

SEMICONDUCTORS

Part No.	Symbol & Description
HD74LS00P	Z1–Z3, Z6
HD74LS02P	Z4
HD74LS139P	Z5
HD74LS03P	Z7–Z9
HD74LS04P	Z20
SN74LS157N	Z17
SN7489N	Z18, Z19
TC4001P	Z15
MK3850N	Z10
MK3853N	Z11
MK90005N	Z12
2716	Z13, Z14
2SC1815-Y or O	Q1, Q2
SM-1-02	D1–D3
WZ-036	D4, D5
WZ-120	D6

CAPACITORS

Part No.	Symbol & Description
CQSH 331J 50	C1
CEA 010 P50	C2
CEA 470 P16	C3, C4
CKDYF 103Z 50	C10–C19
CSZAH 470M 6R3	C5
CCDSL 330J 50	C20

Note: When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

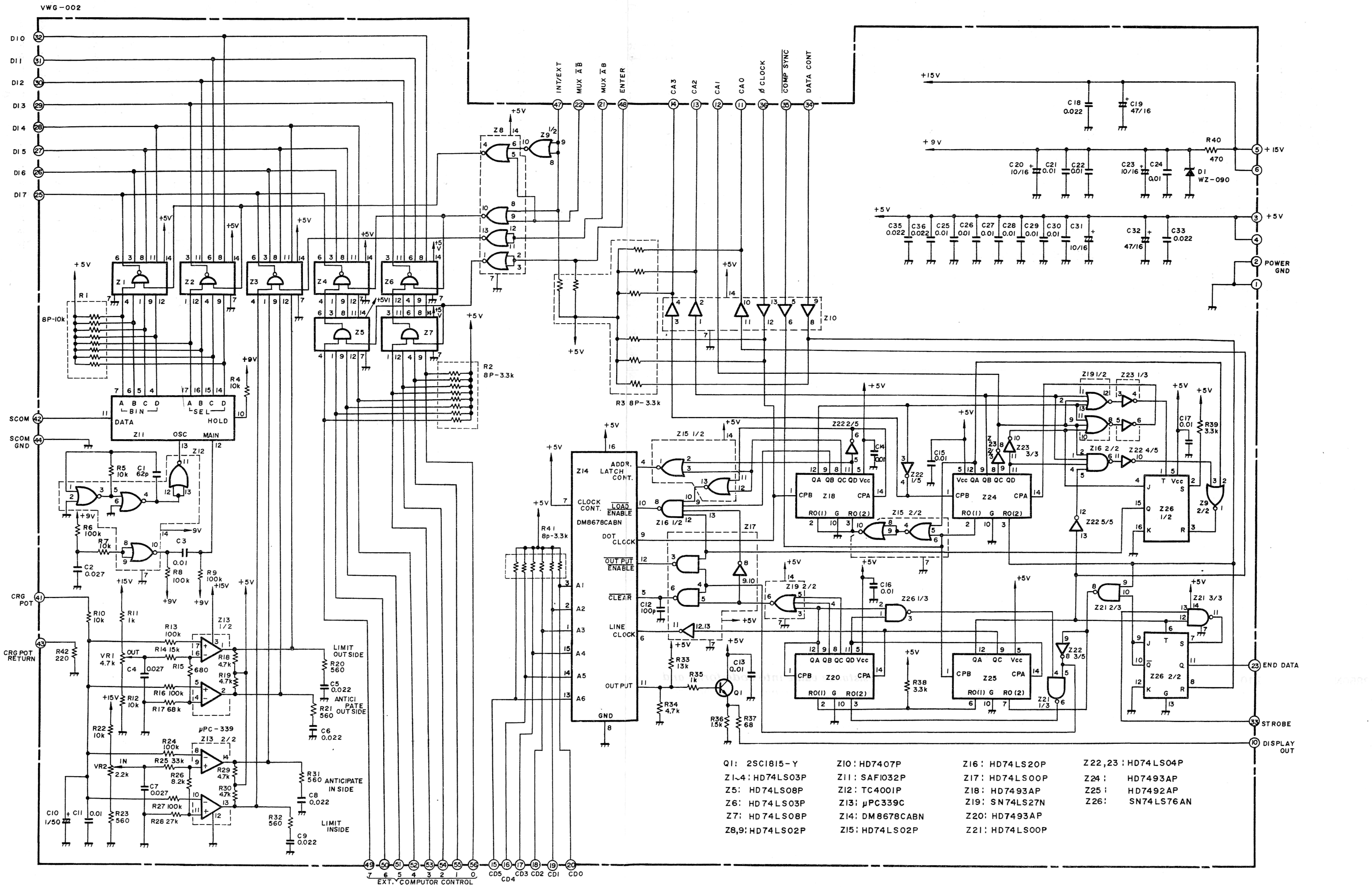
RESISTORS

Part No.	Symbol & Description
RN¼PR □□□□F	R1
RD¼PS □□□J	R2–R13

COILS AND TRANSFORMER

Part No.	Symbol & Description	
VCM-001	VC1	Ceramic trimmer
VTH-001	L1	Ferreit Bead

17.15 CHARACTOR DISPLAY ASSEMBLY (VWG-002)
(DSPL)

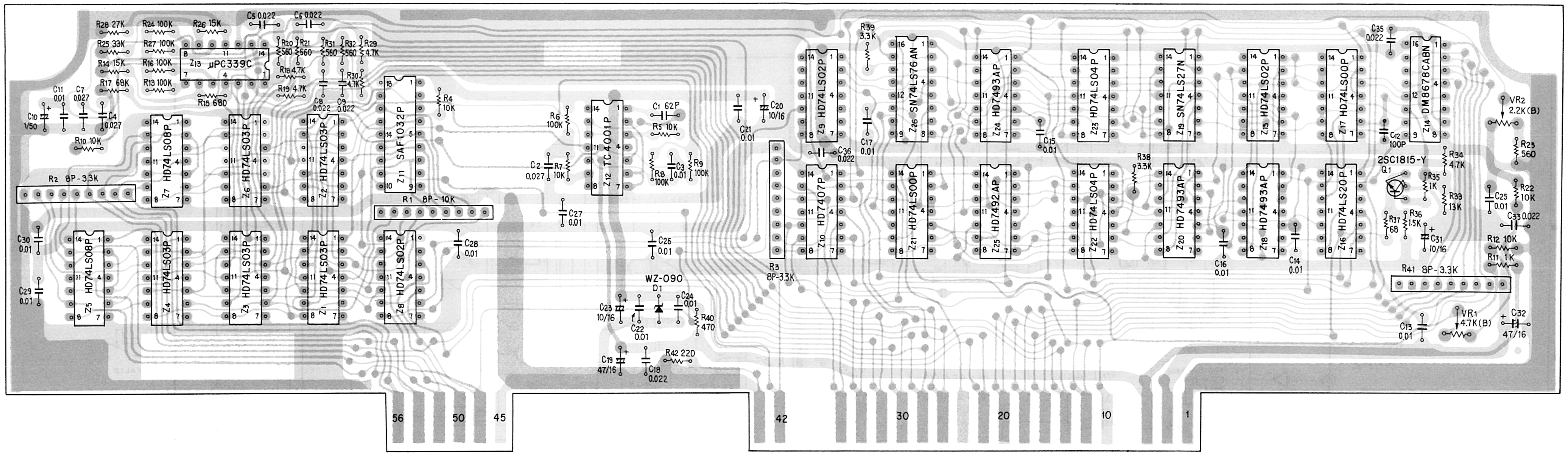


Q1: 2SC1815-Y
Z1~4: HD74LS03P
Z5: HD74LS08P
Z6: HD74LS03P
Z7: HD74LS08P
Z8,9: HD74LS02P

Z10: HD7407P
Z11: SAF1032P
Z12: TC4001P
Z13: μPC339C
Z14: DM8678CABN
Z15: HD74LS02P

Z16: HD74LS20P
Z17: HD74LS00P
Z18: HD7493AP
Z19: SN74LS27N
Z20: HD7493AP
Z21: HD74LS00P

Z22,23: HD74LS04P
Z24: HD7493AP
Z25: HD7492AP
Z26: SN74LS76AN



Parts List

SEMICONDUCTORS

Part No.	Symbol & Description
DM8678CABN	Z14
SAF1032P	Z11
TC4001P	Z12
μPC339C	Z13
HD74LS00P	Z17, Z21
SN74LS76AN	Z26
HD7492AP	Z25
SN74LS27N	Z19
HD74LS20P	Z16
HD74LS08P	Z5, Z7
HD7407P	Z10
HD74LS04P	Z22, Z23
HD74LS03P	Z1–Z4, Z6
HD74LS02P	Z8, Z9, Z15
HD7493AP (SN7493AN)	Z18, Z20, Z24
2SC1815-Y	Q1
WZ-090	D1

CAPACITORS

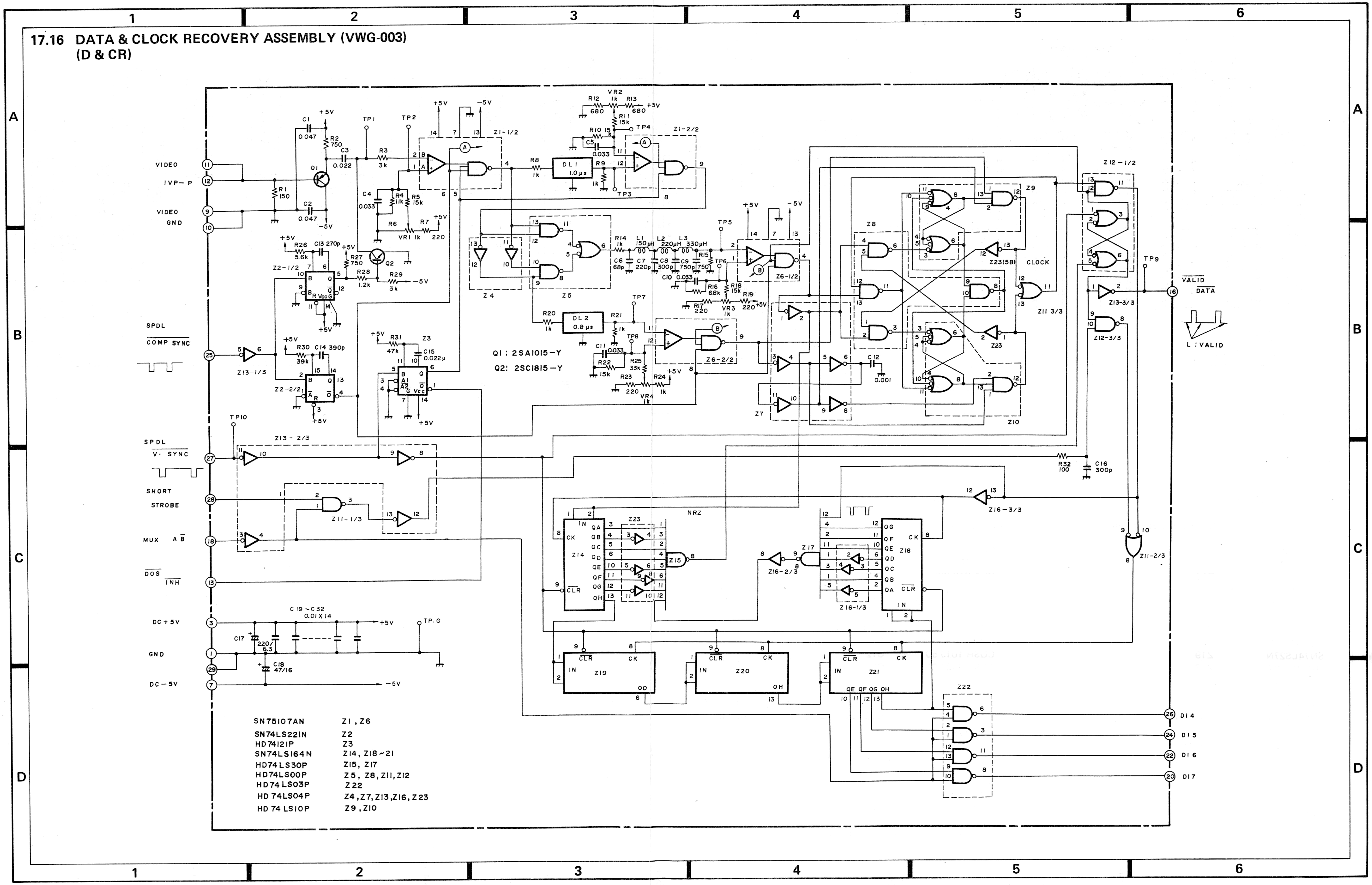
Part No.	Symbol & Description
CEA 470 P16	C19, C32
CEA 100 P16	C20, C23, C31
CEA 010 P25	C10
CKDYF 223Z 50	C5, C6, C8, C9, C18, C33, C35, C36
CKDYF 103Z 50	C11, C13–C17, C21, C22, C24–C30
CQMA 273K 50	C2, C4, C7
CQMA 103K 50	C3
CQSH 101J 50	C12
CQSH 620J 50	C1

Note: *When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.*

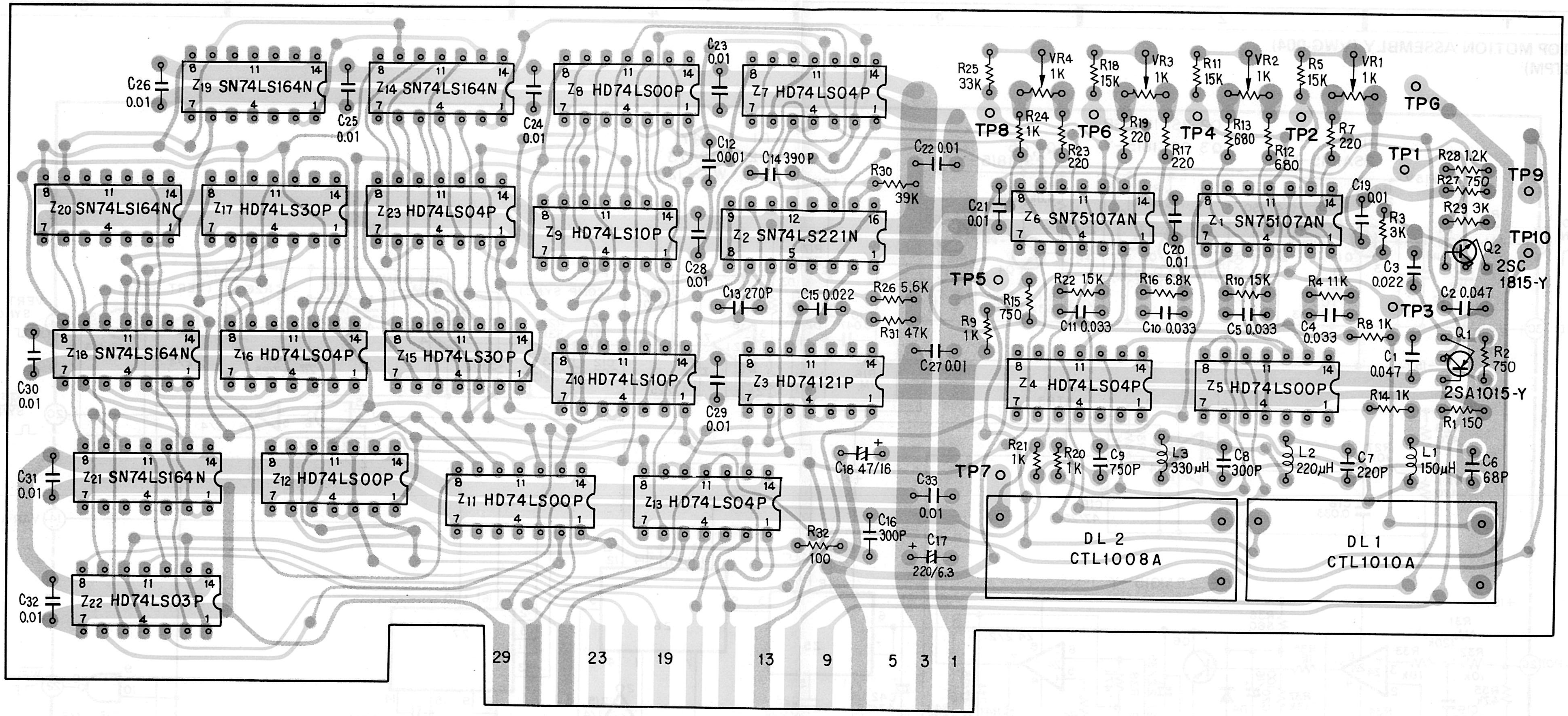
RESISTORS

Part No.	Symbol & Description
VCN-005	R1
VCN-006	R2, R3, R41
VCP-006	VR1 Semi-fixed
VCP-005	VR2 Semi-fixed
RD¼VS □□□J	R6–R40, R42

17.16 DATA & CLOCK RECOVERY ASSEMBLY (VWG-003)
(D & CR)



SN75107AN	Z1, Z6
SN74LS221N	Z2
HD74121P	Z3
SN74LS164N	Z14, Z18~21
HD74LS30P	Z15, Z17
HD74LS00P	Z5, Z8, Z11, Z12
HD74LS03P	Z22
HD74LS04P	Z4, Z7, Z13, Z16, Z23
HD74LS10P	Z9, Z10



Parts List

Note: When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

SEMICONDUCTORS

Part No.	Symbol & Description
SN75107AN	Z1, Z6
SN74LS164N	Z14, Z18–Z21
SN74LS221N	Z2
HD74LS00P	Z5, Z8, Z11, Z12
HD74LS04P	Z4, Z7, Z13, Z16, Z23
HD74LS10P	Z9, Z10
HD74LS30P	Z15, Z17
HD74LS03P	Z22
2SA1015-Y or O	Q1
2SC1815-Y	Q2
HD74121P (SN74121N)	Z3

RESISTORS

Part No.	Symbol & Description
VCR-004	VR1–VR4
RN¼PR □□□□F	R4, R5, R7–R26, R30
RD¼VS □□□J	R1–R3, R27–R29, R31, R32

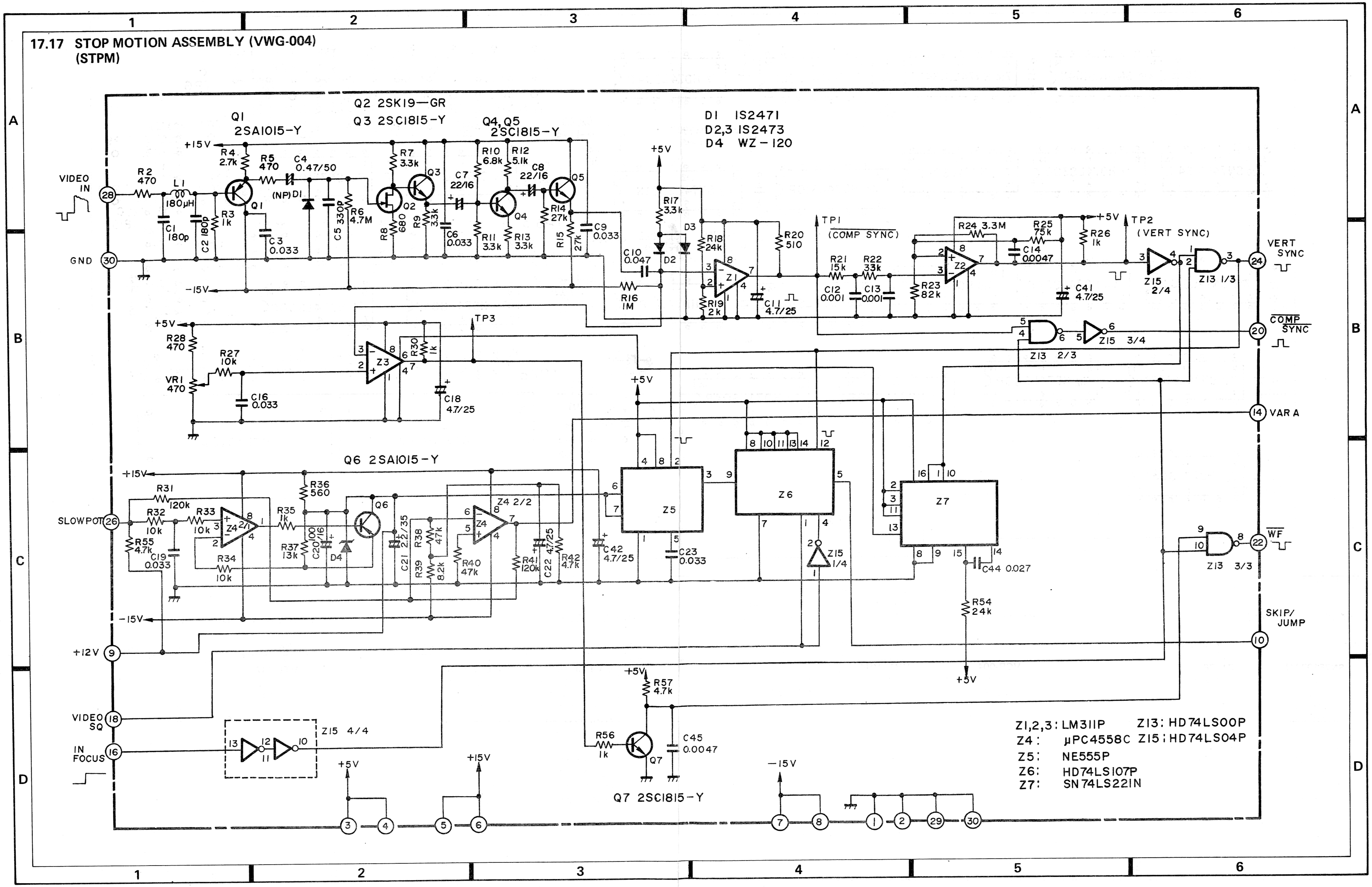
CAPACITORS

Part No.	Symbol & Description
CEA 470P 16	C18C17, C18
CKDYF 473Z 50	C19–C27, C2
CKDYF 103Z 50	C28–C33
CKDYF 333Z 50	C4, C5, C10, C11
CQMA 223K 50	C3, C15
CEA 221P 6R3	C17
CQMA 102K 50	C12
CQSH 680J 50	C6
CQSH 221J 50	C7
CQSH 271J 50	C13
CQSH 301J 50	C8, C16
CQSH 391J 50	C14
CQSH 751J 50	C9

COILS AND TRANSFORMERS

Part No.	Symbol & Description	
VTL-037	L1	
VTL-039	L2	
VTL-041	L3	
VTF-001	DL1	Delay line
VTF-002	DL2	Delay line

17.17 STOP MOTION ASSEMBLY (VWG-004)
(STPM)



Parts List

SEMICONDUCTORS

Part No.	Symbol & Description
SN74LS221N	Z7,
HD74LS107P	Z6
HD74LS00P	Z13
HD74LS04P	Z15
NE555P	Z5
LM311P (μPC271C)	Z1–Z3
μPC4558C	Z4
2SA1015-Y	Q1, Q6
2SA1015-Y or O	Q3–Q5, Q7
2SK19GR	Q2
WZ-120	D4
1S2473	D1–D3

CAPACITORS

Part No.	Symbol & Description
CCDSL 181J 50	C1, C2
CCDSL 331J 50	C5
CKDYF 333Z 50	C3, C6, C9, C16, C19, C23
CKDYB 103K 50	C33–C36
CEA 101P 16	C20
CEA 220P 16	C7, C8
CEA 4R7P 25	C11, C18, C22, C27–C30, C42
CEA R47M 50NP	C4
CSZAH2R2M 35	C21
CQMA 473J 50	C10
CQMA 273J 50	C44
CQMA 472J 50	C14
CQMA 102J 50	C12, C13
CQMA 152K 50	C45

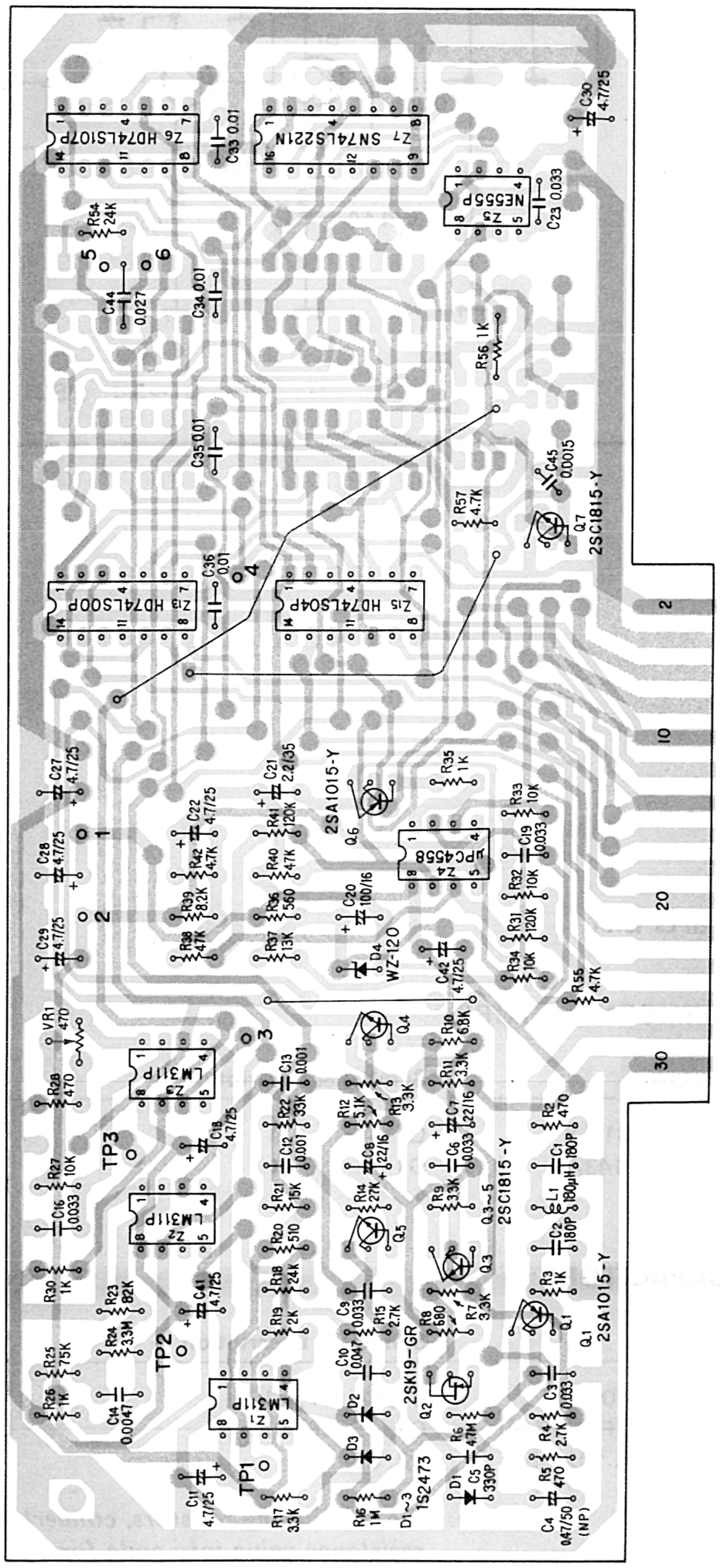
Note: When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

RESISTORS

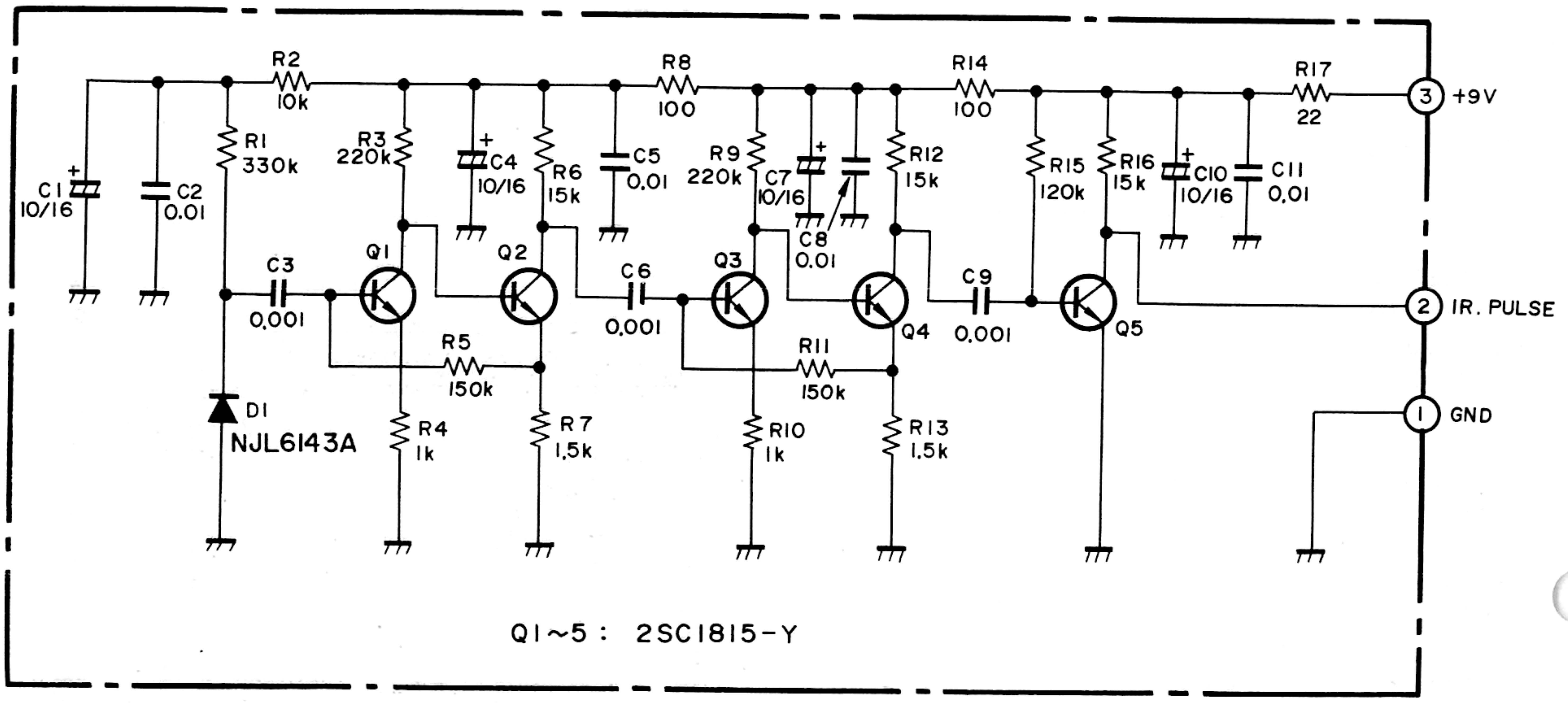
Part No.	Symbol & Description
RD¼VS □□□J	R2–R28, R30–R44, R54–R56
VCP-003	VR1

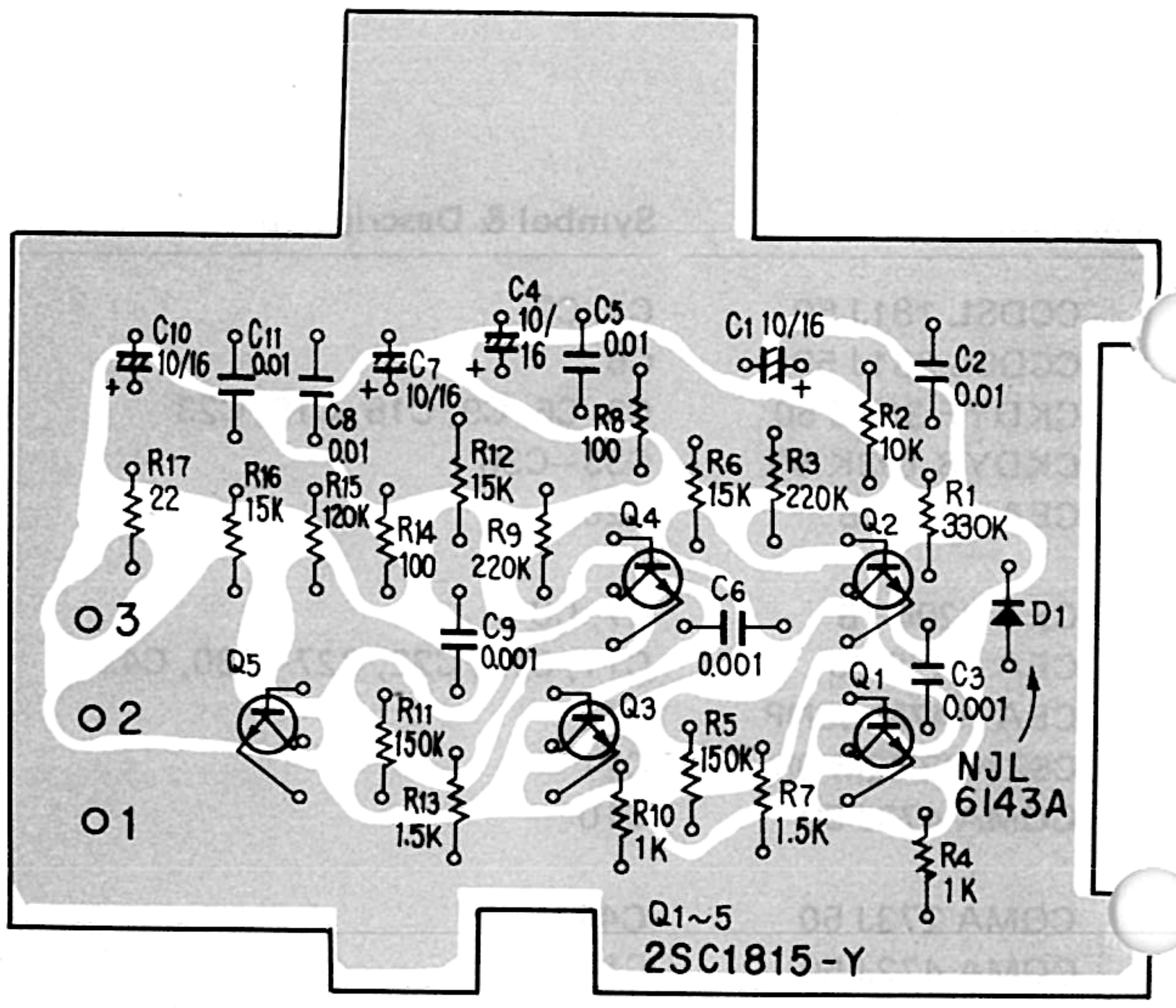
COILS AND TRANSFORMERS

Part No.	Symbol & Description
VTL-038	L1



17.18 MAIN INFRARED BOARD ASSEMBLY (VWG-005) (MIRB)





Parts List

SEMICONDUCTORS

Part No.	Symbol & Description
2SC1815-Y	Q1–Q5
MJL6143A	D1

CAPACITORS

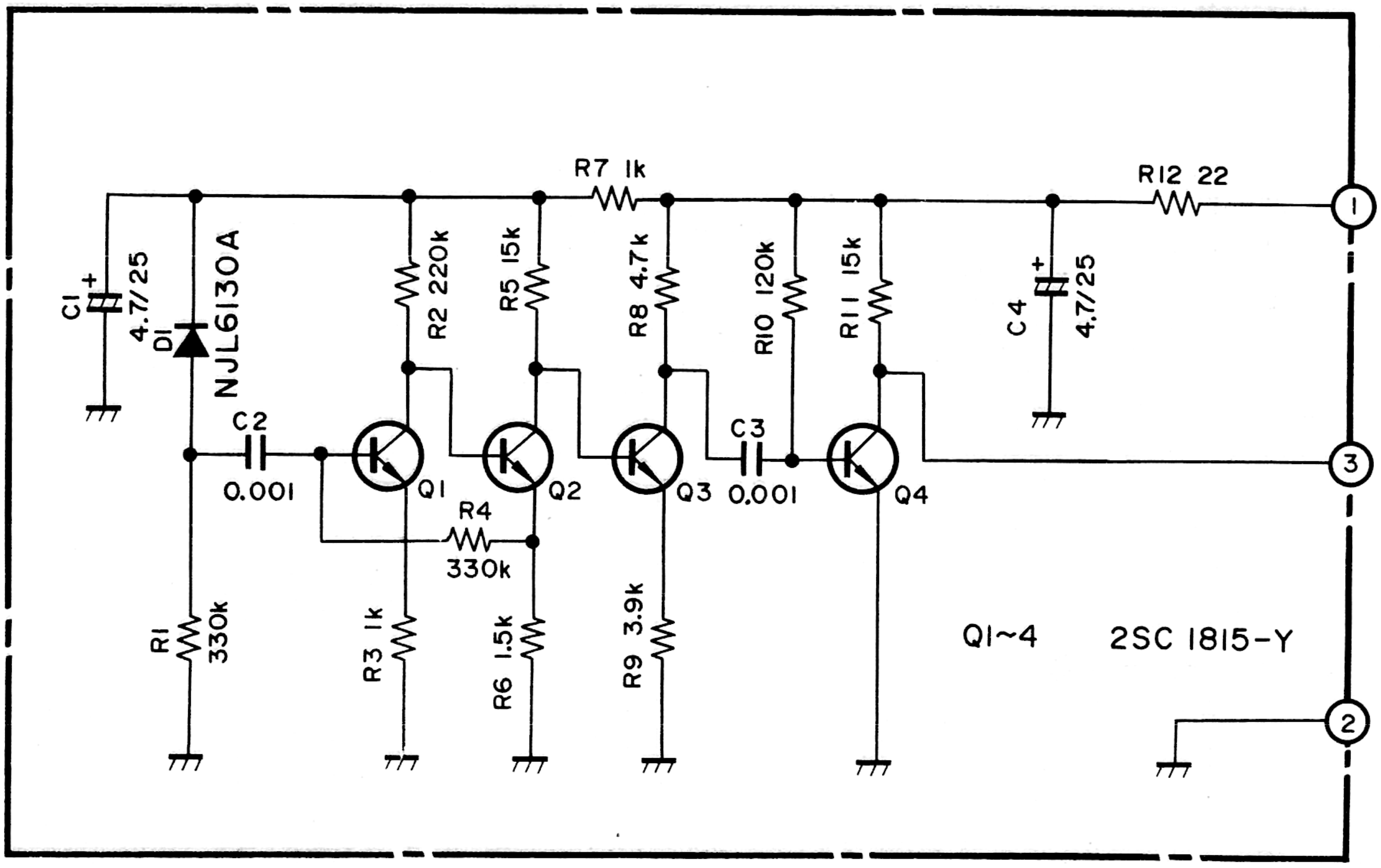
Part No.	Symbol & Description
CEA 100P 16	C1, C4, C7, C10
CKDYF 103Z 50	C2, C5, C8, C11
CQMA 102K 50	C3, C6, C9

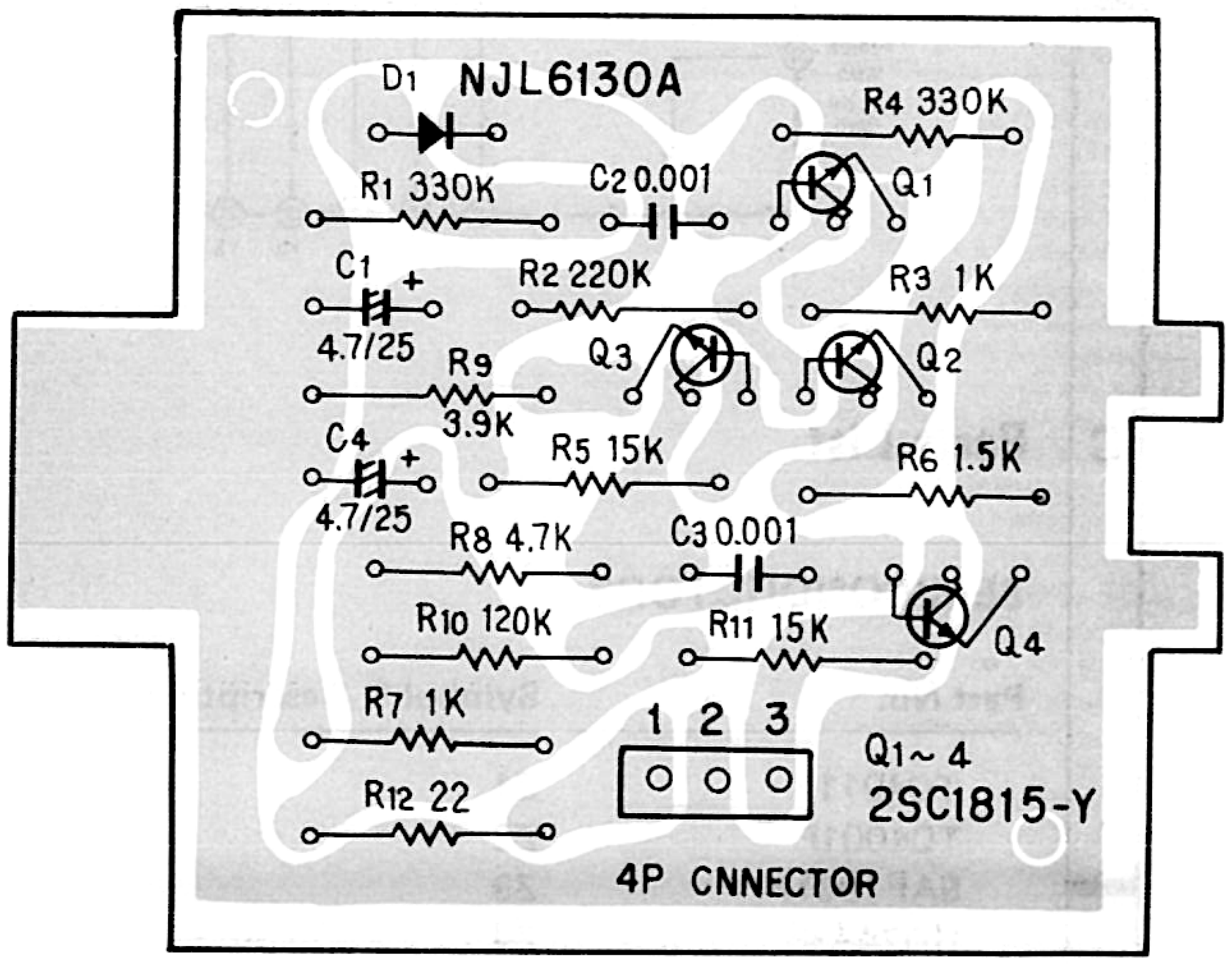
Note: When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

RESISTORS

Part No.	Symbol & Description
RD¼VS □□□J	R1–R17

17.19 SUB INFRARED BOARD ASSEMBLY (VWG-006) (SIRB)





Parts List

SEMICONDUCTORS

Part No.	Symbol & Description
2SC1815-Y	Q1–Q4
NJL6130A	D1

CAPACITOR

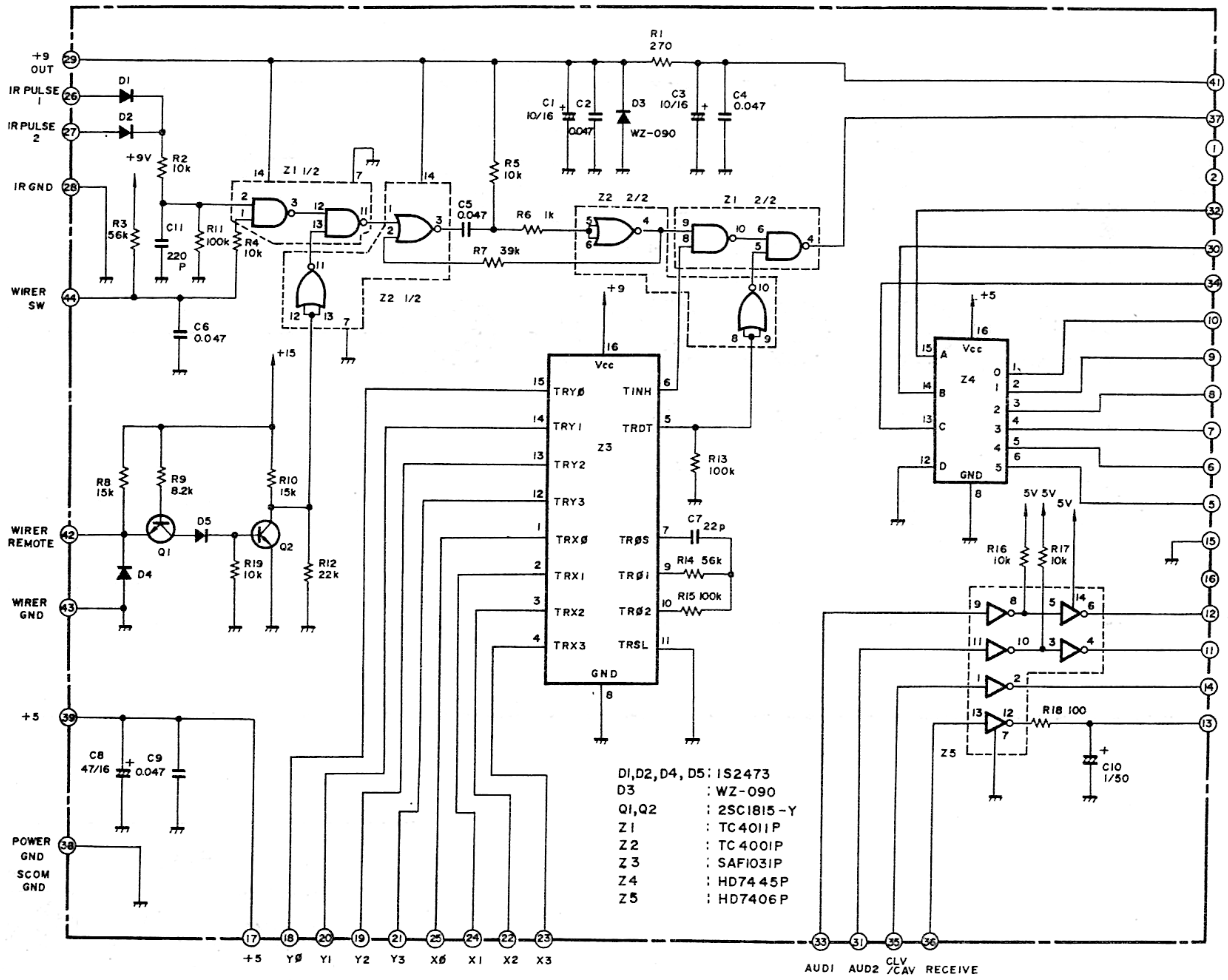
Part No.	Symbol & Description
CSZAH 4R7M 25	C1, C4
CKDYB 102K 50	C2, C3

Note: When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

RESISTORS

Part No.	Symbol & Description
RD¼PS □□□J	R1–R12

17.20 LAMP DRIVER BOARD ASSEMBLY (VWG-007) (LMPD)



Parts List

SEMICONDUCTORS

Part No.	Symbol & Description
TC4011P	Z1
TC4001P	Z2
SAF1031P	Z3
HD7445P	Z4
HD7406P (SN7406N)	Z5
2SC1815-Y	Q1, Q2
1S2473	D1, D2, D4, D5
WZ-090	D3

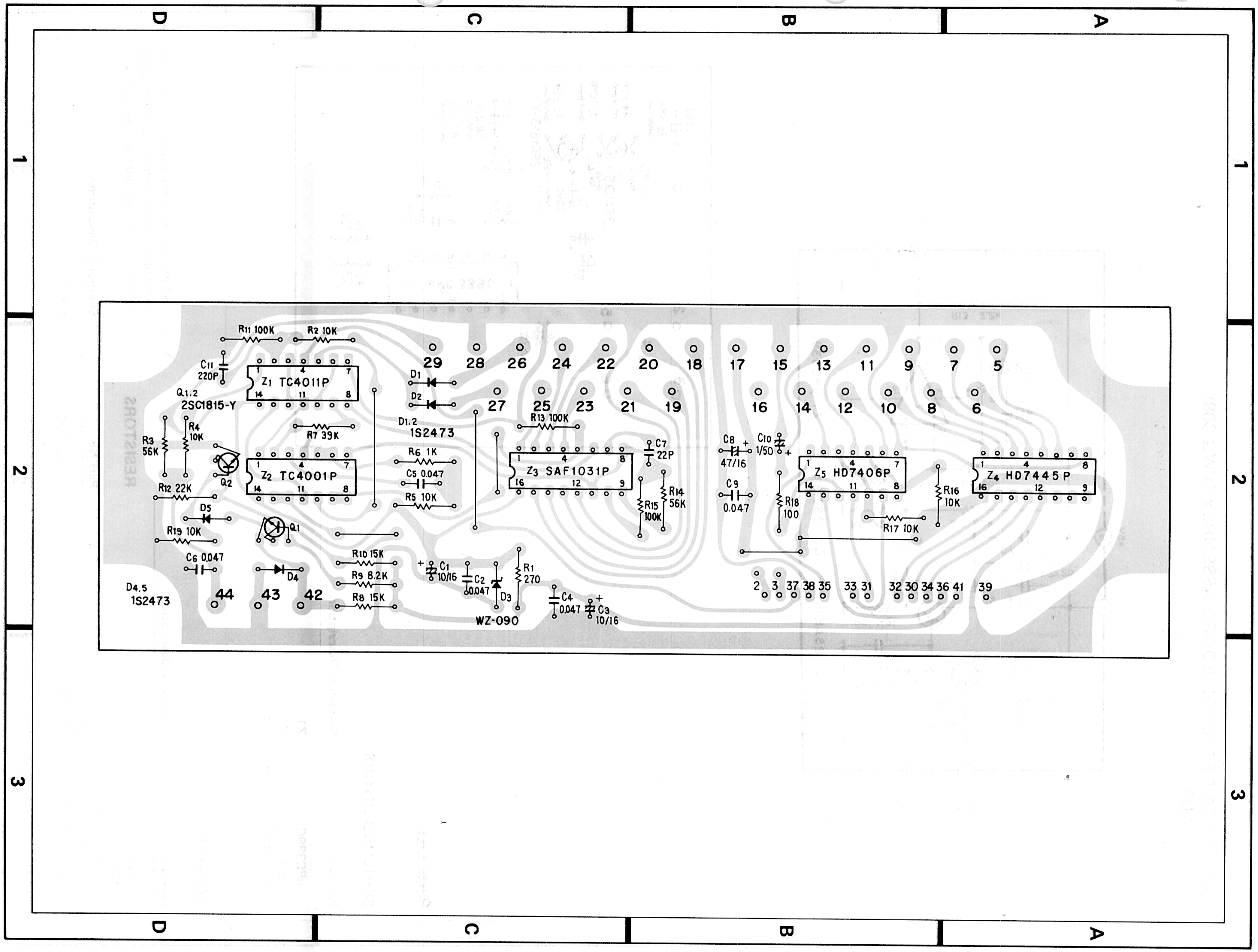
CAPACITORS

Part No.	Symbol & Description
CQSH 220J 50	C7
CKDYF 473Z 50	C2, C4, C9
CCDSL 221Z 50	C11
CQMA 473K 50	C5, C6
CEA 470P 16	C8
CEA 100P 16	C1, C3
CEA 010P 50	C10

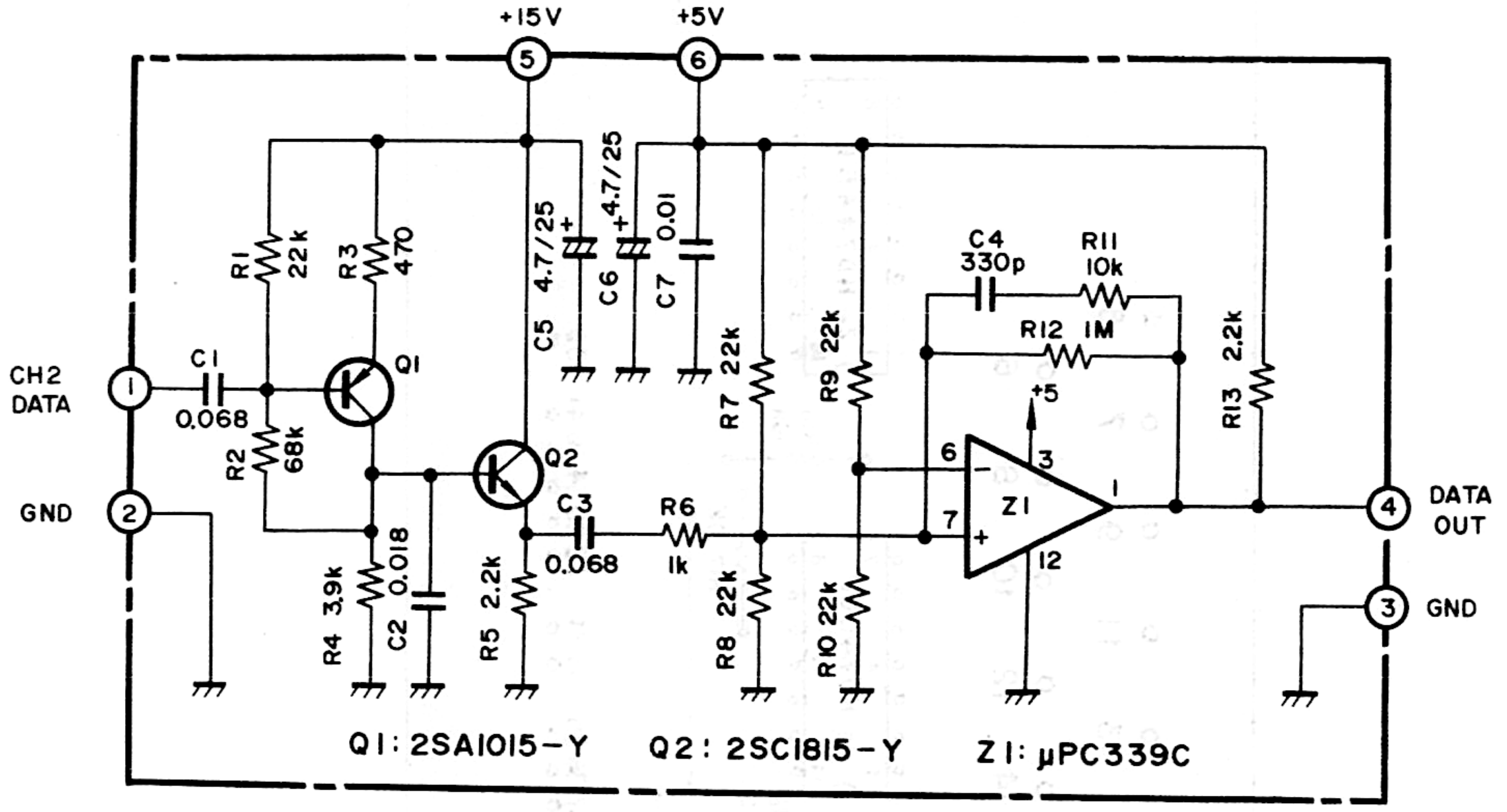
Note: When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

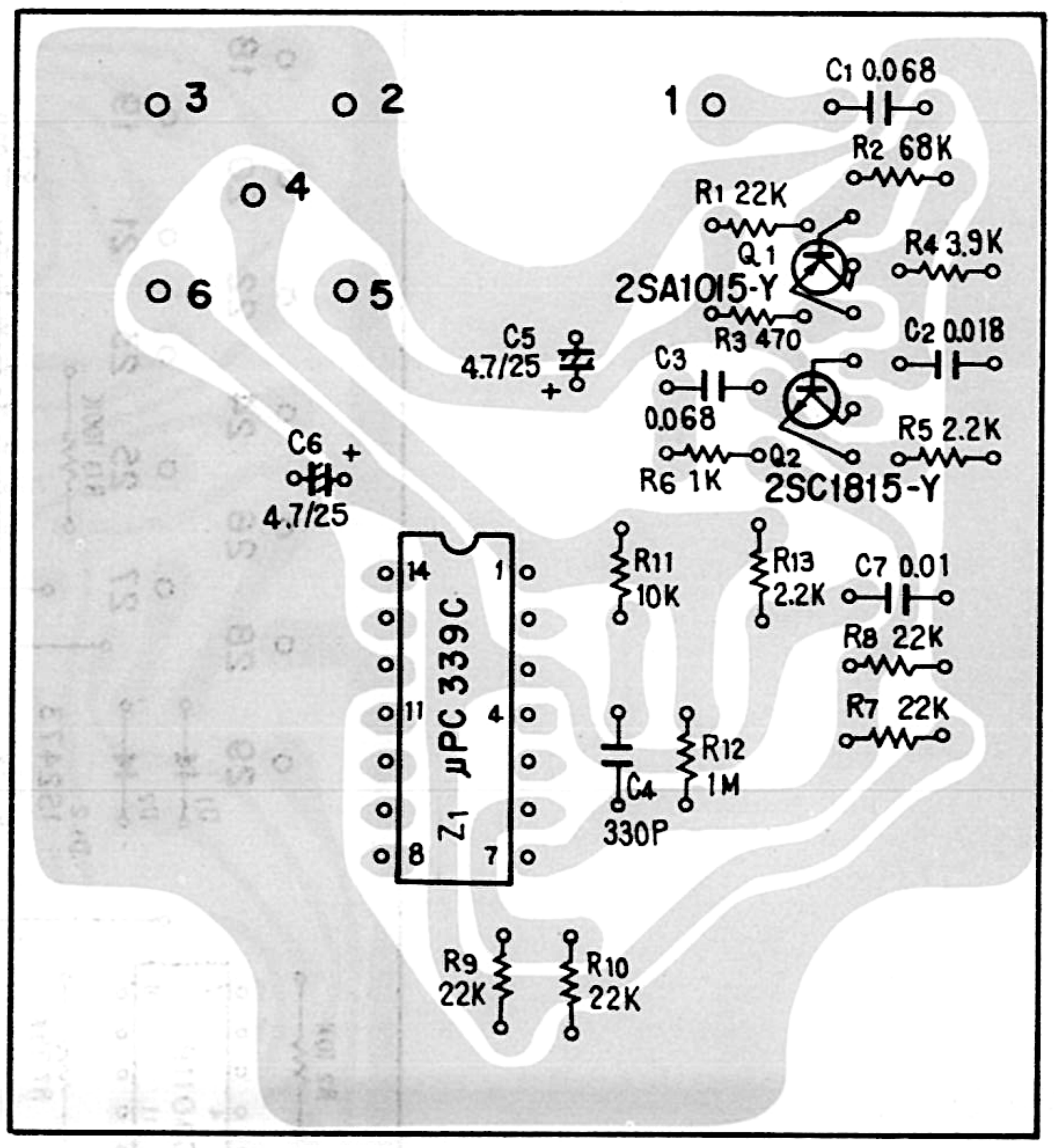
RESISTORS

Part No.	Symbol & Description
RD¼PS □□□J	R1–R8, R9–R13, R15–R19
RN¼PR □□□□F	R14


D
C
B
A
1
2
3
R11 100K
R2 10K
C11
220P
Z1 TC4011P
Q1,2
2SC1815-Y
R3
56K
R4
10K
R7 39K
Z2 TC4001P
Q2
R12 22K
D5
R19 10K
Q1
C6 0.047
D4
D4,5
1S2473
44
43
42
D1
D2
D1,2
1S2473
R6 1K
C5 0.047
R5 10K
R10 15K
R9 8.2K
R8 15K
C1
10/16
C2
0.047
D3
WZ-090
R1
270
C4
0.047
C3
10/16
29
28
26
24
22
20
18
17
15
13
11
9
7
5
27
25
23
21
19
16
14
12
10
8
6
R13 100K
Z3 SAF1031P
C7
22P
R15
100K
R14
56K
C8
47/16
C10
1/50
C9
0.047
R18
100
Z5 HD7406P
R16
10K
R17 10K
Z4 HD7445P
2
3
37
38
35
33
31
32
30
34
36
41
39

17.21 DATA DETECTOR BOARD ASSEMBLY (VWG-008) (DADT)





Parts List

SEMICONDUCTORS

Part No.	Symbol & Description
μPC339C	Z1
2SA1015-Y	Q1
2SC1815-Y or O	Q2

CAPACITORS

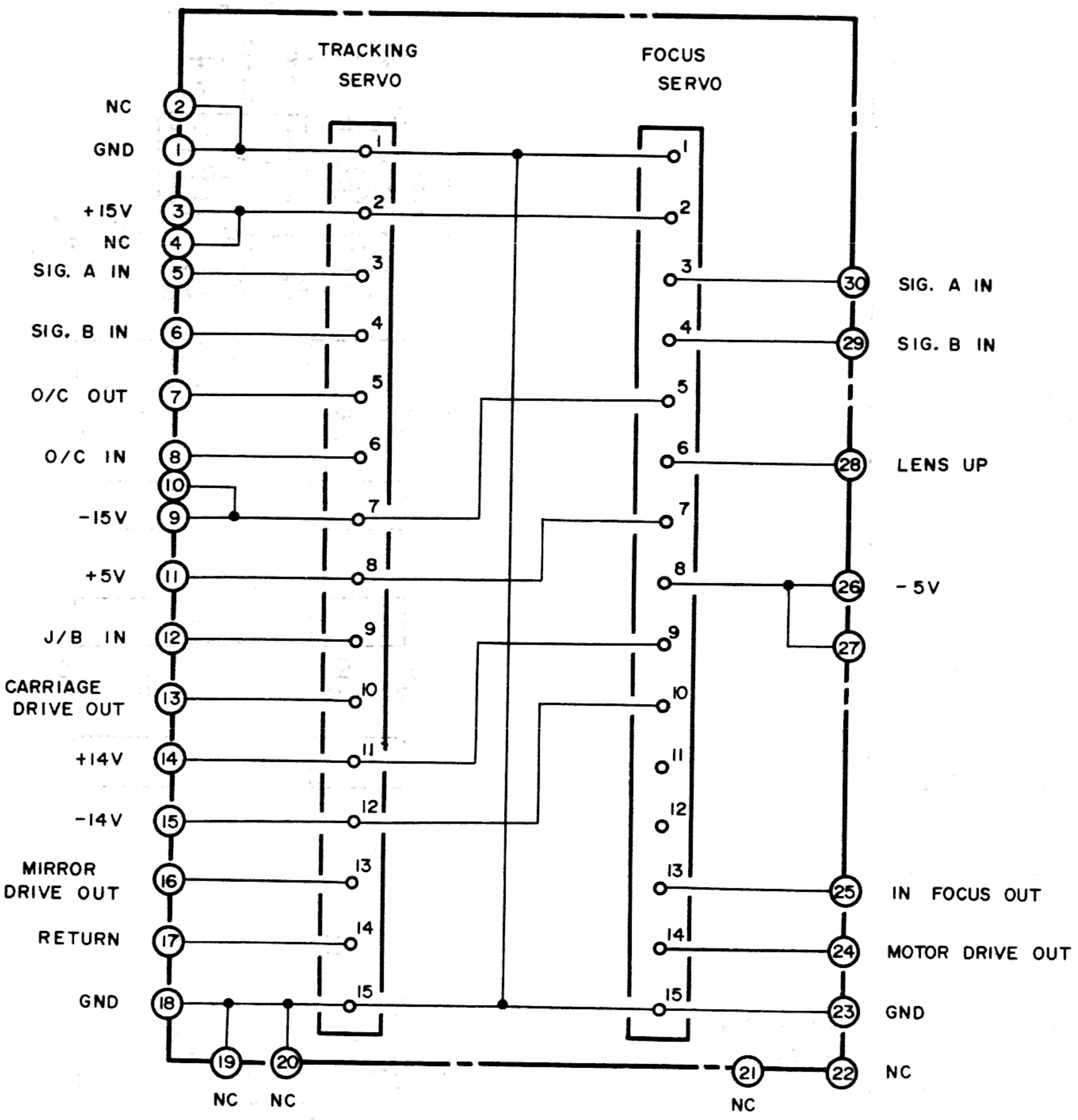
Part No.	Symbol & Description
CQMA 683K 50	C1, C3
CQMA 183K 50	C2
CKDYF 103Z 50	C7
CCDYF 331Z 50	C4
CEA 4R7P 25	C5, C6

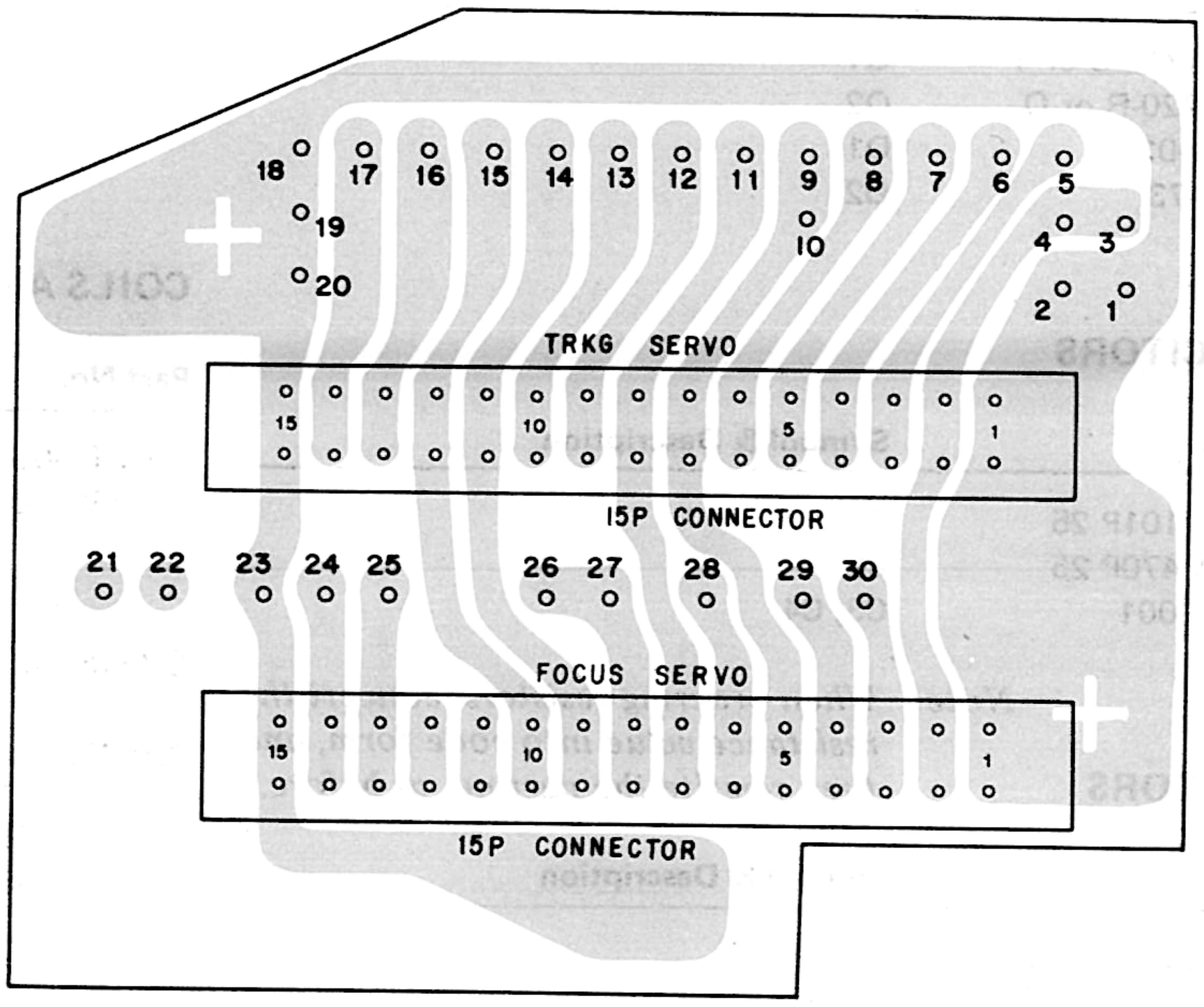
Note: When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

RESISTORS

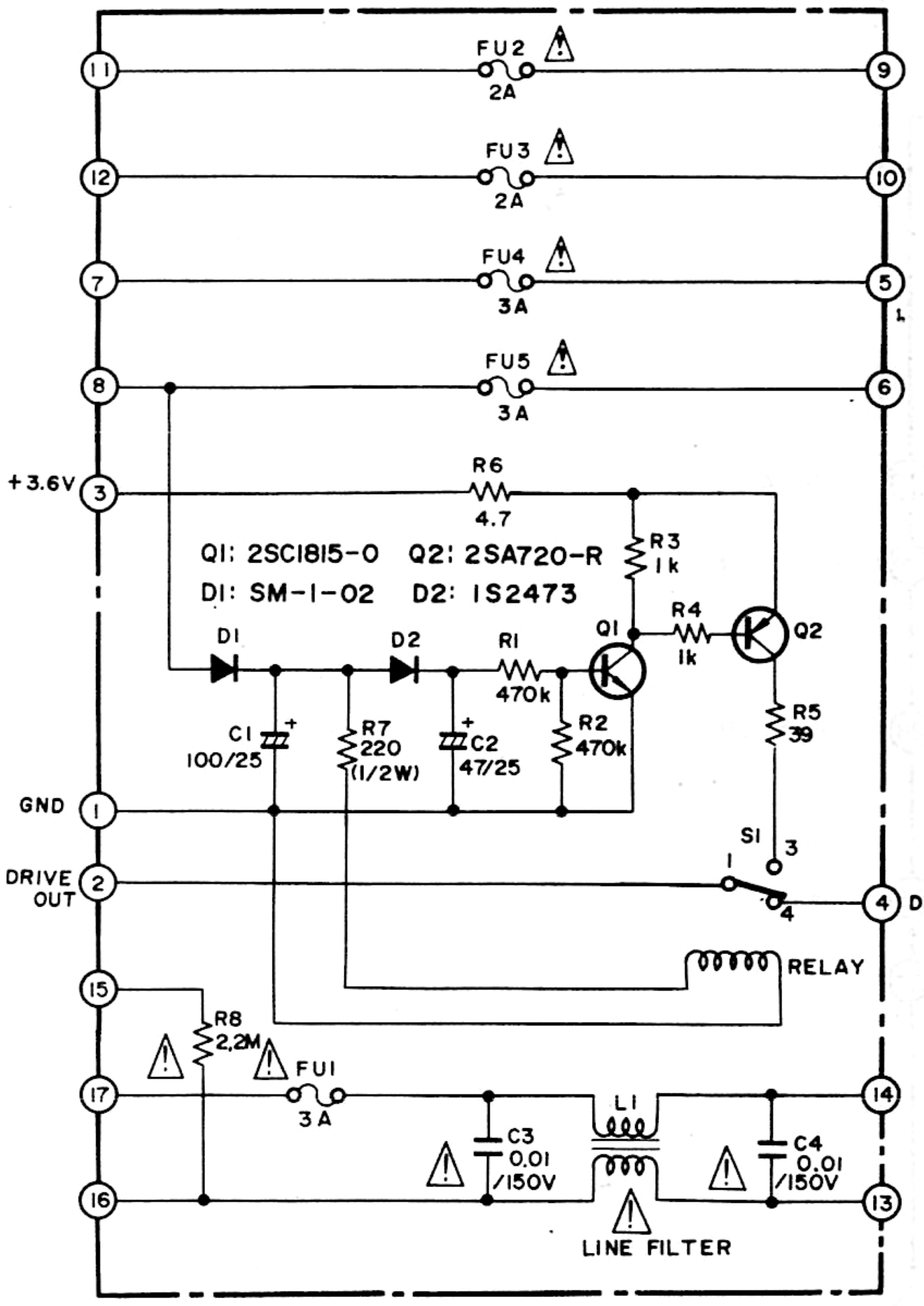
Part No.	Symbol & Description
RD¼VS □□□J	R1–R13

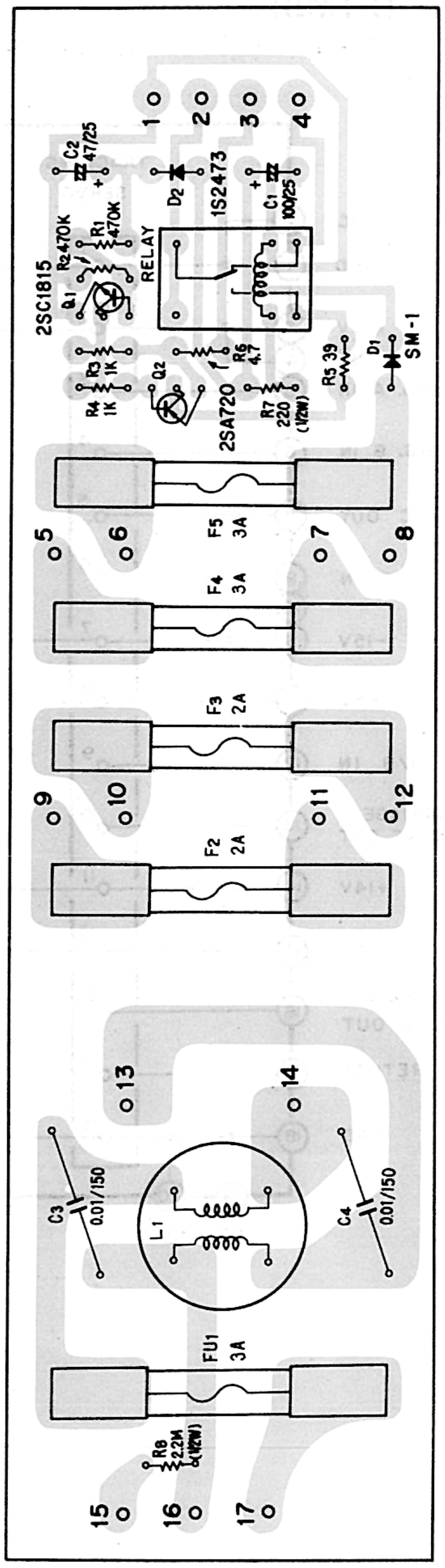
17.22 FOCUS & TRACKING MOTHER BOARD ASSEMBLY (VWX-002) (FTMB)





17.23 FUSE & FOCUS MOTOR PROTECTOR ASSEMBLY (VWR-004) (FFMP)





Parts List

- *Parts without part number cannot be supplied.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*

SEMICONDUCTORS

Part No.	Symbol & Description
2SC1815-O or Y	Q1
2SA720-R or Q	Q2
SM-1-02	D1
1S2473	D2

CAPACITORS

Part No.	Symbol & Description
CEA 101P 25	C1
CEA 470P 25	C2
⚠VCG-001	C3, C4

Note: When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

RESISTORS

Part No.	Symbol & Description
RD¼VS □□□J	R1–R6
⚠RD½VS □□□J	R7, R8

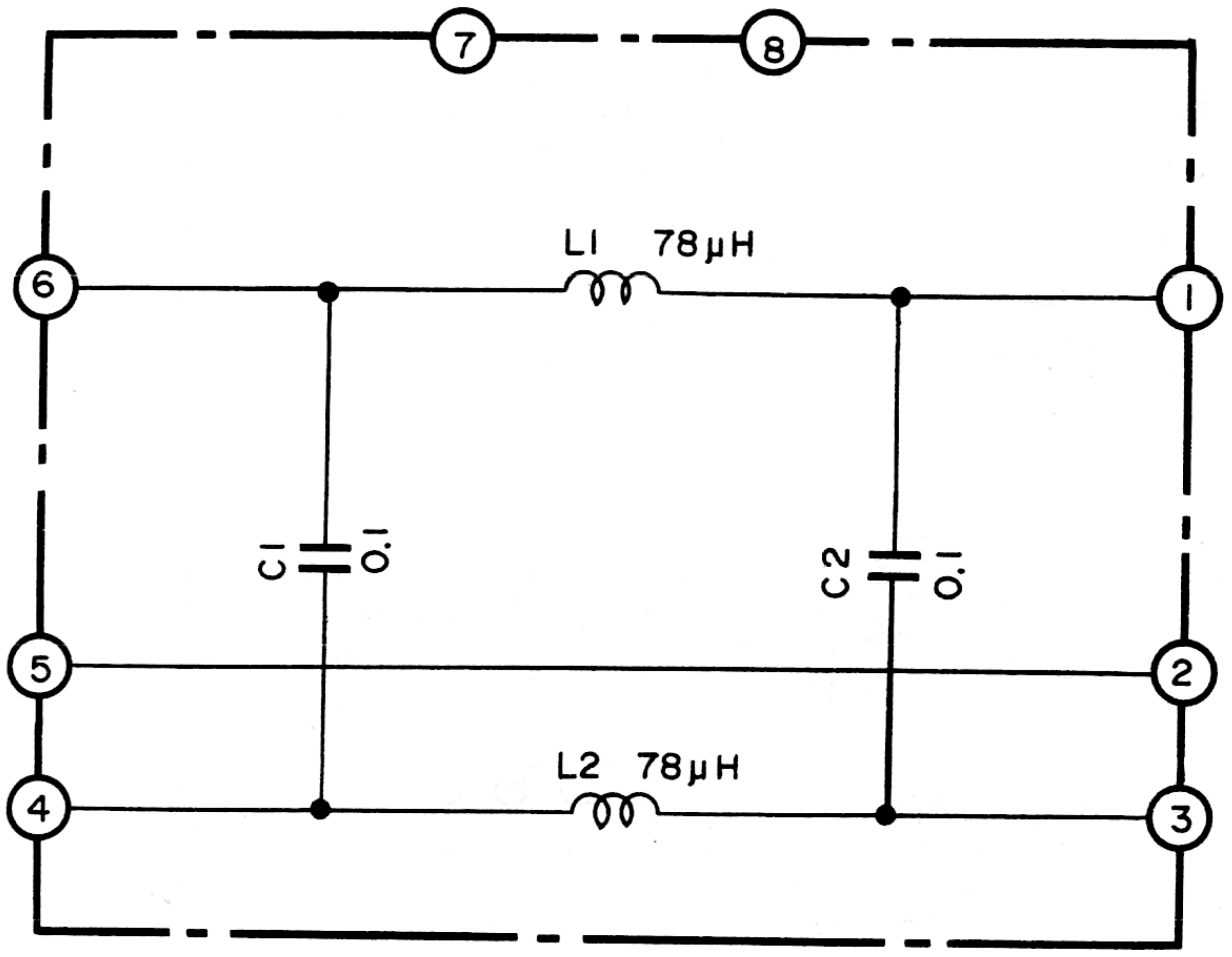
COILS AND TRANSFORMERS

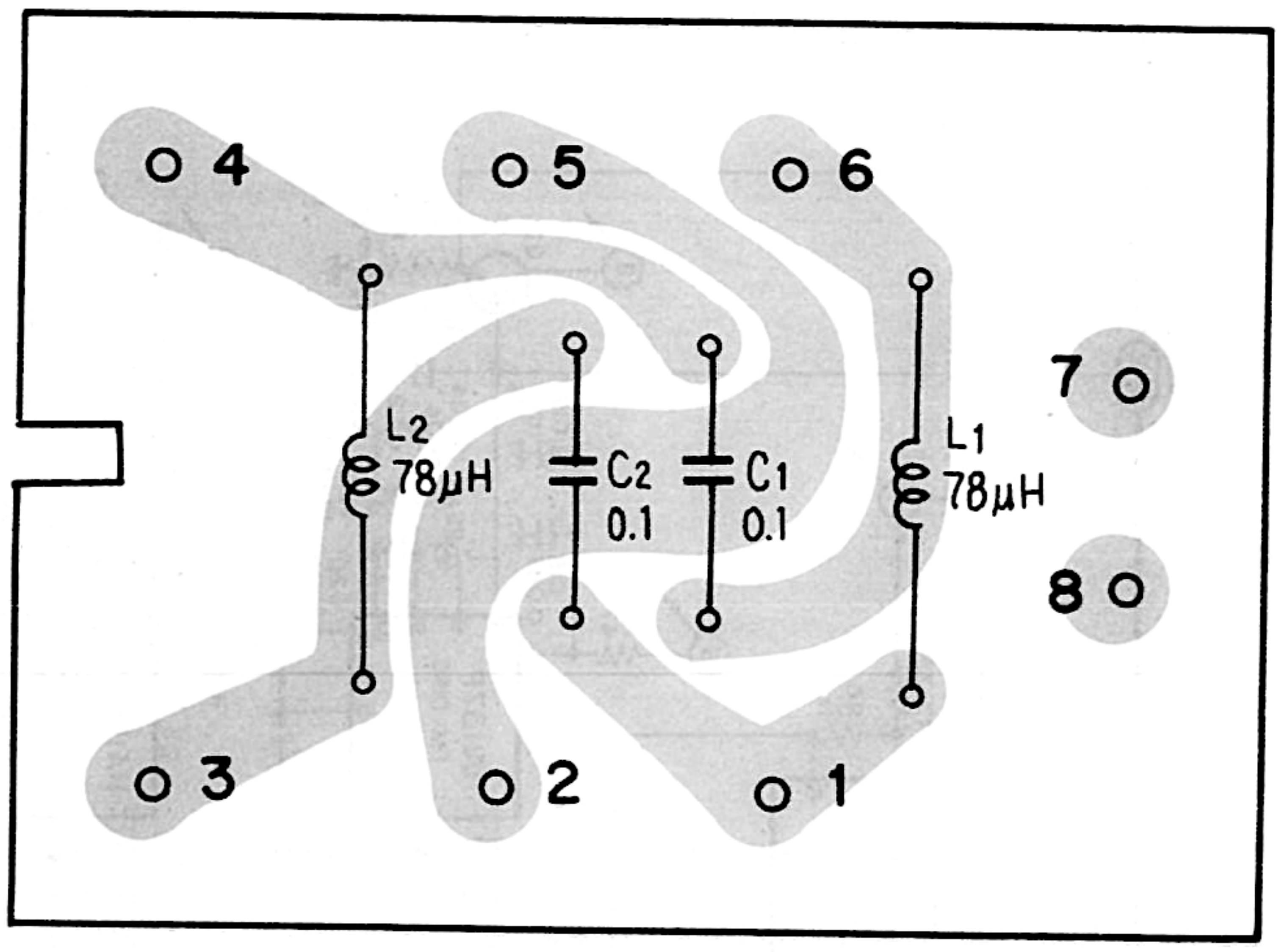
Part No.	Symbol & Description
⚠VTL-001	L1
VSR-001	S1

OTHERS

Part No.	Symbol & Description
VEK-003	FU1, FU4, FU5
VEK-004	FU2, FU3

17.24 NOISE FILTER PRINTED BOARD ASSEMBLY (VWY-003) (NFPB)





Parts List

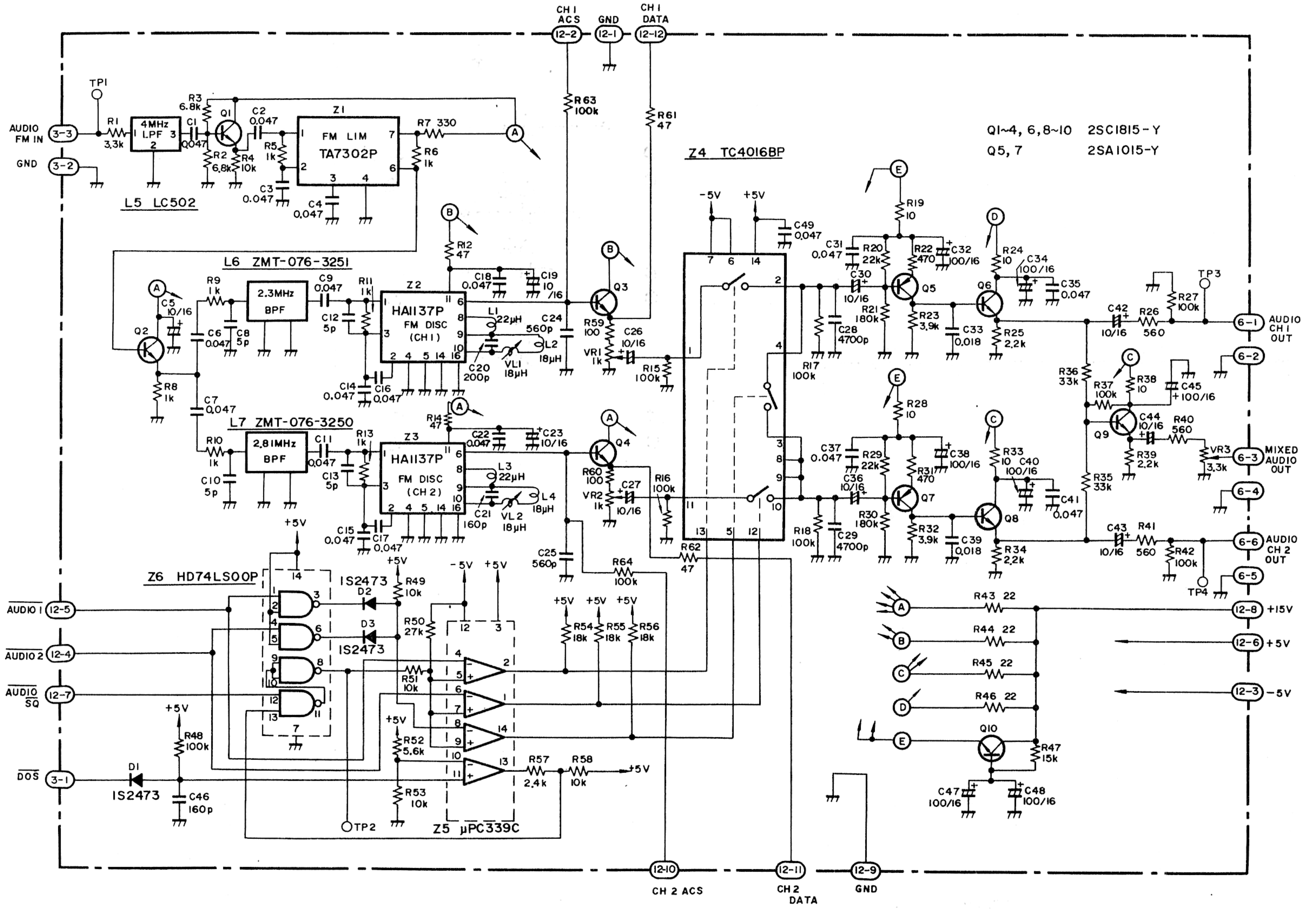
COILS AND TRANSFORMERS

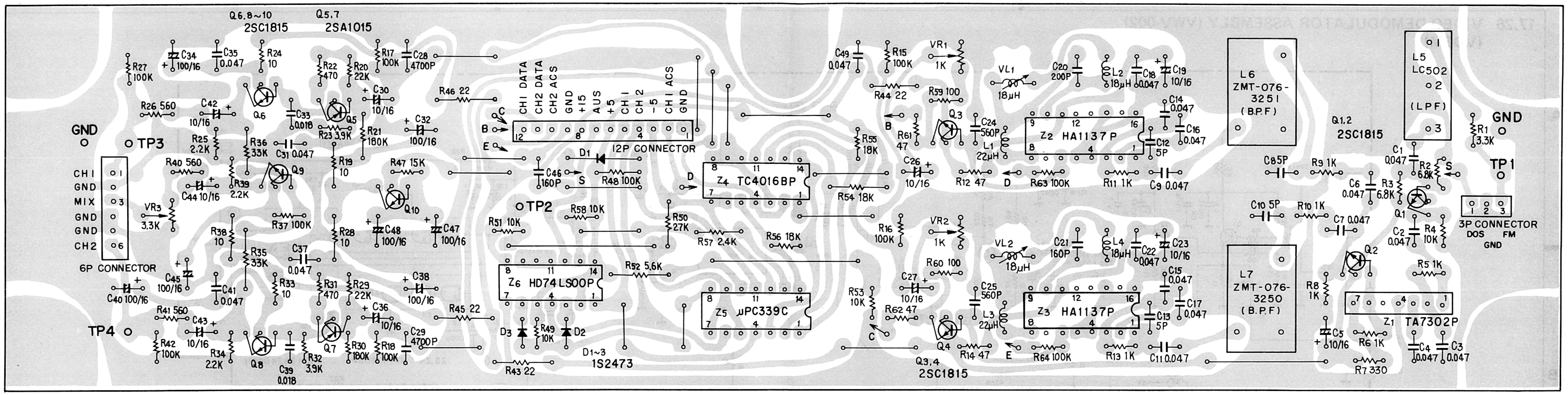
Part No.	Symbol & Description
VTF-008	L1, L2

CAPACITORS

Part No.	Symbol & Description
CKDYF 104Z 50	C1, C2

17.25 AUDIO BOARD ASSEMBLY (VWV-003) (AUDB)





Parts List

SEMICONDUCTORS

Part No.	Symbol & Description
TA7302P	Z1
HA1137P	Z2, Z3
TC4016BP	Z4
μPC339C	Z5
HD74LS00P	Z6
2SC1815-Y or O	Q1–Q4, Q6, Q8–Q10
2SA1015-Y or O	Q5, Q7
1S2473	D1–D3

CAPACITORS

Part No.	Symbol & Description
CKDYF 473Z 50	C1–C4, C6, C7, C9, C11, C14–C18, C22, C31, C35, C37, C41, C49
CCDSL 561J 50	C24, C25
CCDSL 050C 50	C8, C10, C12, C13
CCDSL 161J 50	C46
CQMA 183J 50	C33, C39
CQSH 161J 50	C21
CEA 101P 16	C32, C34, C38, C40, C45, C47, C48
CEA 100P 16	C5, C19, C23, C26, C27, C30, C36, C42 C43, C44
CQMA 472K 50	C28, C29
CQSH 201J 50	C20

RESISTORS

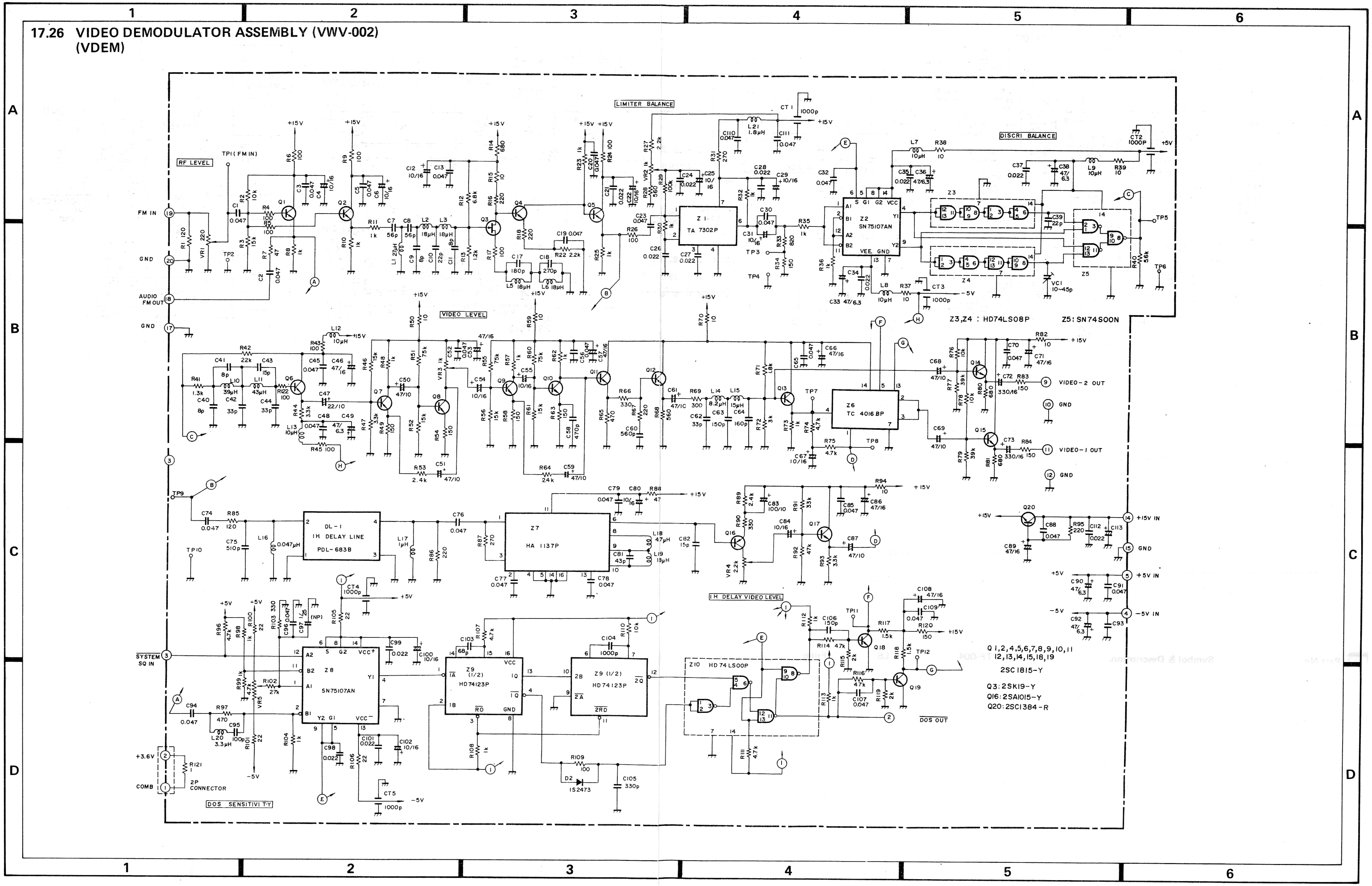
Note: When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

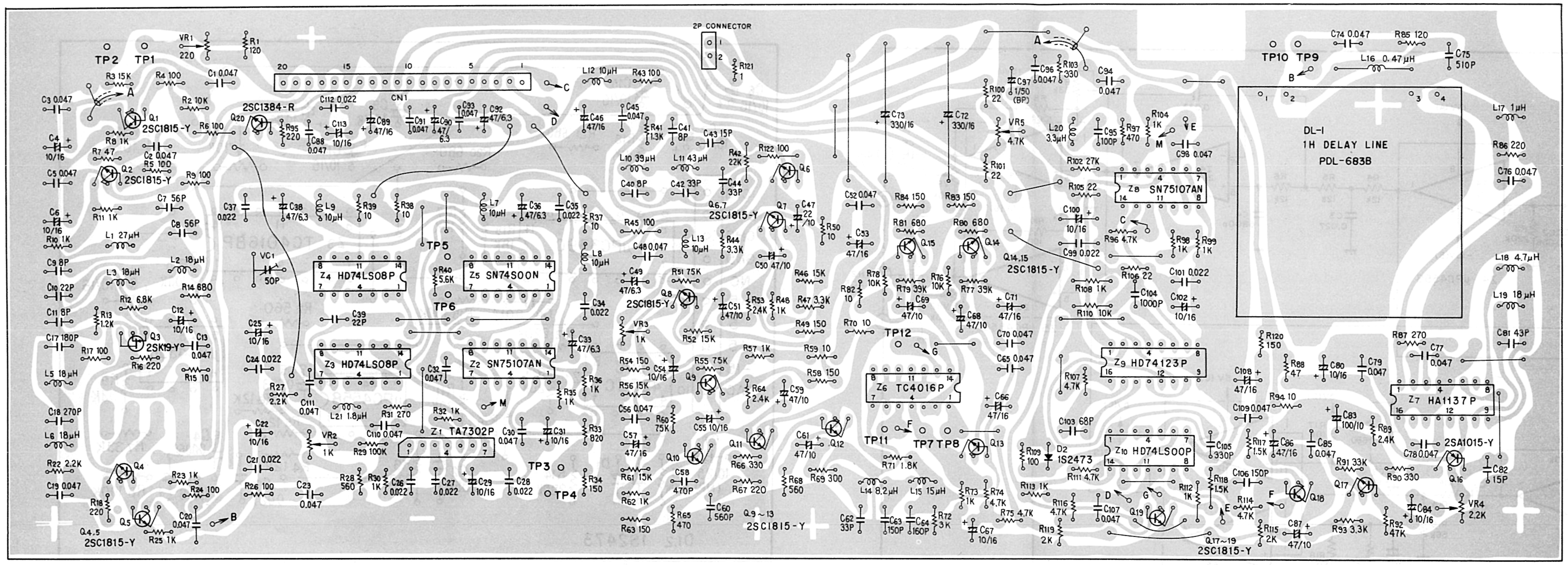
Part No.	Symbol & Description	
RD¼VS □□□J	R1–R64	
VCP-034	VR3	Semi-fixed
VCP-024	VR1, VR2	Semi-fixed

COILS AND TRANSFORMERS

Part No.	Symbol & Description	
VTL-027	L1, L3	Coil
VTL-026	L2, L4	Coil
VTF-006	VL1, VL2	Coil
VTF-003	L5	Filter
VTF-004	L6	Filter
VTF-005	L7	Filter

17.26 VIDEO DEMODULATOR ASSEMBLY (VWV-002)
(VDEM)





Parts List

SEMICONDUCTORS

Part No.	Symbol & Description
TA7302P	Z1
SN75107AN	Z2, Z8
HD74LS08P	Z3, Z4
SN74S00N	Z5
TC4016BP	Z6
HA1137P	Z7
HD74LS00P	Z10
HD74123P	Z9
(SN74123N)	
2SC1815-Y	Q1–Q2, Q4–Q15, Q17–Q19
2SA1015-Y or O	Q16
2SK19-Y	Q3
2SC1384-R	Q20
1S2473	D2

RESISTORS

Note: When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

Part No.	Symbol & Description	
RD¼VS □□□J	R1–R18, R22–R108, R110–R120, R122	
VCP-022	VR1	Semi-fixed
VCP-024	VR2, VR3	Semi-fixed
VCP-025	VR4	Semi-fixed
VCP-026	VR5	Semi-fixed

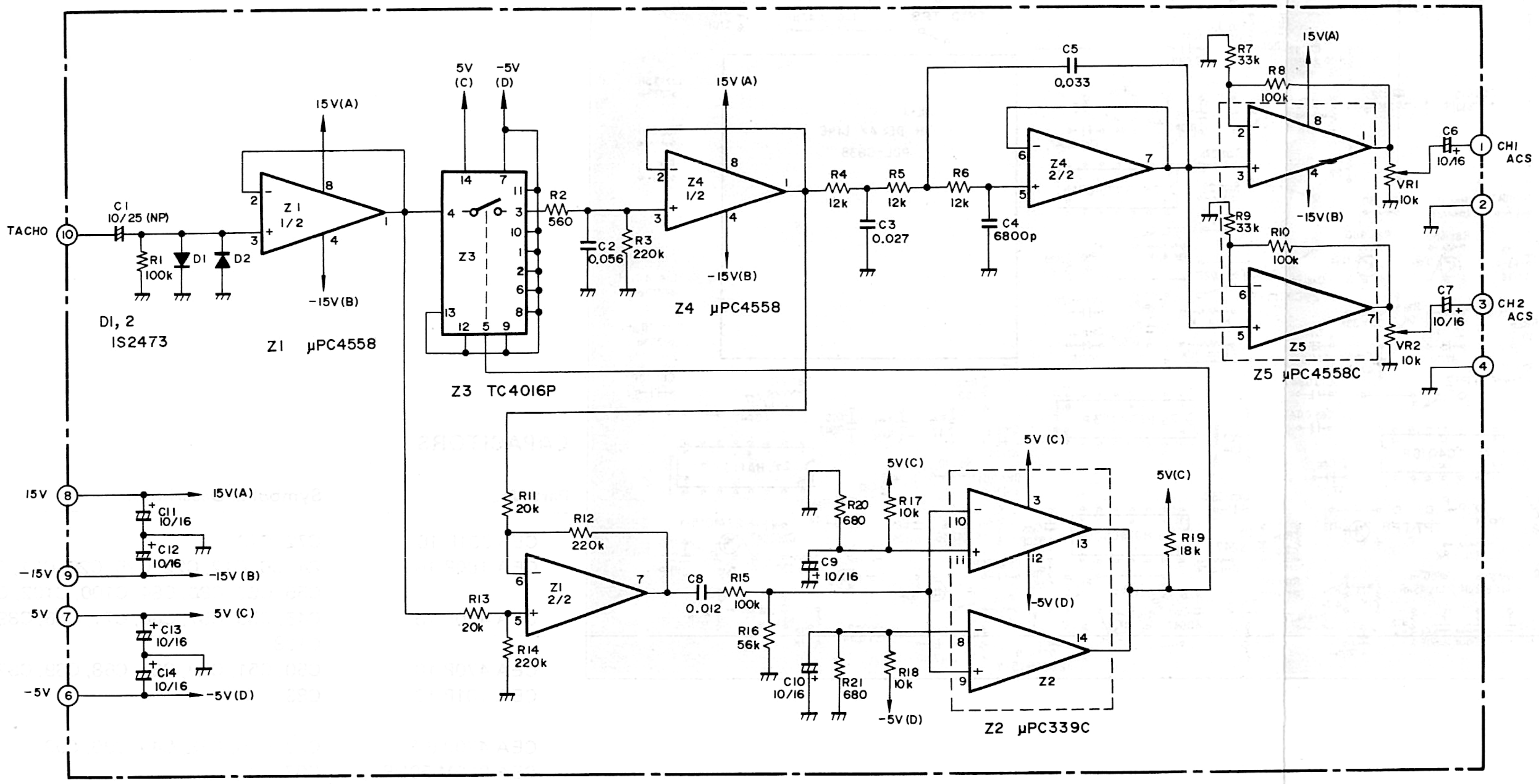
COILS AND TRANSFORMERS

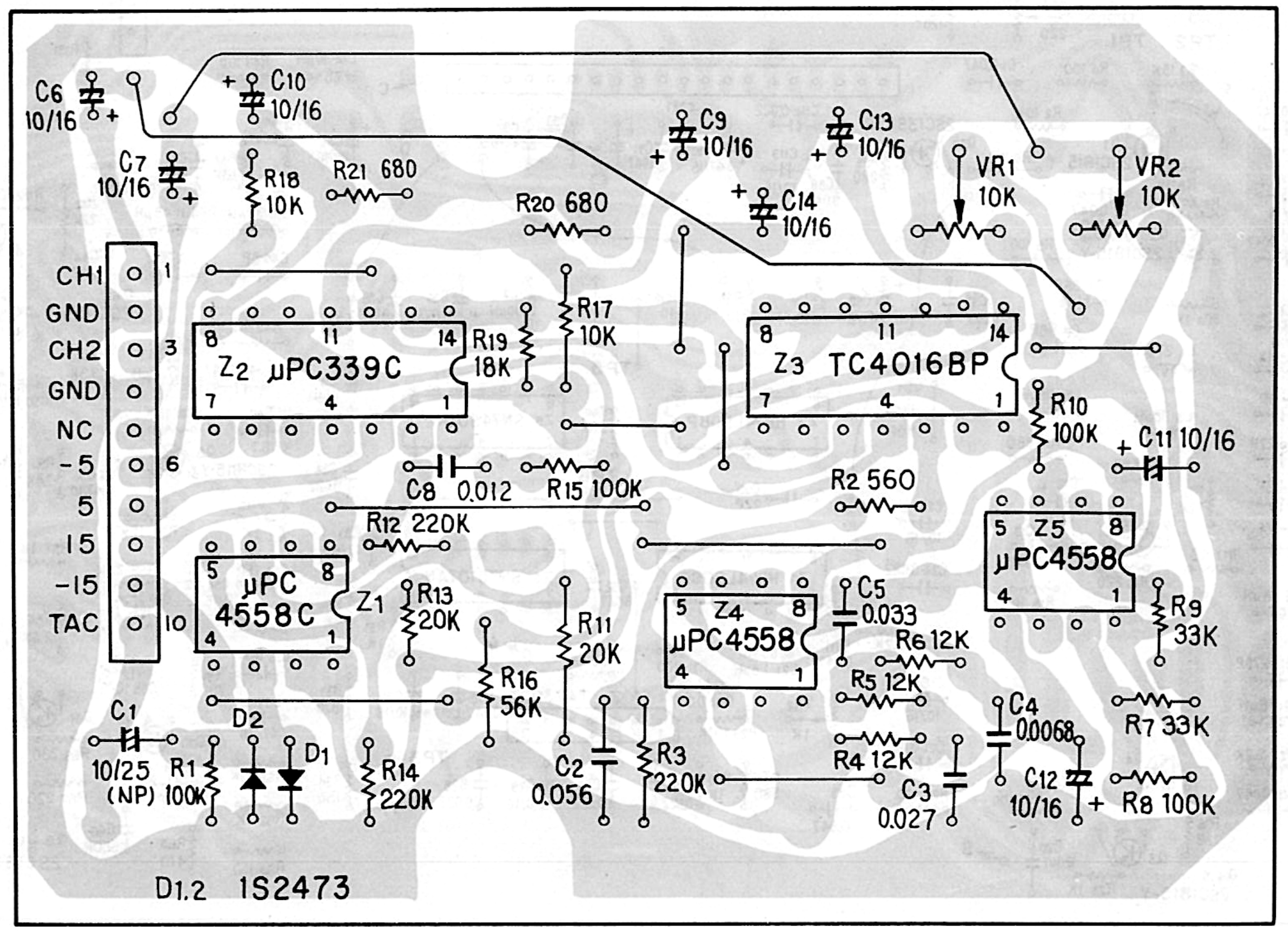
Part No.	Symbol & Description	
VTL-011	L17	Coil
VTL-017	L20	Coil
VTL-019	L18	Coil
VTL-022	L14	Coil
VTL-023	L7–L9, L12, L13	Coil
VTL-025	L15	Coil
VTL-026	L2, L3, L5, L6, L19	Coil
VTL-028	L1	
VTL-030	L10	
VTL-051	L11	
VTL-014	L21	
VTF-009	L16	Peaking coil
VTF-007	DL1	Delay line

CAPACITORS

Part No.	Symbol & Description	
CEB 331P 16	C72, C73	
CEA 100P 16	C4, C6, C12, C22, C25, C29, C31, C54, C55, C67, C80, C84, C100, C102, C113	
CEA 470P 16	C46, C53, C57, C66, C71, C86, C89, C108	
CEA 470P 10	C50, C51, C59, C61, C68, C69, C87	
CEA 101P 10	C83	
CEA 470P 6.3	C33, C36, C38, C49, C90, C92	
CEA 010M 50NP	C97	
CEA 220P 10	C47	
CKDYF 473Z 50	C1–C3, C5, C13, C19, C20, C23, C30, C32, C45, C48, C52, C56, C65, C70, C74, C76–C79, C85, C88, C91, C93, C94, C96, C107, C109–C111	
CCDCH 080D 50	C9, C11, C40, C41	
CCDCH 150J 50	C82	
CCDSL 101J 50	C95	
CCDSL 511J 50	C75	
CKDYF 223Z 50	C21, C24, C26–C28, C34, C35, C37, C98, C99, C101, C112	
CQSH 150J 50	C43	
CQSH 220J 50	C10, C39	
CQSH 330J 50	C42, C44, C62	
CQSH 430J 50	C81	
CQSH 560J 50	C7, C8	
CQSH 680J 50	C103	
CQSH 151J 50	C63, C106	
CQSH 161J 50	C64	
CQSH 181J 50	C17	
CQSH 271J 50	C18	
CQSH 331J 50	C105	
CQMA 102K 50	C104	
CQSH 471J 50	C58	
CQSH 561J 50	C60	
VCM-001	VC1	Ceramic trimmer

17.27 AUDIO COMPENSATOR ASSEMBLY (VWV-004) (ACOM)





Parts List

SEMICONDUCTORS

Part No.	Symbol & Description
TC4016P	Z3
μPC339C	Z2
μPC4558C	Z1, Z4, Z5
1S2473	D1, D2

CAPACITORS

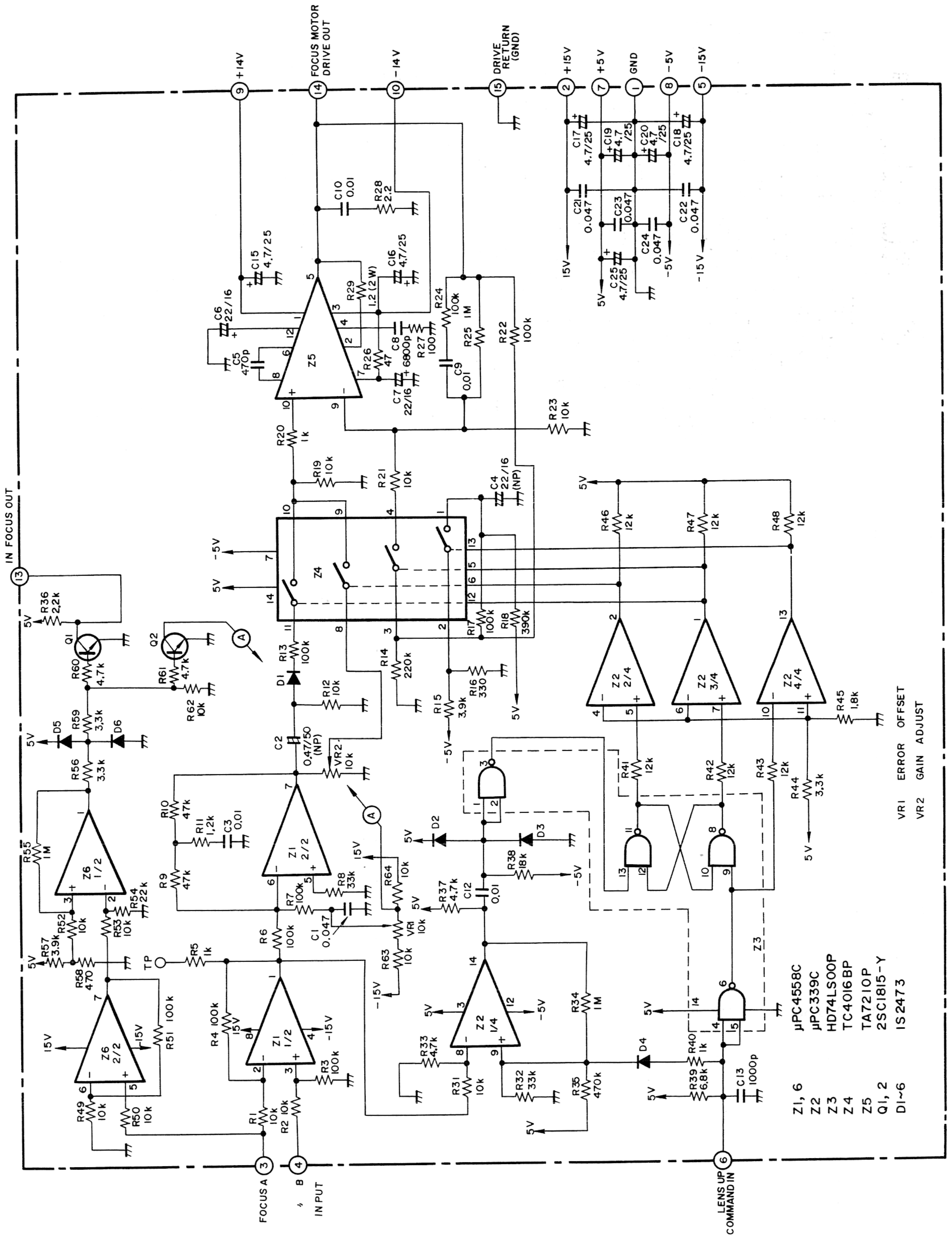
Part No.	Symbol & Description
CQMA 563K 50	C2
CQMA 273K 50	C3
CQMA 682K 50	C4
CQMA 333K 50	C5
CQMA 123K 50	C8
CEA 100P 16	C6, C7, C9–C14
CEA 100M 25NP	C1

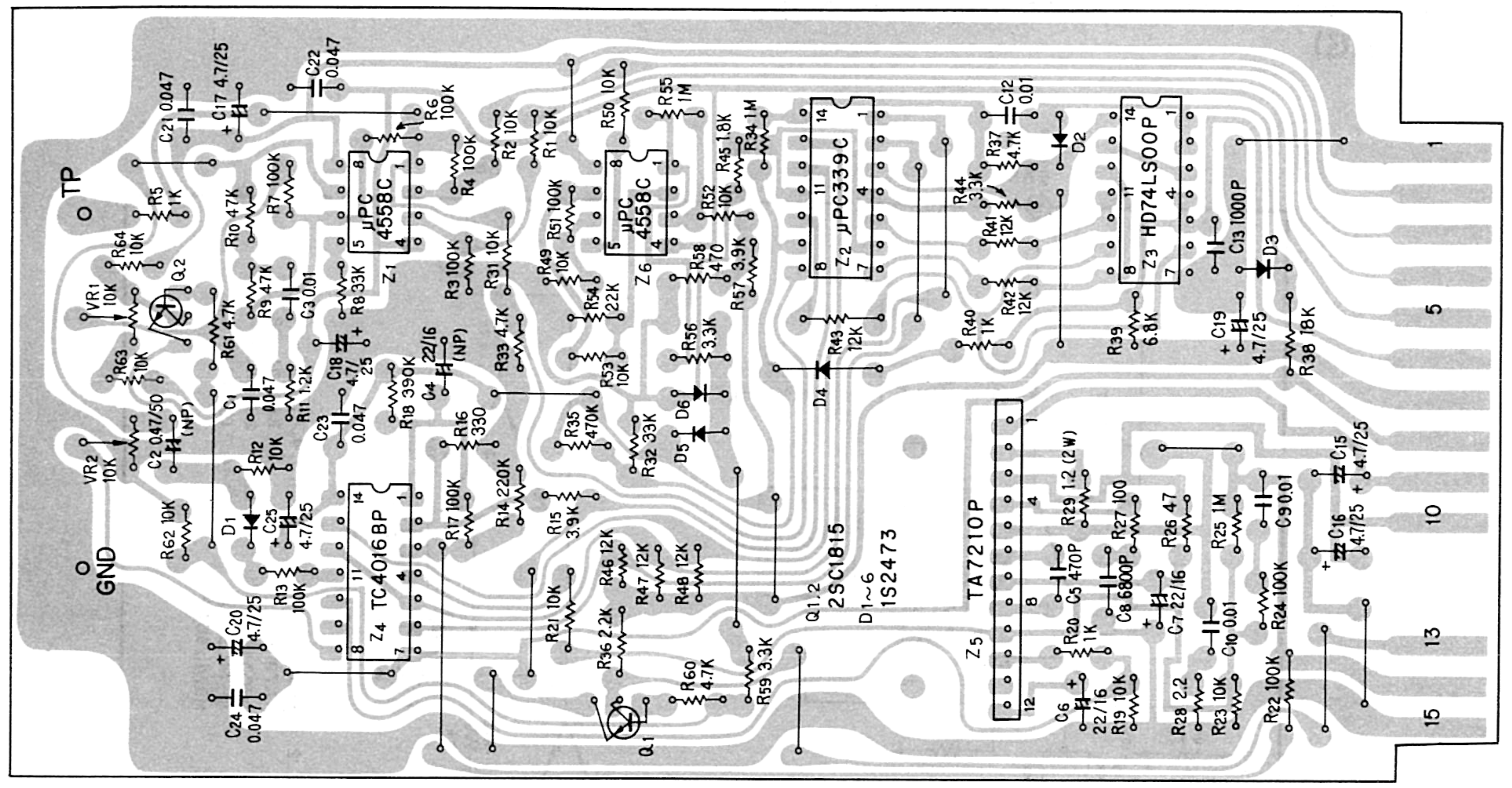
Note: When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

RESISTORS

Part No.	Symbol & Description
RD¼VE □□□J	R1–R21
VCP-007	VR1, VR2 Semi-fixed

17.28 FOCUS SERVO ASSEMBLY (VWS-001) (FOCS)





Parts List

SEMICONDUCTORS

Part No.	Symbol & Description
μPC4558C	Z1, Z6
μPC339C	Z2
HD74LS00P	Z3
TC4016BP	Z4
TA72109	Z5
2SC1815-Y or O	Q1, Q2
1S2473	D1–D6

CAPACITORS

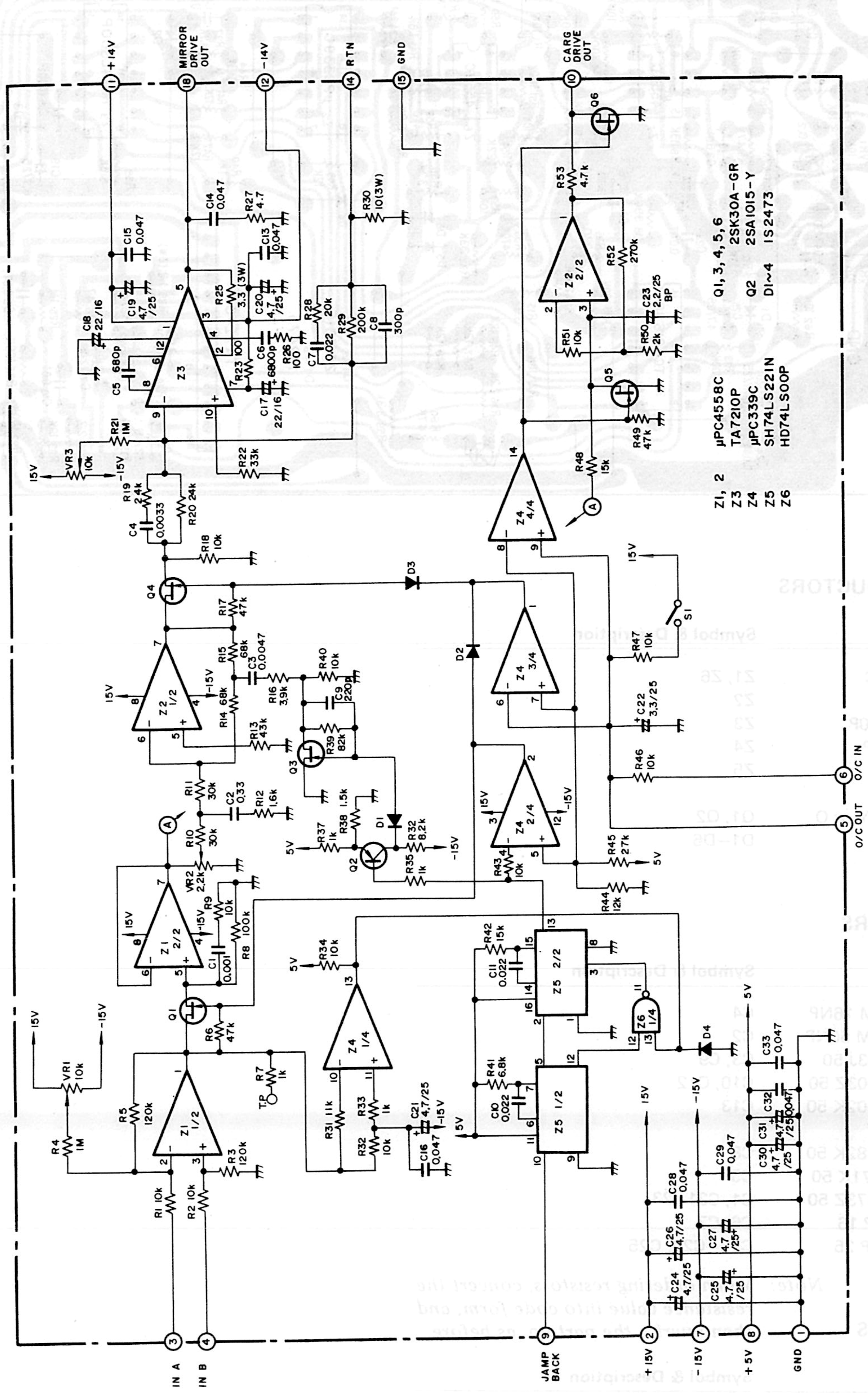
Part No.	Symbol & Description
CEA 220M 16NP	C4
CEAR 47M 50NP	C2
CQMA 103J 50	C3, C9
CKDYF 103Z 50	C10, C12
CKDYB 102K 50	C13
CKDYB 682K 50	C8
CCDSL 471K 50	C5
CKDYF 473Z 50	C1, C21–23
CEA 220P 16	C6, C7
CEA 4R7P 25	C15–C20, C25

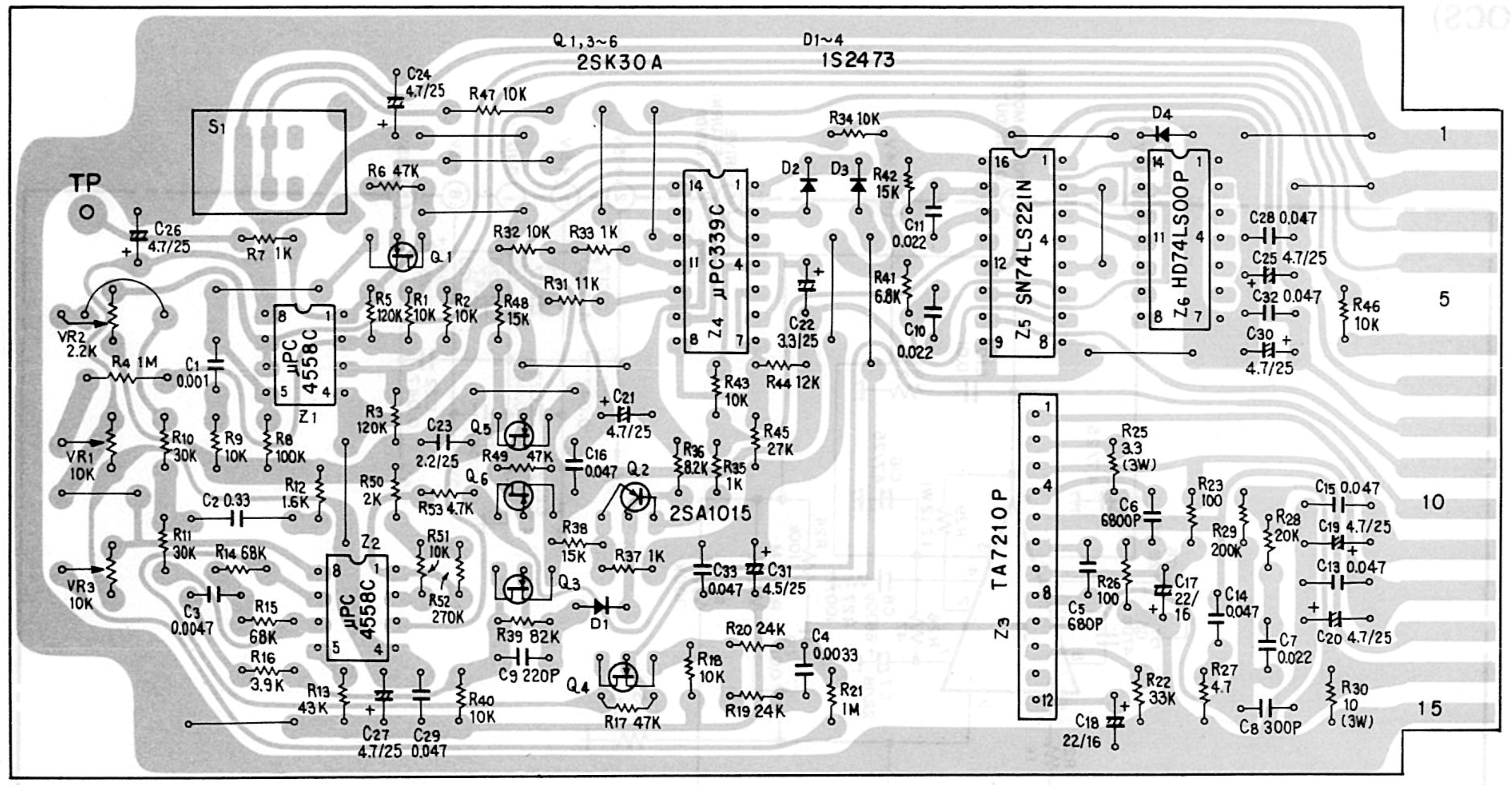
Note: *When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.*

RESISTORS

Part No.	Symbol & Description
RD¼VS □□□J	R1–R28, R31–R64
VCP-007	VR1, VR2 Semi-fixed
VCN-009	R29

17.29 TRACKING SERVO ASSEMBLY (VWS-002) (TRKG)





Parts List

SEMICONDUCTORS

Part No.	Symbol & Description
µPC4558C	Z1, Z2
µPC339C	Z4
TA2109	Z3
SN74LS221N	Z5
HD74LS00P	Z6
2SK30A-GR or Y	Q1, Q3, Q4–Q6
2SA1015-Y or O	Q2
1S2473	D1–D4

CAPACITORS

Part No.	Symbol & Description
CQMA 102J 50	C1
CQMA 334J 50	C2
CQMA 472J 50	C3
CQMA 332J 50	C4
CQMA 223J 50	C7, C10, C11
CQSH 301J 50	C8
CQSH 221J 50	C9
CKDYF 473Z 50	C13–C16, C28, C29, C32, C33
CCDSL 681K 50	C5
CKDYB 682K 50	C6
CEA 4R7P 25	C19, C20, C21, C24–C27, C30, C31
CEA 220P 16	C17, C18
CEA 3R3P 25	C22
CEA 2R2M 25NP	C23

Note: *When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.*

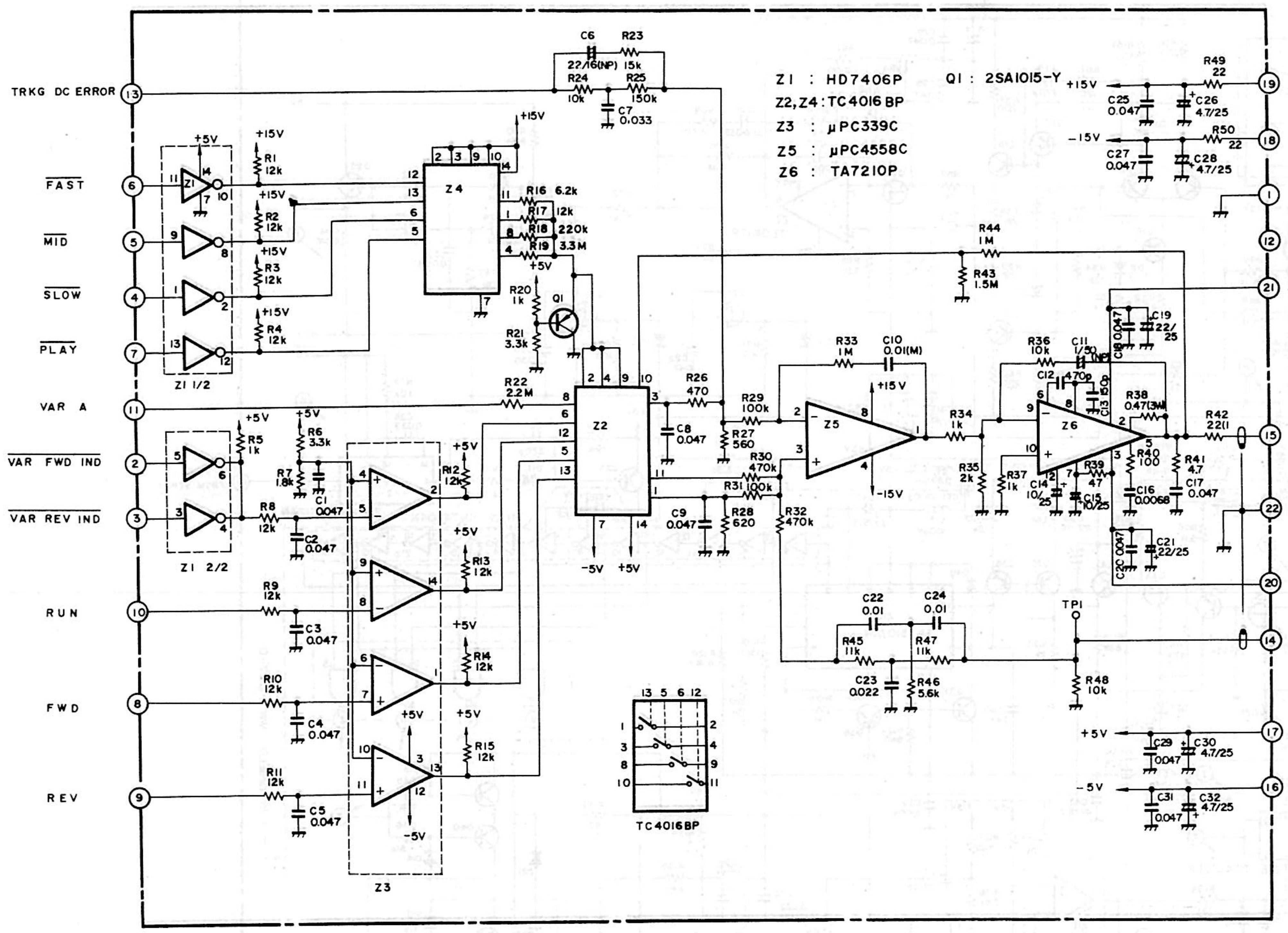
RESISTORS

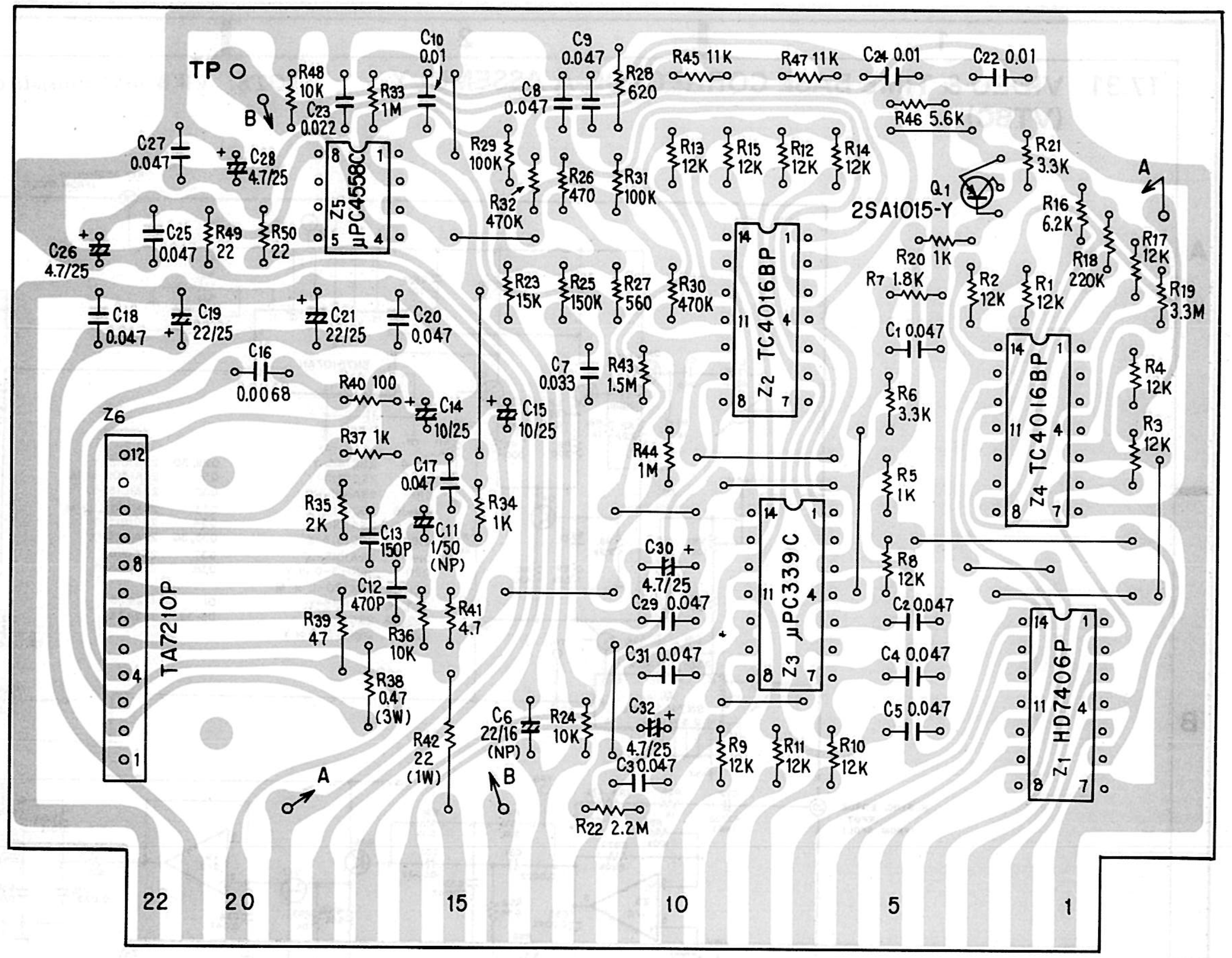
Part No.	Symbol & Description	
RD¼VS □□□J	R1–R23, R26–R29, R31–R53	
VCN-003	R25	
VCN-004	R30	
VCP-007	VR1, VR3	Semi-fixed
VCP-005	VR2	Semi-fixed

OTHERS

Part No.	Symbol & Description	
VEC-001		Insulator (mica)
VSH-001	S1	Switch

17.30 CARRIAGE SERVO ASSEMBLY (VWS-003) (CARG)





Parts List

OTHERS

Part No.	Symbol & Description
VEC-001	Insulator (mica)

SEMICONDUCTORS

Part No.	Symbol & Description
µPC4558C	Z5
µPC339C	Z3
TA7210P	Z6
TC4016BP	Z2, Z4
HD7406P (SN7406N)	Z1
2SA1015-Y or O	Q1

CAPACITORS

Part No.	Symbol & Description
CEA 100P 25	C14, C15
CEA 220P 25	C19, C21
CEA 220P 16NP	C6
CEA 4R7P 25	C26, C28, C30, C32
CEA 010M 50NP	C11
CKDYF 473Z 50	C1–C5, C8, C9, C17, C18, C20, C25, C27, C29, C31
CKDYF 333Z 50	C7
CQMA 223J 50	C23
CQMA 103J 50	C22, C24
CQMA 103K 50	C10
CKDYB 682K 50	C16
CCDSL 471J 50	C12
CCDSL 151J 50	C13

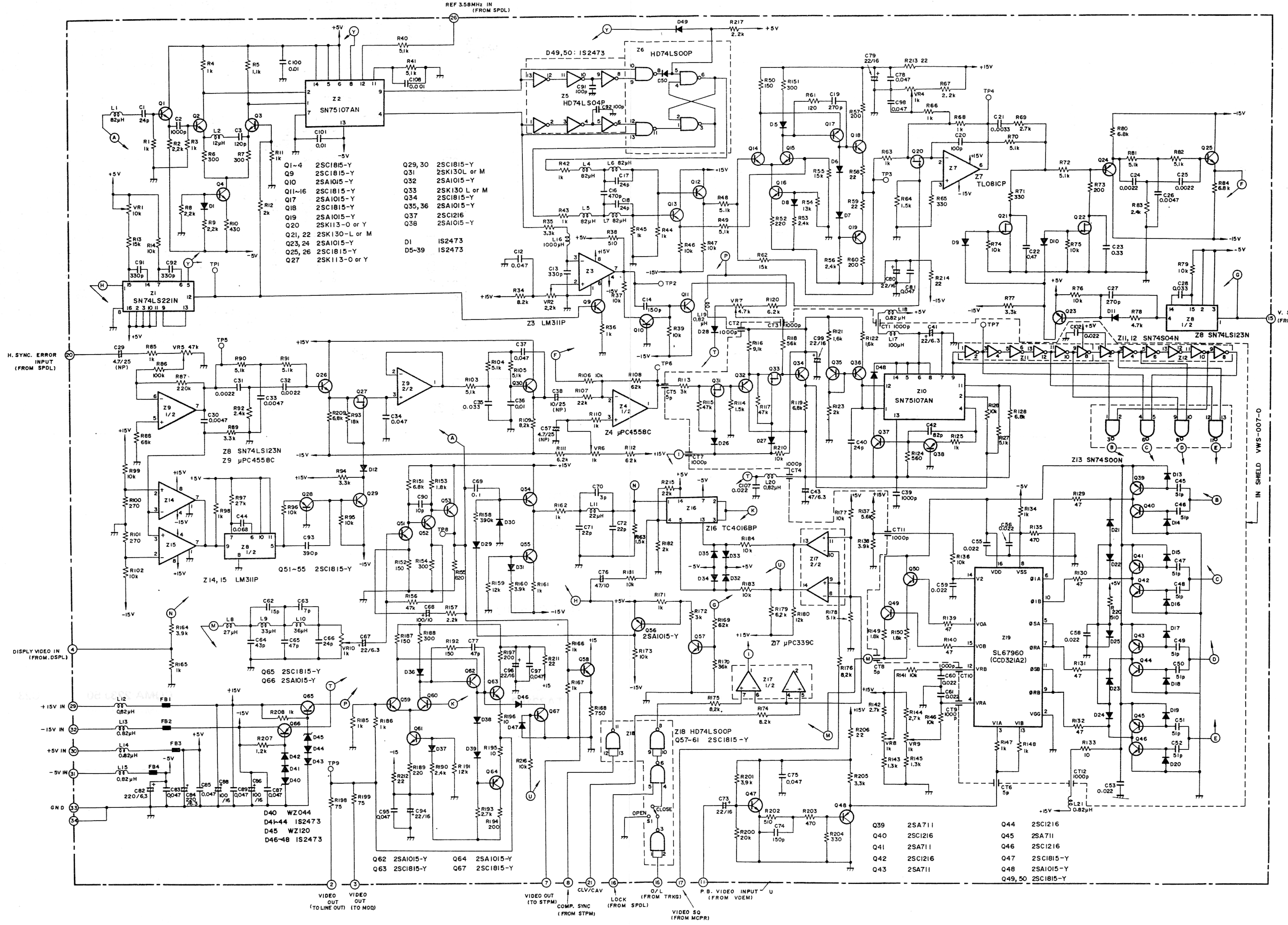
RESISTORS

Note: *When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.*

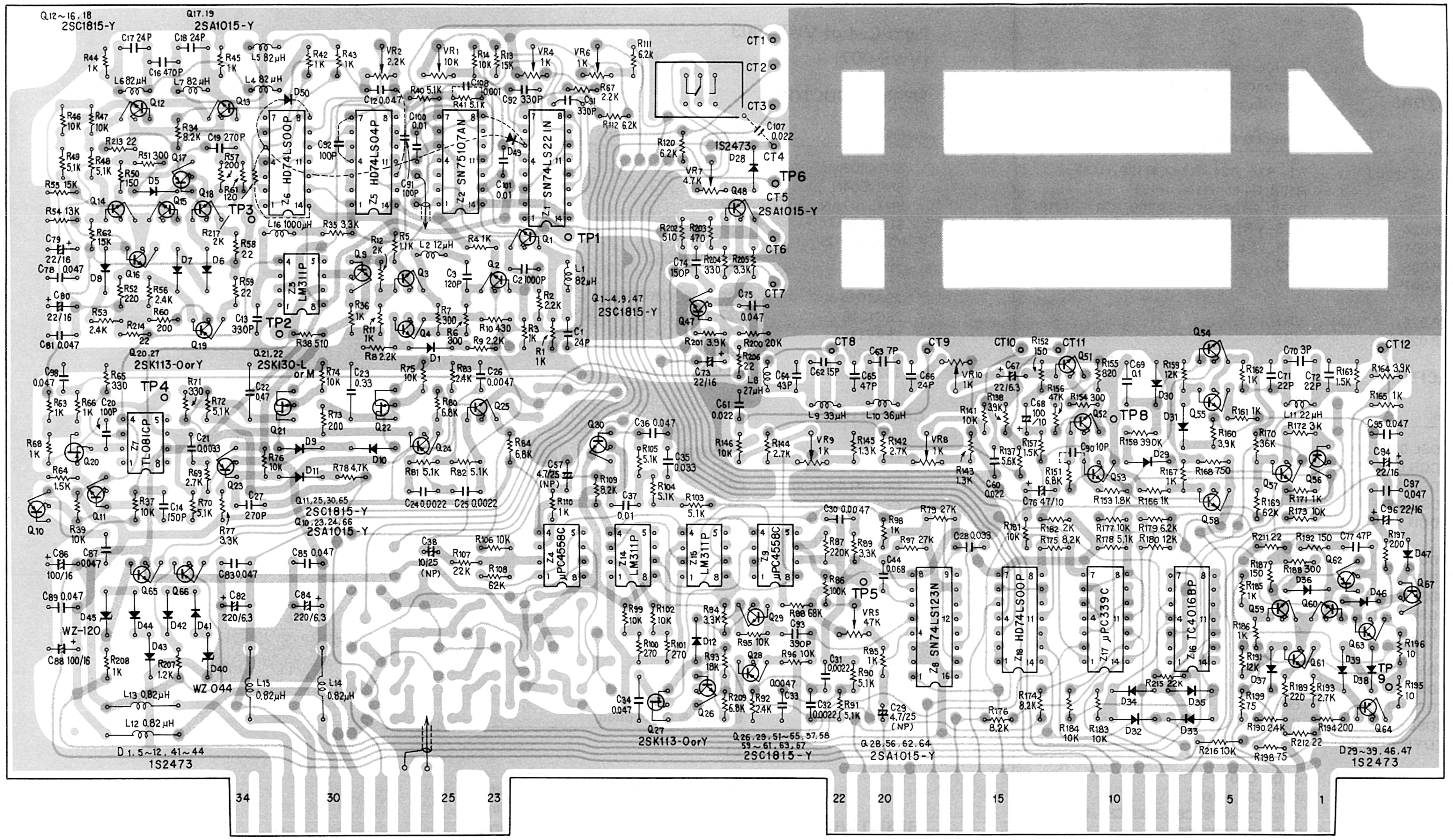
Part No.	Symbol & Description
RD¼VS □□□J	R1–R37, R39–R50
VCN-008	R38

17.31 VIDEO & TIME BASE CORRECTOR-A ASSEMBLY (VTBC)

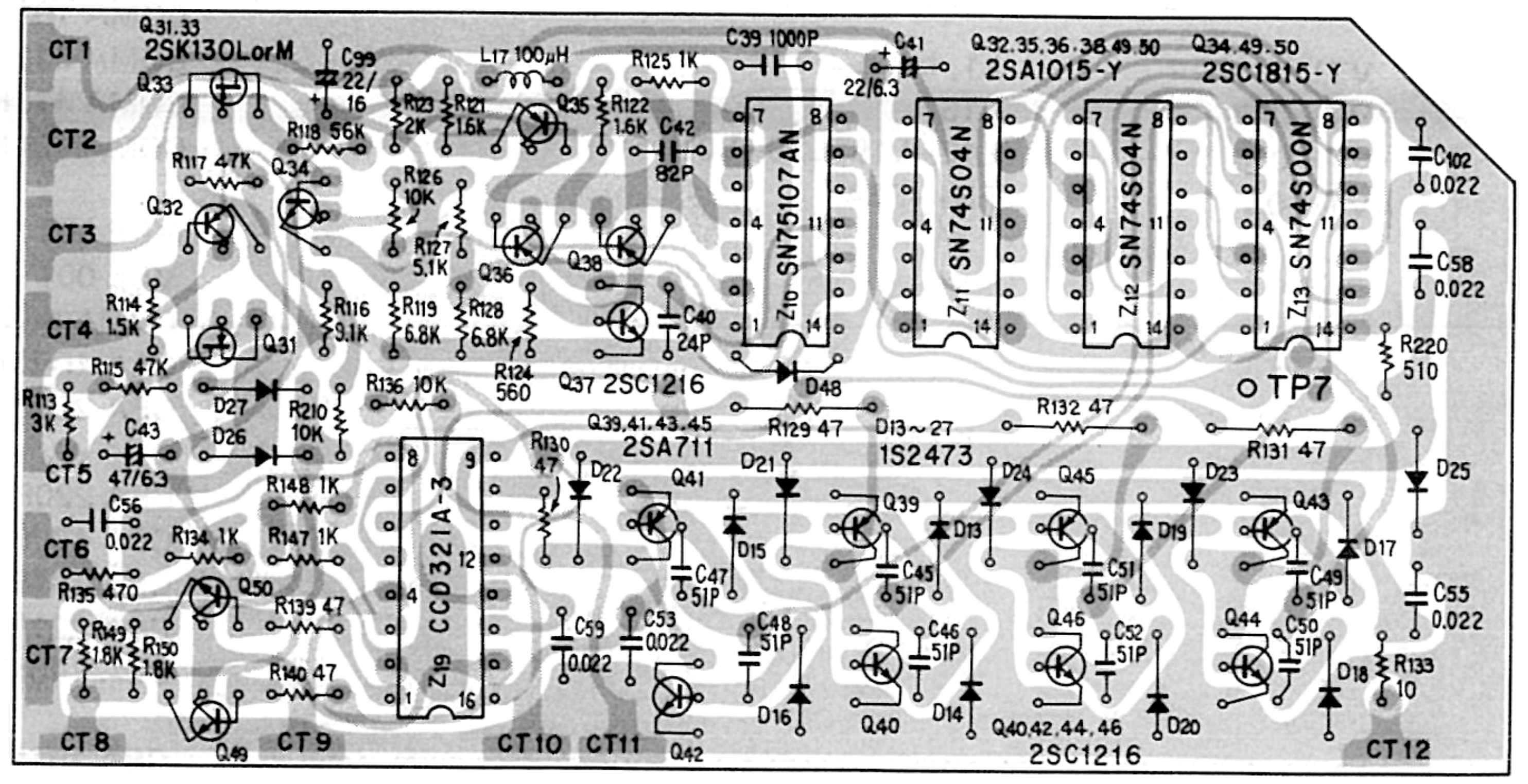
NOTE: VWW-003 consists of VWS-005, VWS-007.



VWS-005



VWS-007



Parts List of VWW-003 (VWS-005)

OTHER

Part No.	Symbol & Description
VSH-001	S1

SEMICONDUCTORS

Part No.	Symbol & Description
SN74LS221N	Z1
SN74LS123N	Z8
SN75107AN	Z2
LM311P (μPC271C)	Z3, Z14, Z15
HD74LS00P	Z6, Z18
HD74LS04P	Z5
TL081CP	Z7
μPC4558C	Z4, Z9
μPC339C	Z17
TC4016BP	Z16
2SA1015-Y	Q10, Q17, Q19, Q23, Q24, Q28, Q56, Q62, Q64, Q66, Q48
2SC1815-Y	Q1–Q4, Q9, Q11–Q16, Q18, Q25, Q26, Q29, Q30, Q47, Q57–Q59, Q51–Q55, Q60, Q61, Q63, Q65, Q67
2SK130-M	Q21, Q22
2SK113-Y or O	Q20, Q27
1S2473	D1, D5–D12, D28–D39, D41–D44, D46, D47
WZ-120	D45
WZ-044	D40

COILS AND TRANSFORMERS

Part No.	Symbol & Description
VTL-024	L2
VTL-052	L11
VTL-053	L8
VTL-054	L9
VTL-055	L10
VTL-034	L1, L4–L7
VTL-047	L16
VTF-010	L12–L15, L18–L21
VTH-001	FB1–FB4

RESISTORS

Note: *When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.*

Part No.	Symbol & Description
RD¼VS □□□J	R1–R14, R34–R112, R120, R137, R138, R141–R146, R151–R157, R159–R193, R195–R209, R211–R216
VCP-024	VR8–VR10
VCP-004	VR4, VR6
VCP-005	VR2
VCP-007	VR1
VCP-026	VR7
VCP-029	VR5

CAPACITORS

Part No.	Symbol & Description
CCDSL 030C 50	C70
CCDCH 070D 50	C63
CCDCH 150J 50	C62
CCDSL 220J 50	C71, C72
CCDCH 240J 50	C1, C17, C18, C66
CCDSL 100D 50	C90
CCDCH 430J 50	C64
CCDSL 470J 50	C65, C77
CCDSL 101J 50	C20, C91, C92
CCDSL 121J 50	C3
CCDSL 151J 50	C14, C74
CCDSL 271J 50	C19, C27
CCDSL 391J 50	C93
CCDSL 471J 50	C16
CKDYB 102K 50	C2, C108
CKDYF 103Z 50	C100, C101
CKDYF 223Z 50	C60, C61, C107
CKDYF 473Z 50	C12, C75, C78, C81, C83, C85, C87, C89, C95, C97, C98
CQMA 332K 50	C21
CQMA 222K 50	C24, C25, C31, C32
CQMA 472K 50	C26, C30, C33
CQMA 103K 50	C36
CQMA 333K 50	C28, C35
CQMA 473K 50	C34, C37
CQMA 104K 50	C69
VCE-002	C23
VCE-001	C22
CQMA 683K 50	C44
CEA 4R7M 25NP	C29, C57
CEA 220P 16	C73, C79, C80, C94, C96
CEA 220P 10	C67
CEA 470P 10	C76
CEA 101P 16	C86, C88
CEA 221P 6R 3	C82, C84
CEA 100M 25NP	C38
CEA 101P 10	C68
CQSH 331J 50	C13, C91, C92

Parts List of VWW-003 (VWS-007)

SEMICONDUCTORS

Part No.	Symbol & Description
SN74S00N	Z13
SN74S04N	Z11, Z12
SN75107AN	Z10
SL67960 (CCD321A2)	Z19
2SC1815-Y	Q34, Q49, Q50
2SA1015-Y	Q32, Q35, Q36, Q38
2SC1216	Q37, Q40, Q42, Q44, Q46
2SA711	Q39, Q41, Q43, Q45
2SK130M	Q31, Q33
1S2473	D13–D27, D48

CAPACITORS

Part No.	Symbol & Description
CCDCH 240J 50	C40
CCDCH 510J 50	C45–C52
CCDSL 820J 50	C42
CKDYB 102K 50	C39
CKDYF 223Z 50	C53, C55, C56, C58, C59, C102

COILS AND TRANSFORMERS

Part No.	Symbol & Description
VTL-035	L17

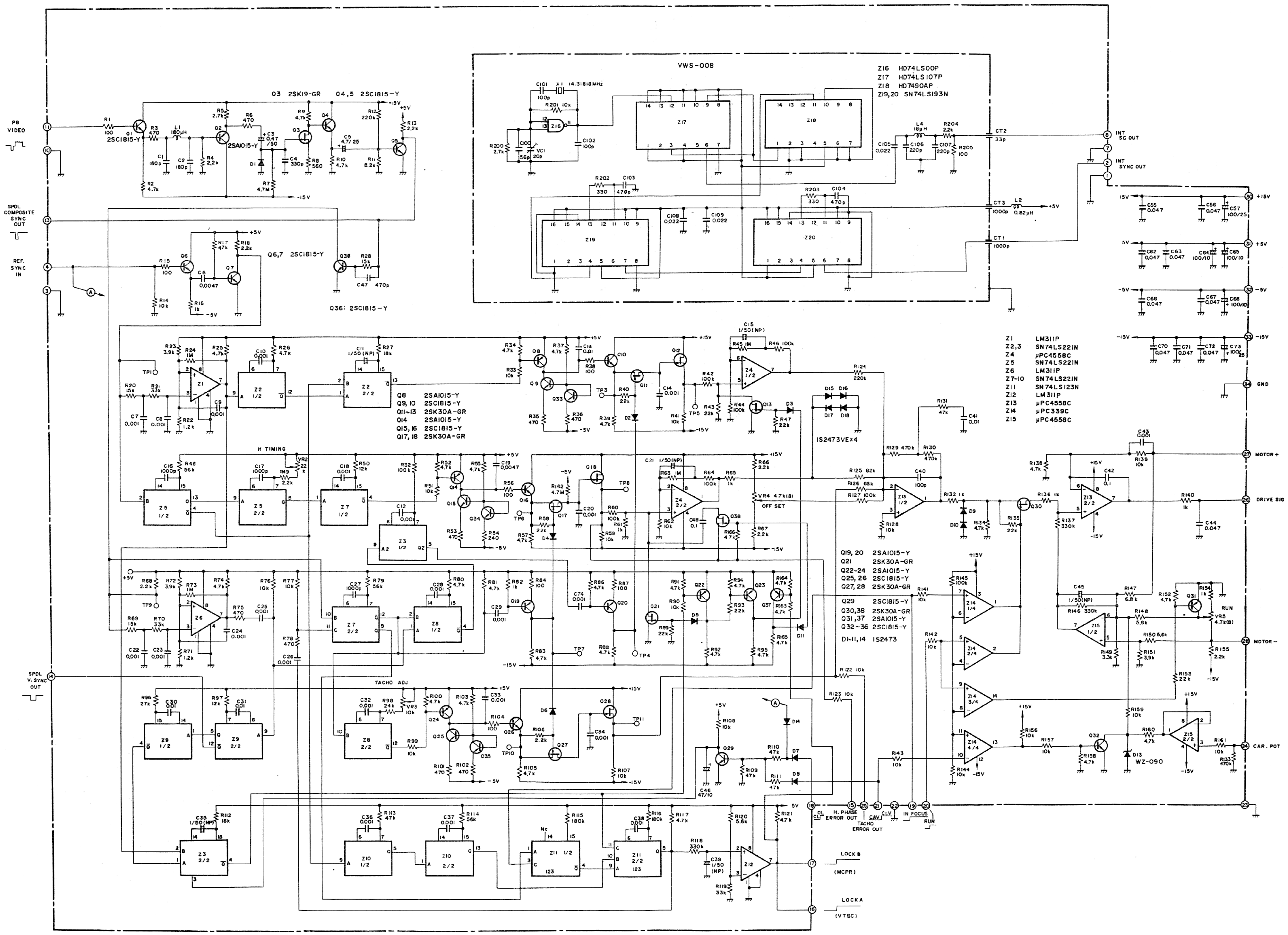
RESISTORS

Note: *When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.*

Part No.	Symbol & Description
RD¼VS □□□J	R113–R119, R121–R136, R139, R140, R147–R150, R210, R220

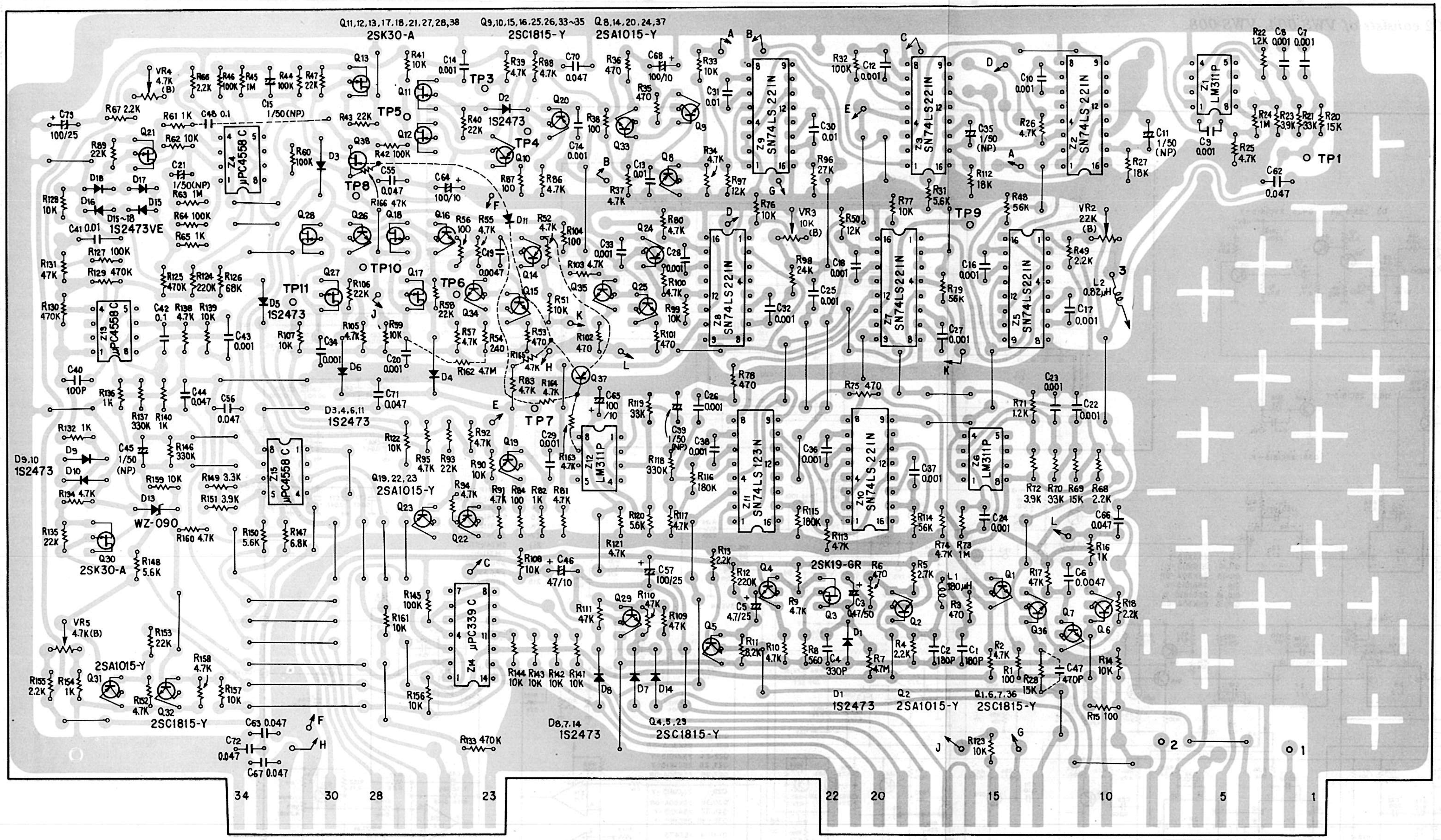
17.32 SPINDLE SERVO ASSEMBLY (SPDL)

NOTE: VWW-002 consists of VWS-004, VWS-008.

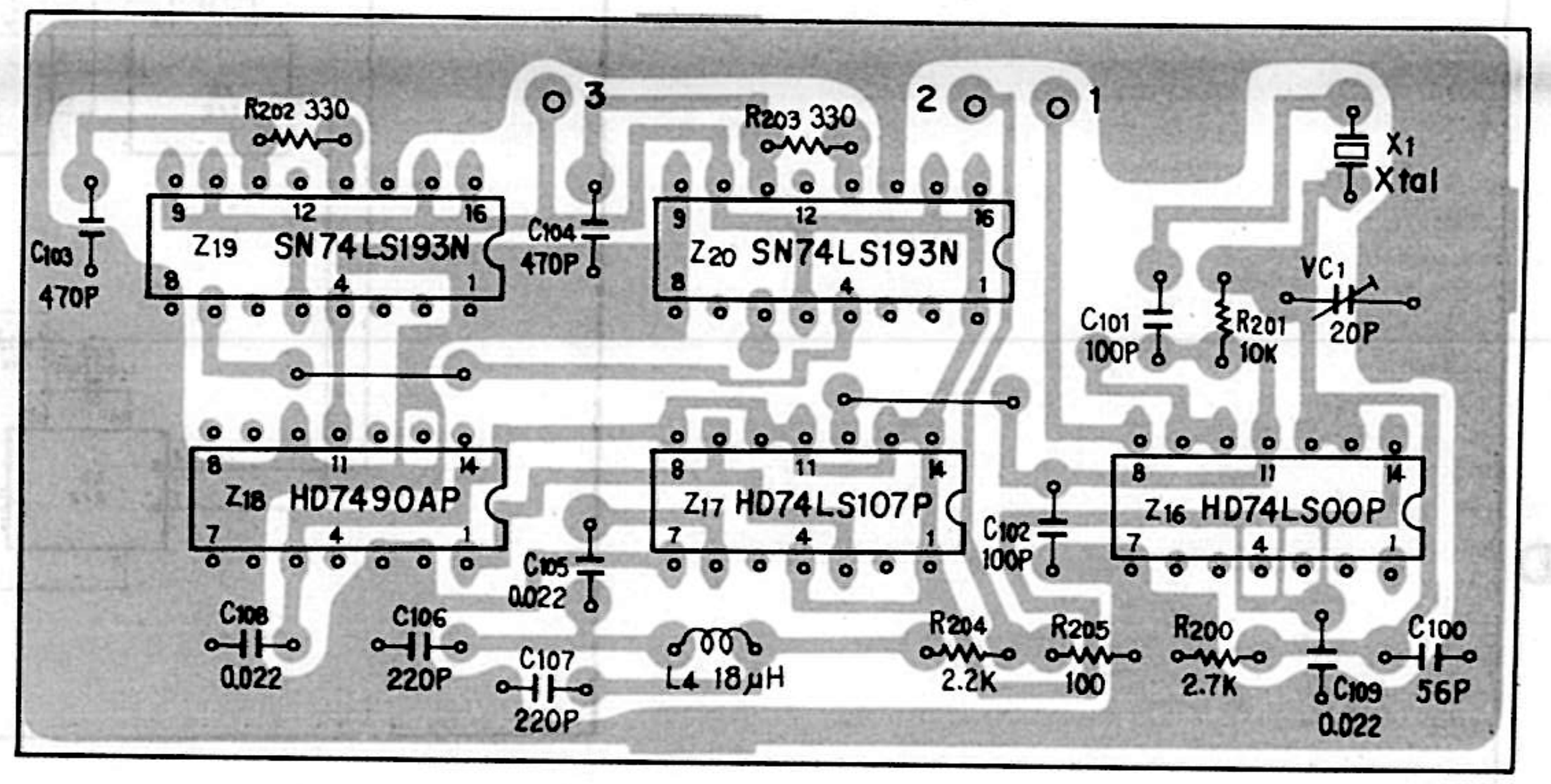


NOTE:
There are two kinds of P.C. Boards (VWS-004) used, which differ according to the location of the parts such as transistors, etc. When repairing the P.C. Board (VWS-004), contrast it with the P.C. Board (VWS-004) on page 194 and use the right one.

VWS-004



VWS-008



Parts List of VWW-002 (VWS-004)

SEMICONDUCTORS

Part No.	Symbol & Description
LM311P (μPC271C)	Z1, Z6, Z12
SN74LS221N	Z2, Z5, Z7, Z8–Z10, Z3
SN74LS123N	Z11
μPC4558C	Z4, Z13, Z15
μPC339C	Z14
2SC1815-Y	Q1, Q4–Q7, Q9, Q10, Q15, Q16, Q25, Q26, Q29, Q32–Q36
2SA1015-Y or O	Q2, Q8, Q14, Q19, Q20, Q22–Q24, Q31, Q37
2SK19-GR	Q3
2SK30A-GR	Q11–Q13, Q17, Q18, Q21, Q27, Q28, Q30, Q38
1S2473	D1–D10, D14, D11
1S2473VE	D15–D18
WZ-090	D13

CAPACITORS

Part No.	Symbol & Description
CQSH 102J 50	C16, C17, C27
CCDSL 471J 50	C47
CCDSL 331J 50	C4
CCDSL 181J 50	C1, C2
CCDSL 101J 50	C40
CKDYF 473Z 50	C44, C55, C56, C62, C63, C66, C67, C72, C70, C71
CKDYB 102K 50	C9, C24
VCE-004	C42
CQMA 103K 50	C13, C30, C31, C41
CQMA 472K 50	C6
CQMA 102K 50	C10, C12, C14, C18, C20, C25, C26, C28, C29, C34, C36, C37, C38, C43, C74
CQMA 472J 50	C19
CQMA 102J 50	C7, C8, C22, C23, C32, C33
CEA 101P 25	C57, C73
CEA 101P 10	C64, C65, C68
CEA 470 P10	C46
CEA 4R7P 25	C5
CEA R47P 50	C3
CEA 010M 50NP	C15, C21, C35, C39, C45, C11

Note: When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

RESISTORS

Part No.	Symbol & Description	
RD¼PS □□□J	R1–R26, R28:R29, R31–R47, R49–R78, R80–R84, R86–R162	
RN¼PR□□□□F	R48, R79, R27	
VCR-027	VR3	Semi-fixed
VCR-008	VR2	Semi-fixed
VCR-006	VR4	Semi-fixed
VCP-006	VR5	Semi-fixed

COILS AND TRANSFORMERS

Part No.	Symbol & Description	
VTL-038	L1	Coil
VTF-010	L2	Peaking coil

Parts List of VWW-002 (VWS-008)

SEMICONDUCTORS

Part No.	Symbol & Description
HD7490AP	Z18
SN74LS193N	Z19, Z20
HD74LS00P	Z16
HD74LS107P	Z17

OTHERS

Part No.	Symbol & Description	
VSS-001	X1	X'tal
VCM-002	VC1	Ceramic trimmer

CAPACITORS

Part No.	Symbol & Description
CCDCH 101J 50	C102
CCDCH 560J 50	C100
CCDUJ 101J 50	C101
CKDYF 223Z 50	C105, C108, C109
CCDSL 221J 50	C106, C107
CKDYB 471K 50	C103, C104

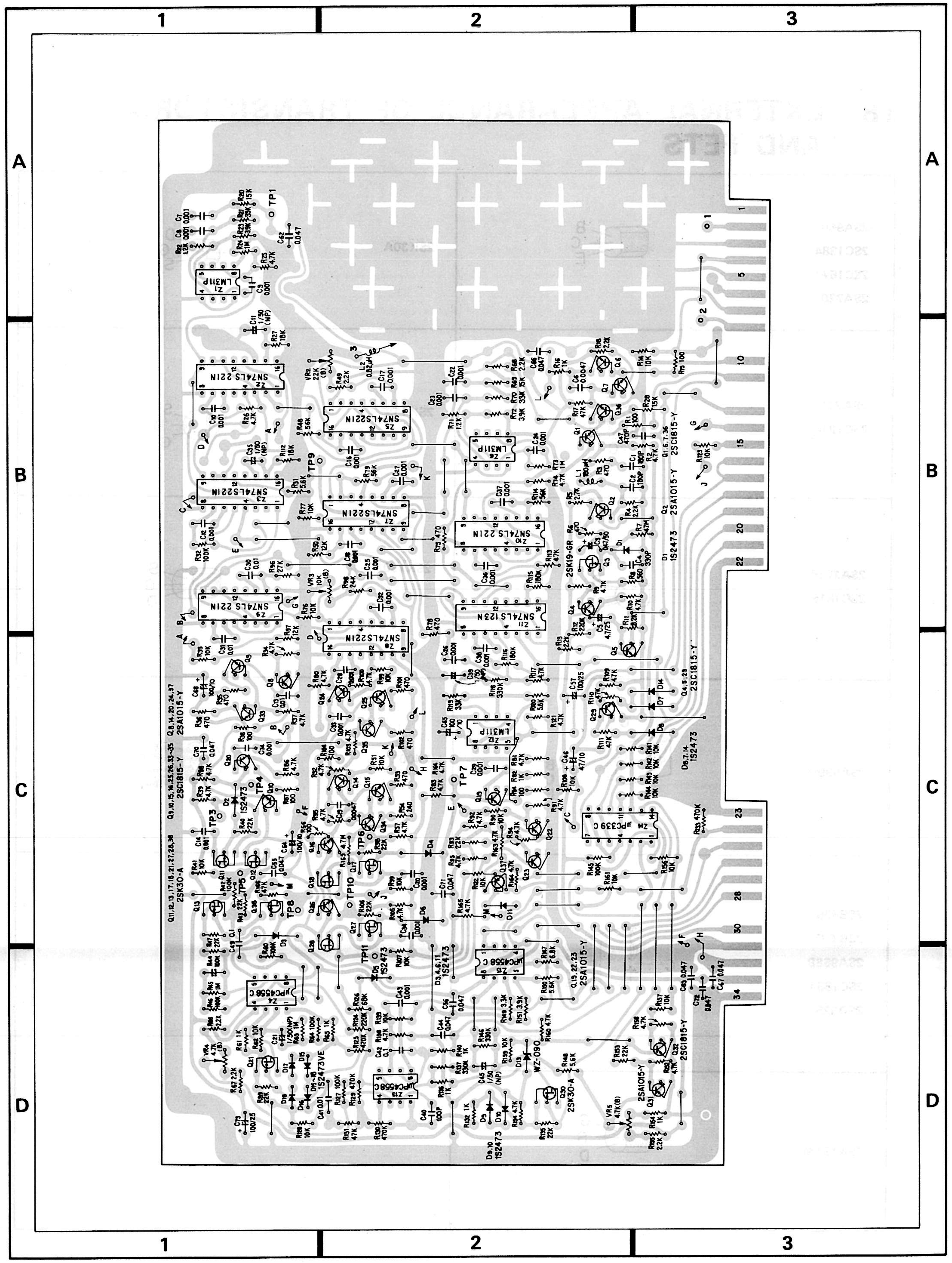
COILS AND TRANSFORMER

Part No.	Symbol & Description
VTL-026	Coil

Note: When ordering resistors, convert the resistance value into code form, and then rewrite the part no. as before.

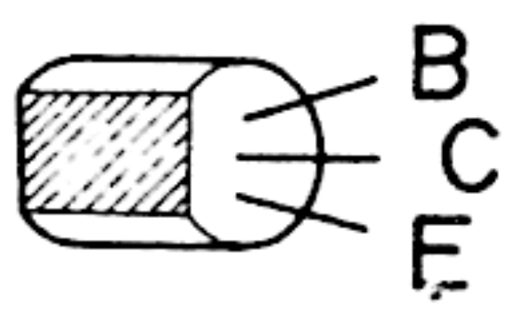
RESISTORS

Part No.	Symbol & Description
RD¼VS □□□J	R200–R205

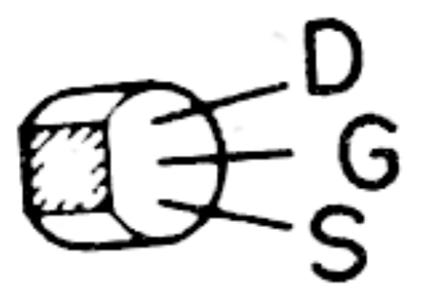


18. EXTERNAL APPEARANCE OF TRANSISTORS AND FETS

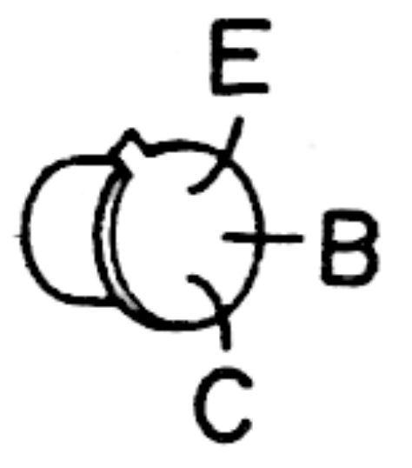
2SA950
2SC1384
2SC1674
2SA720



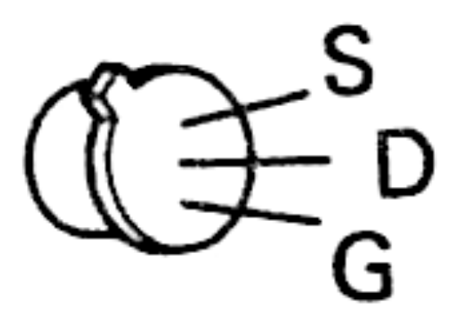
2SK30A



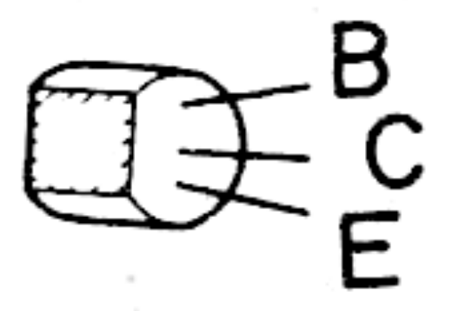
2SA711
2SC1216



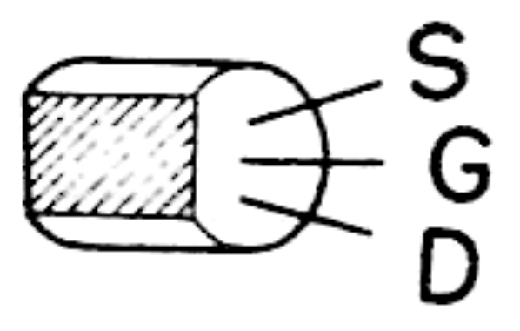
2SK113



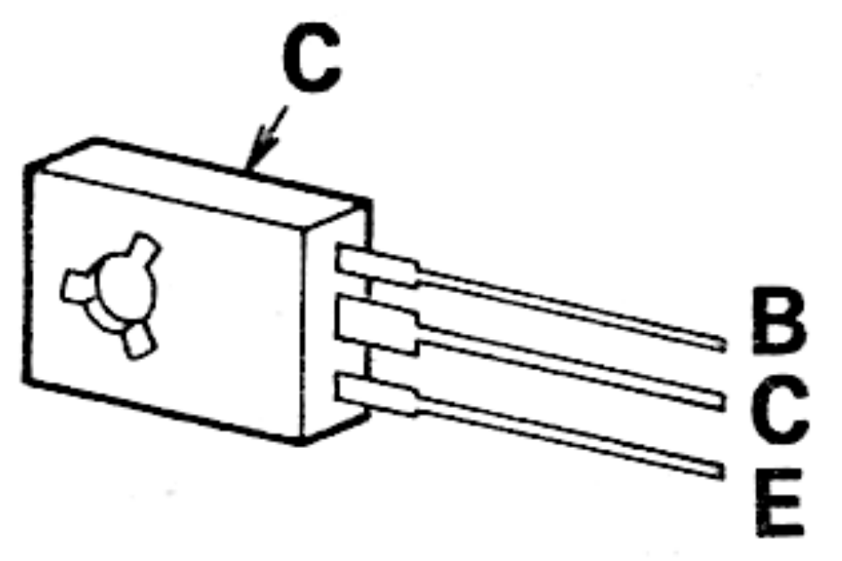
2SA1015
2SC1815



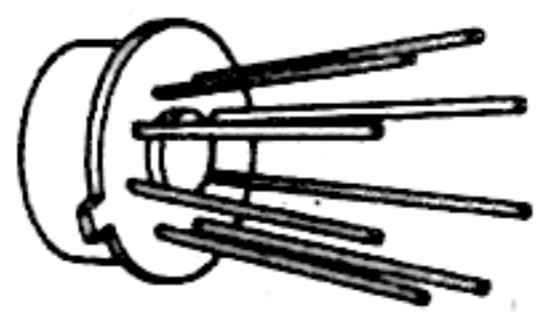
2SK130



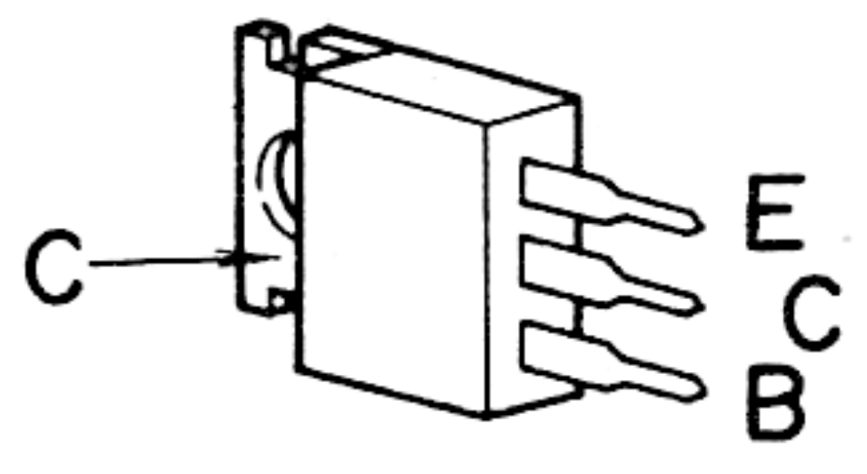
2SA939V



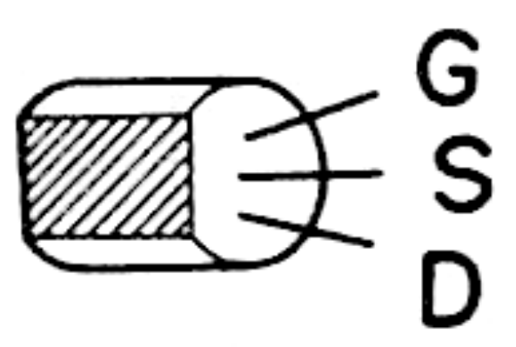
F4001



2SB595
2SB 675
2SA968B
2SC1881
2SD525



2SK19TM

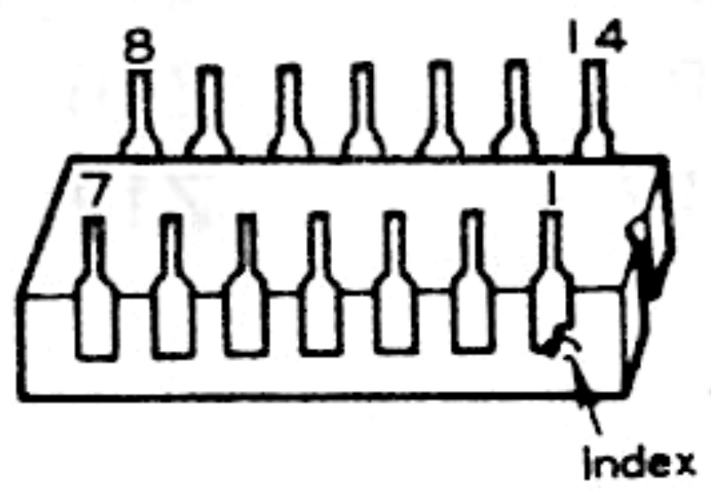


19. EXTERNAL APPEARANCE OF ICs

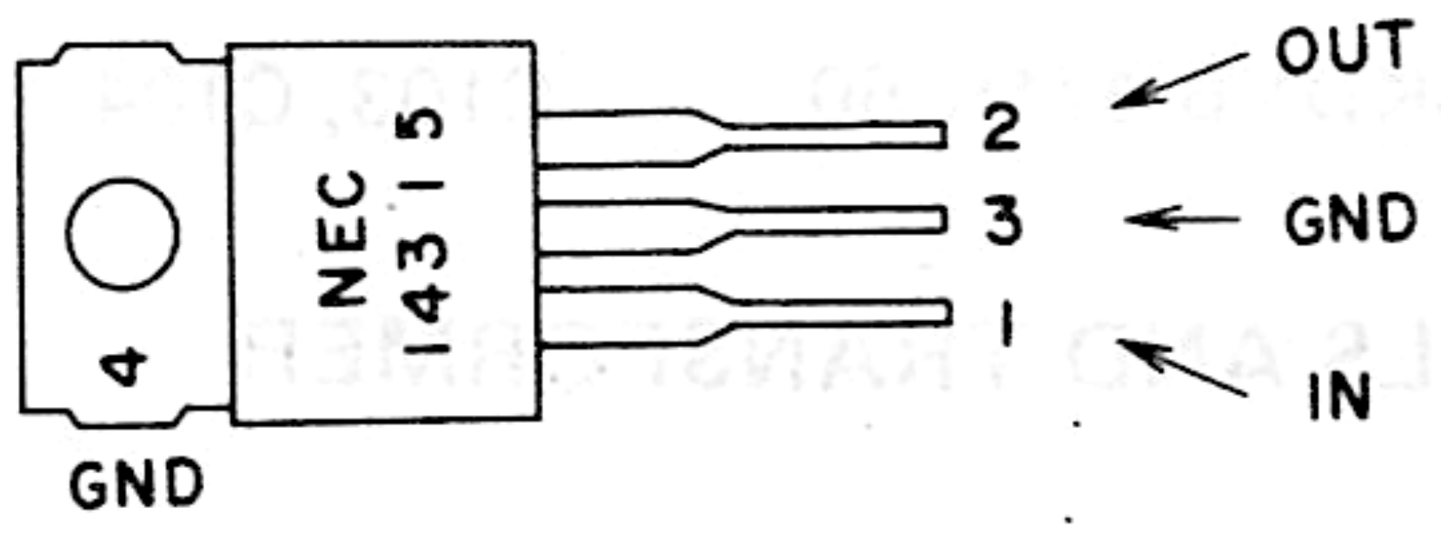
µPC339C
HD7490AP
HD7406P
HD7407P
HD7492AP
HD7493AP
HD75107AP
HD74121P
HD74LS00P
HD74LS02P
HD74LS03P
HD74LS04P
HD74LS08P
HD74LS10P
HD74LS20P
HD74LS20P
HD74LS30P
HD74LS107P

SN75107AN
SN74S00N
SN74S04N
SN74LS27N
SN74LS164N

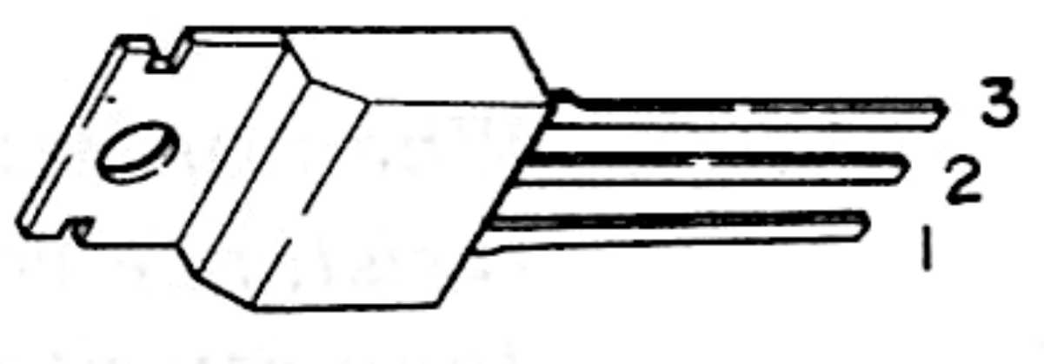
TC4001BP
TC4011BP
TC4016BP



µPC14315H

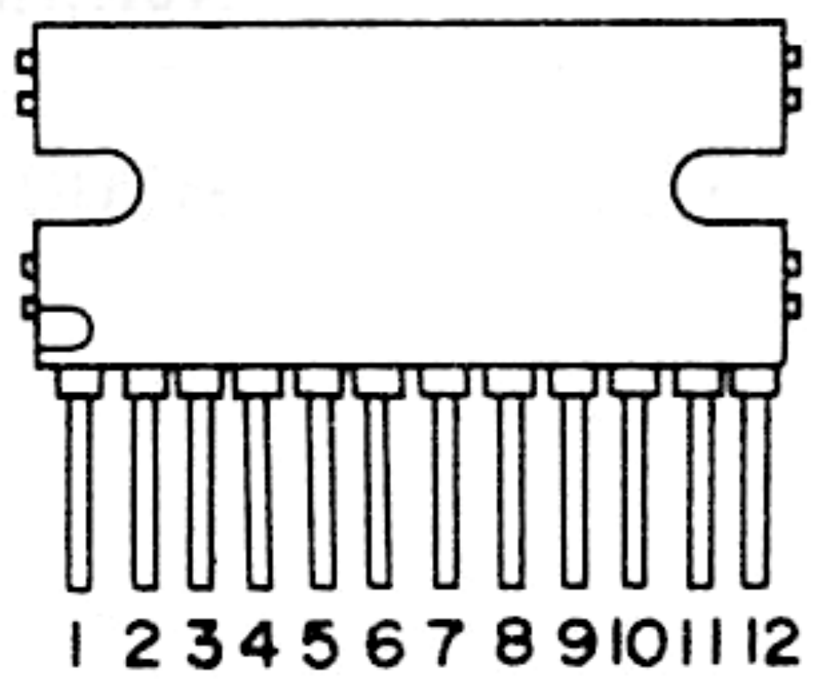


MC7915CT

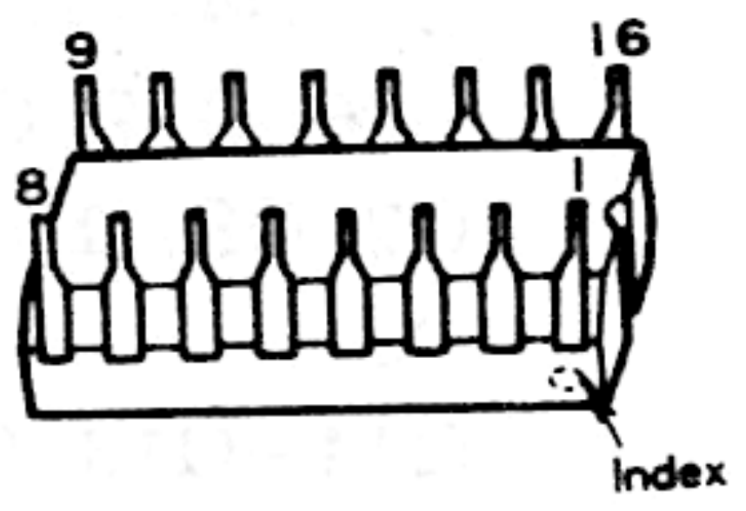


Pin 1. Ground
2. Input
3. Output

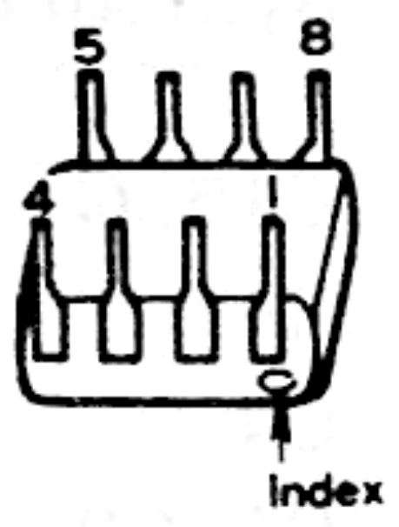
TA7210P



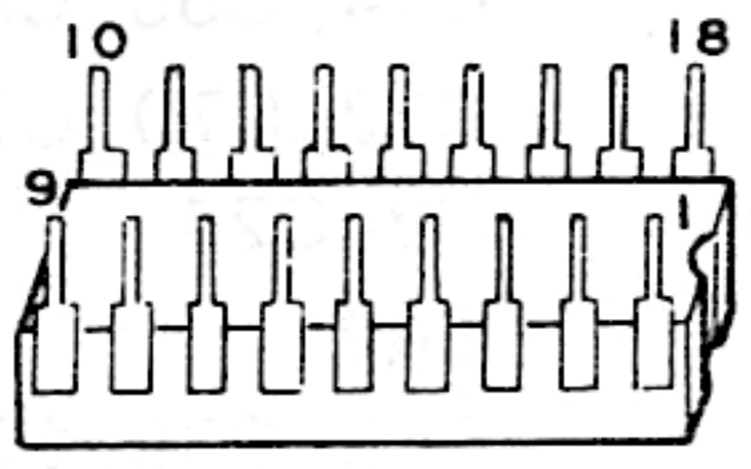
HA1137P
HD7445P
HD74123P
HD74LS139P
SN74LS193N
SN7489N
SN74LS76N
SN74LS123N
SN74LS157N
SN74LS221N
DM8678CABN
TC5508P
CCD321A-3
SAF1031P



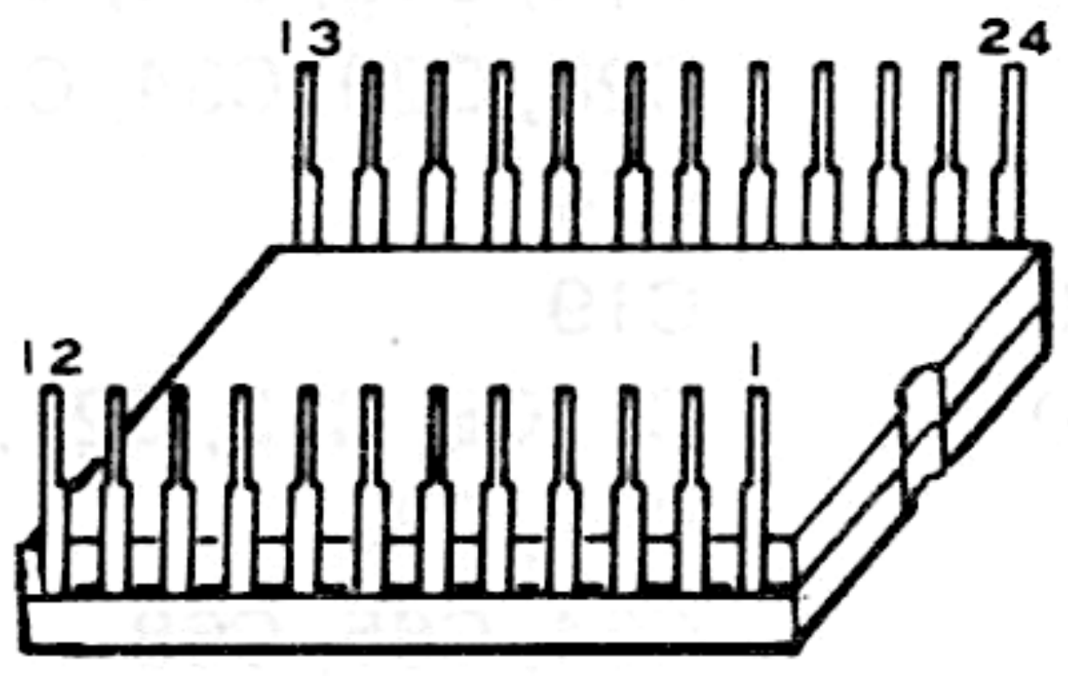
µPC4558C
LM311P
NE555P
TL081CP



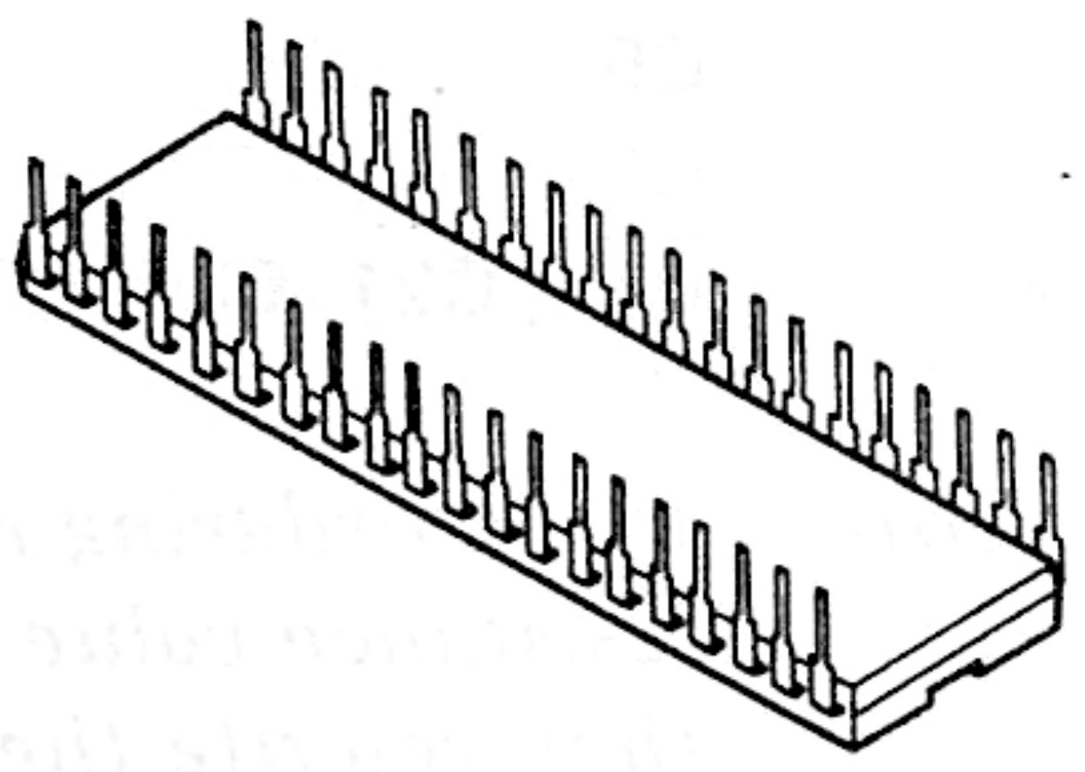
SAF1032P



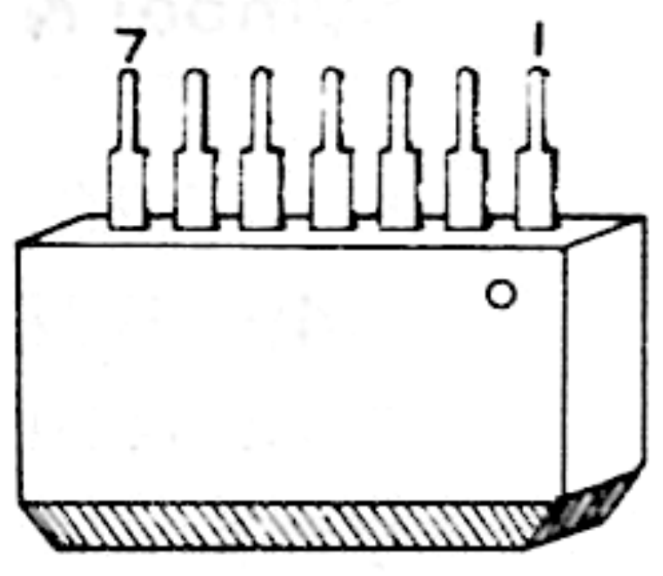
2716



MK3850N
MK3853N
MK90005N

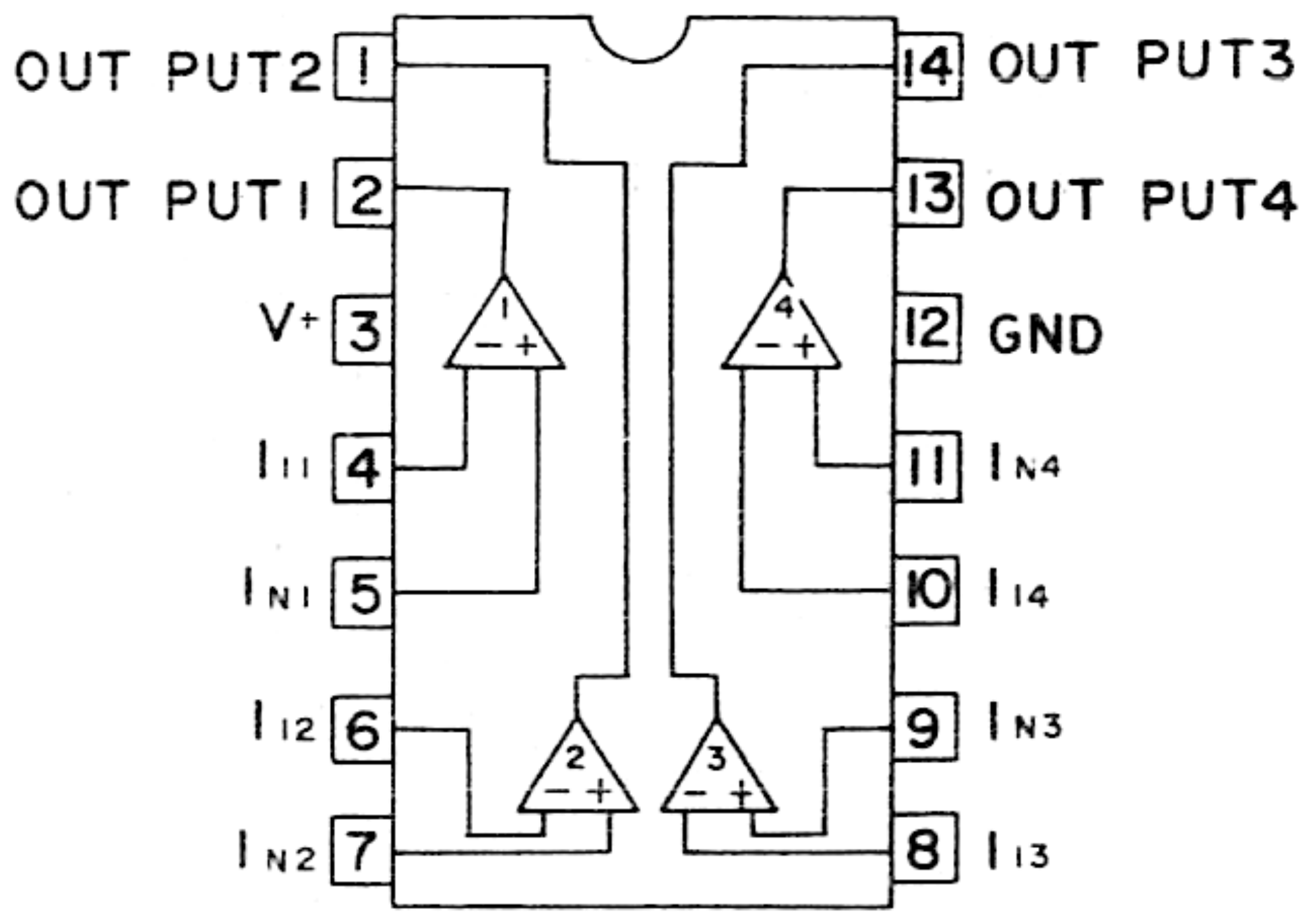


TA7302P

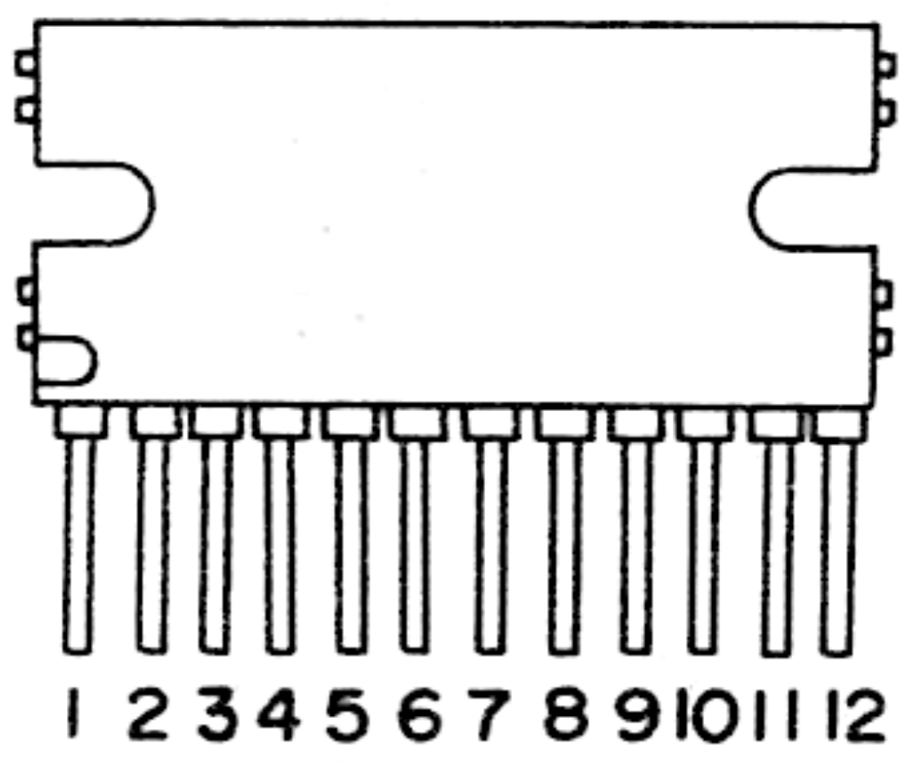


20. TERMINAL ASSIGNMENTS

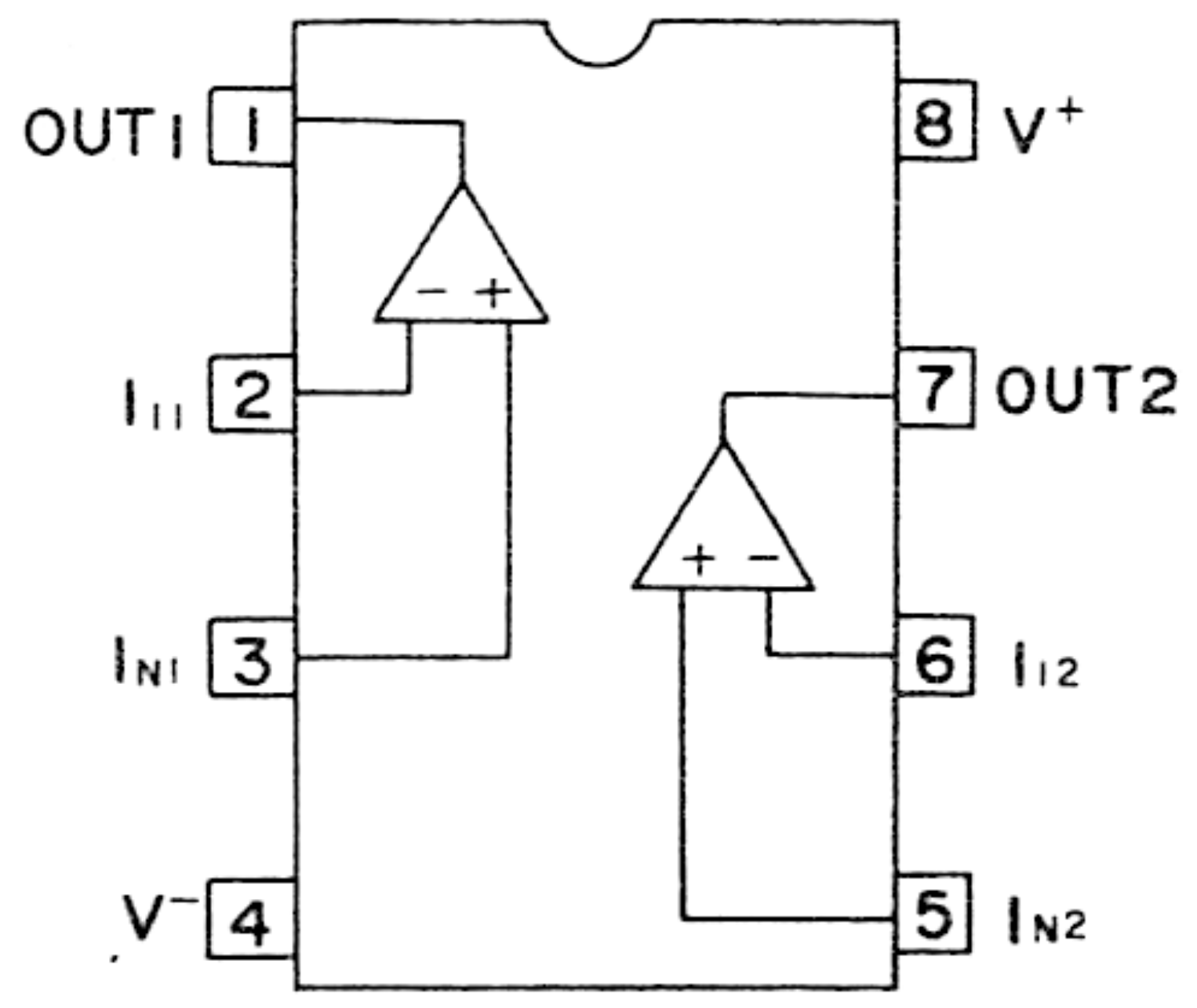
μPC339C



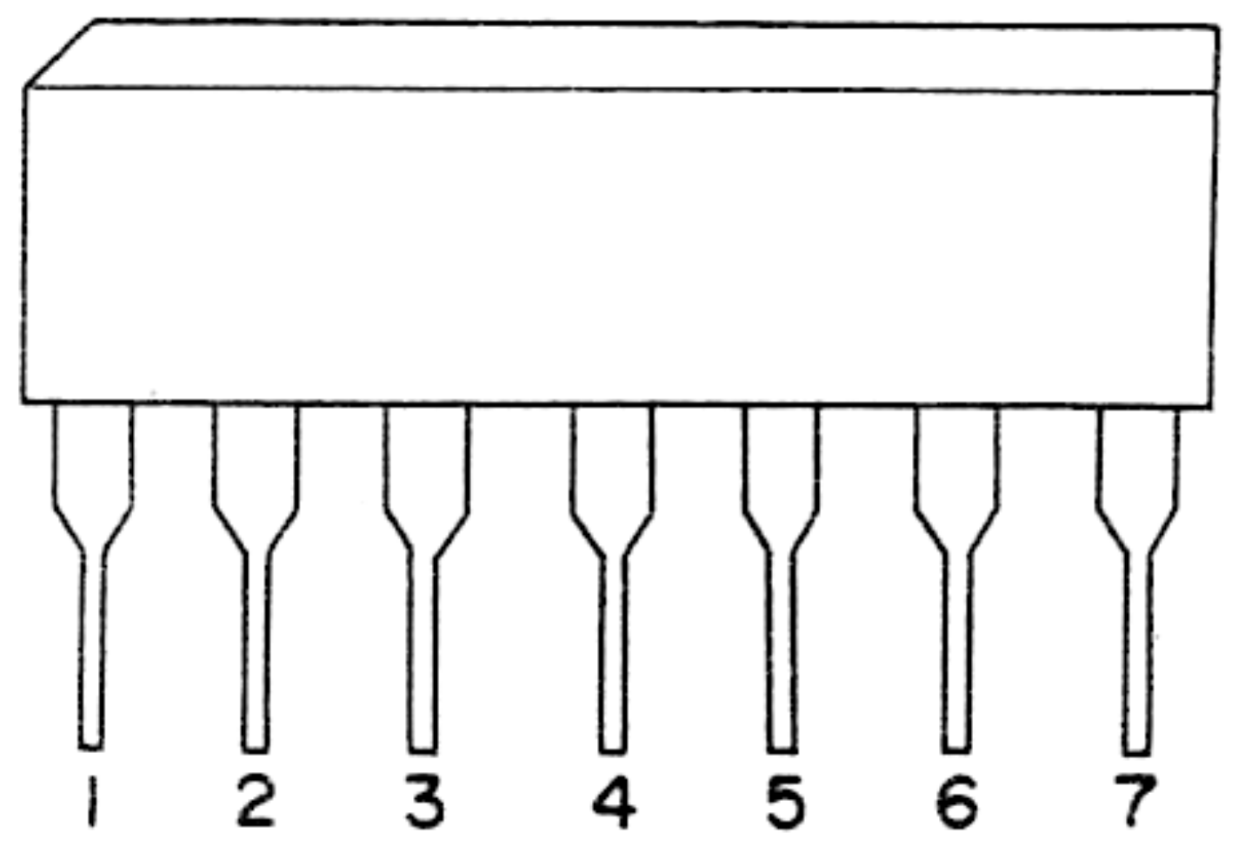
TA7210P



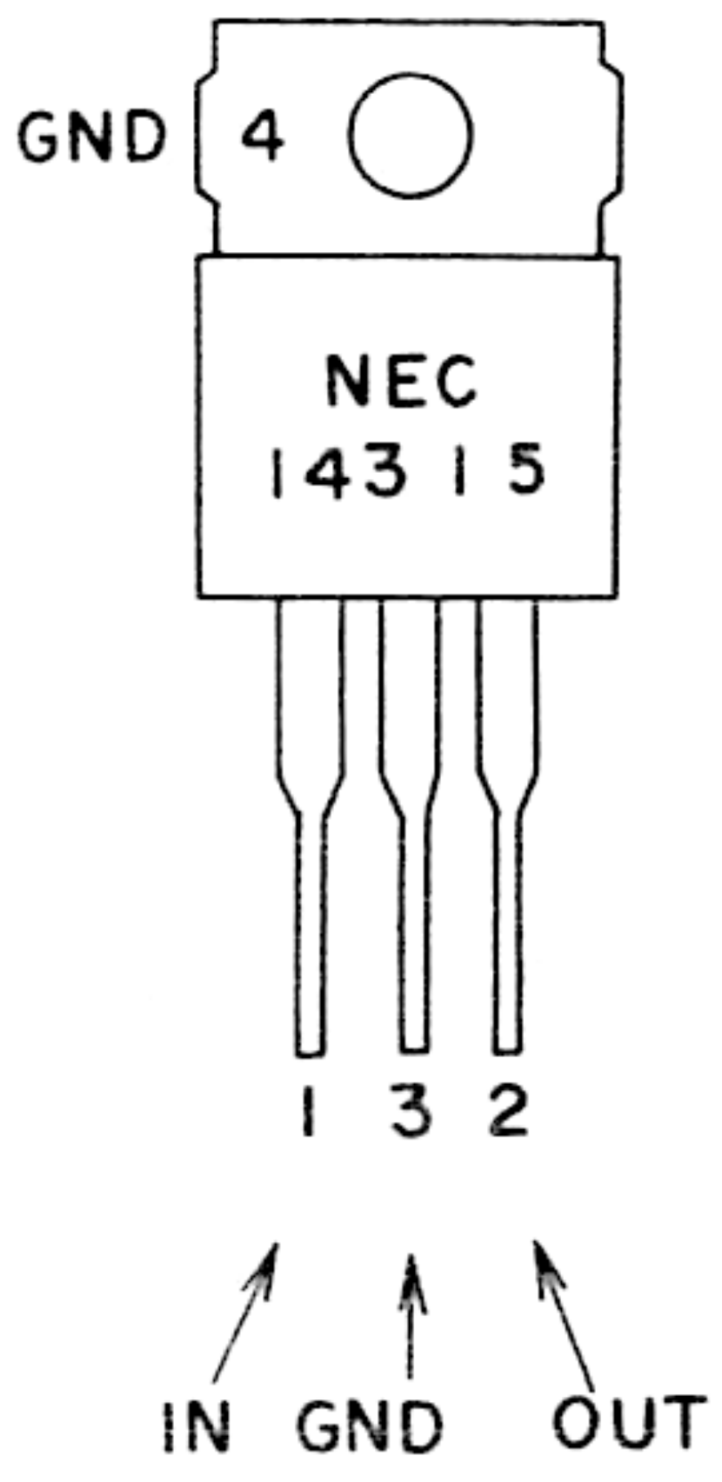
μPC4558C



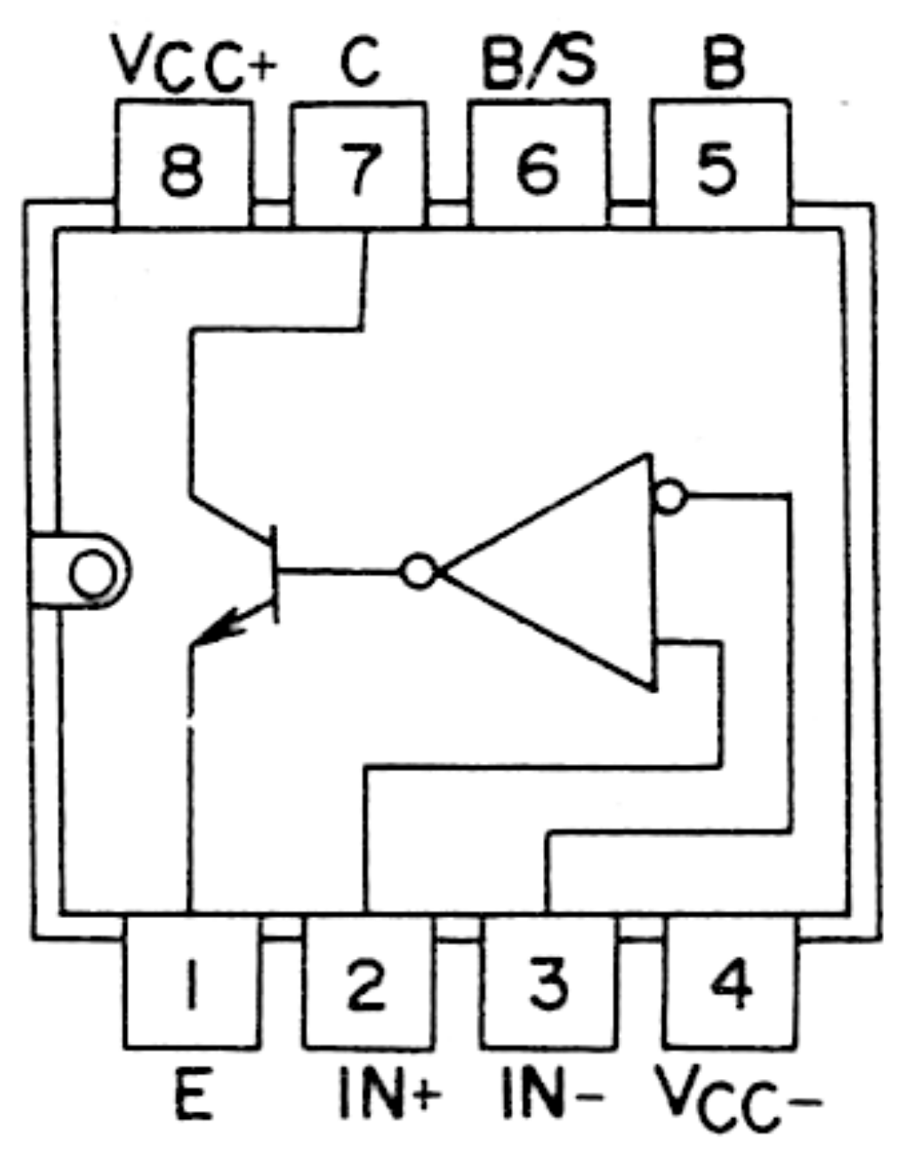
TA7302P



μPC14315H



LM311P



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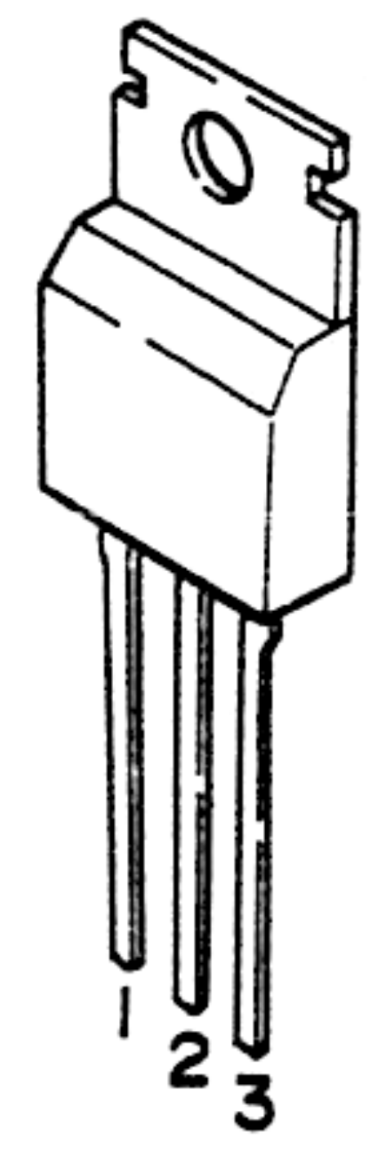
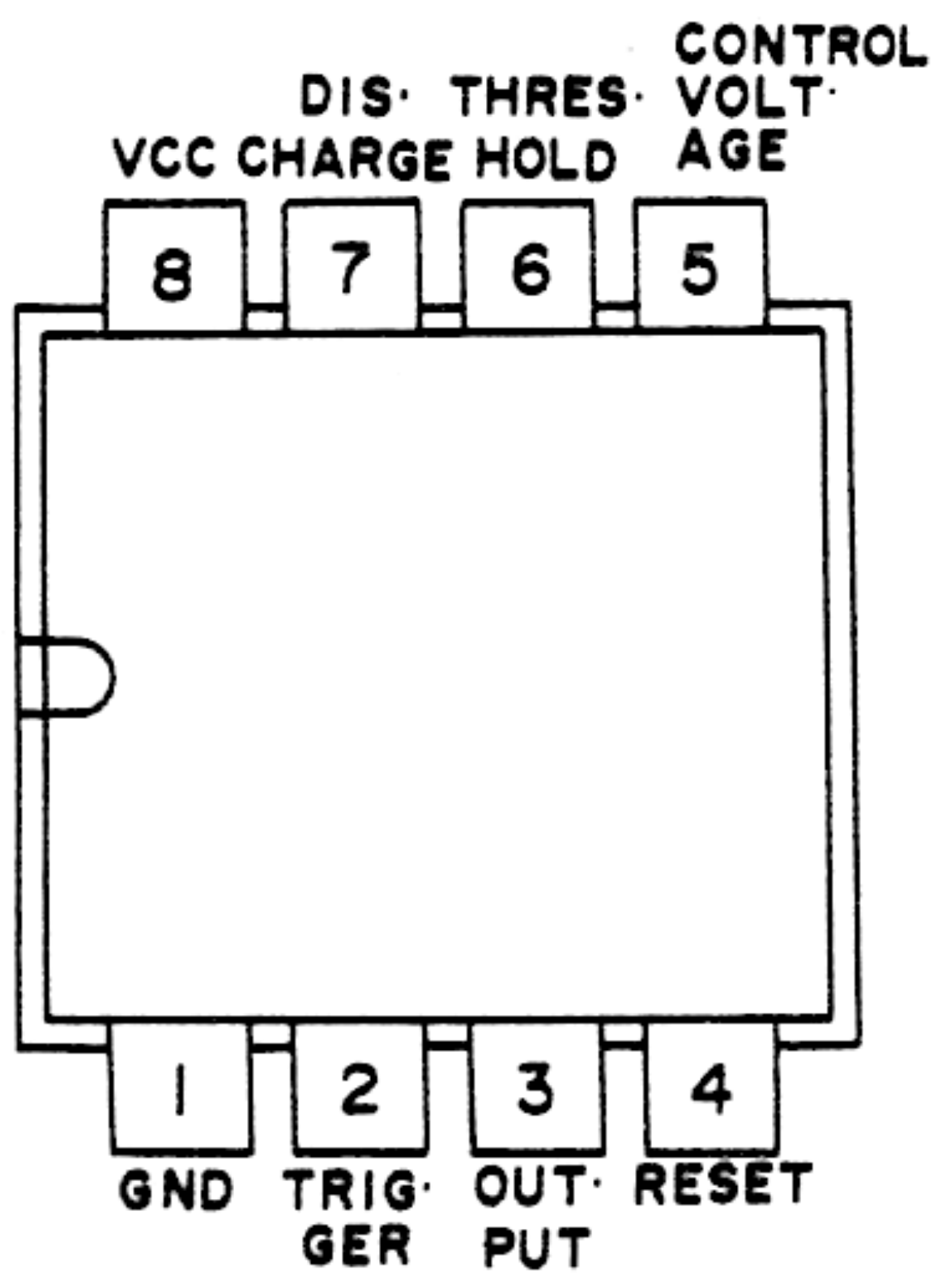


Pin 1. Ground
2. Input
3. Output

NE555P



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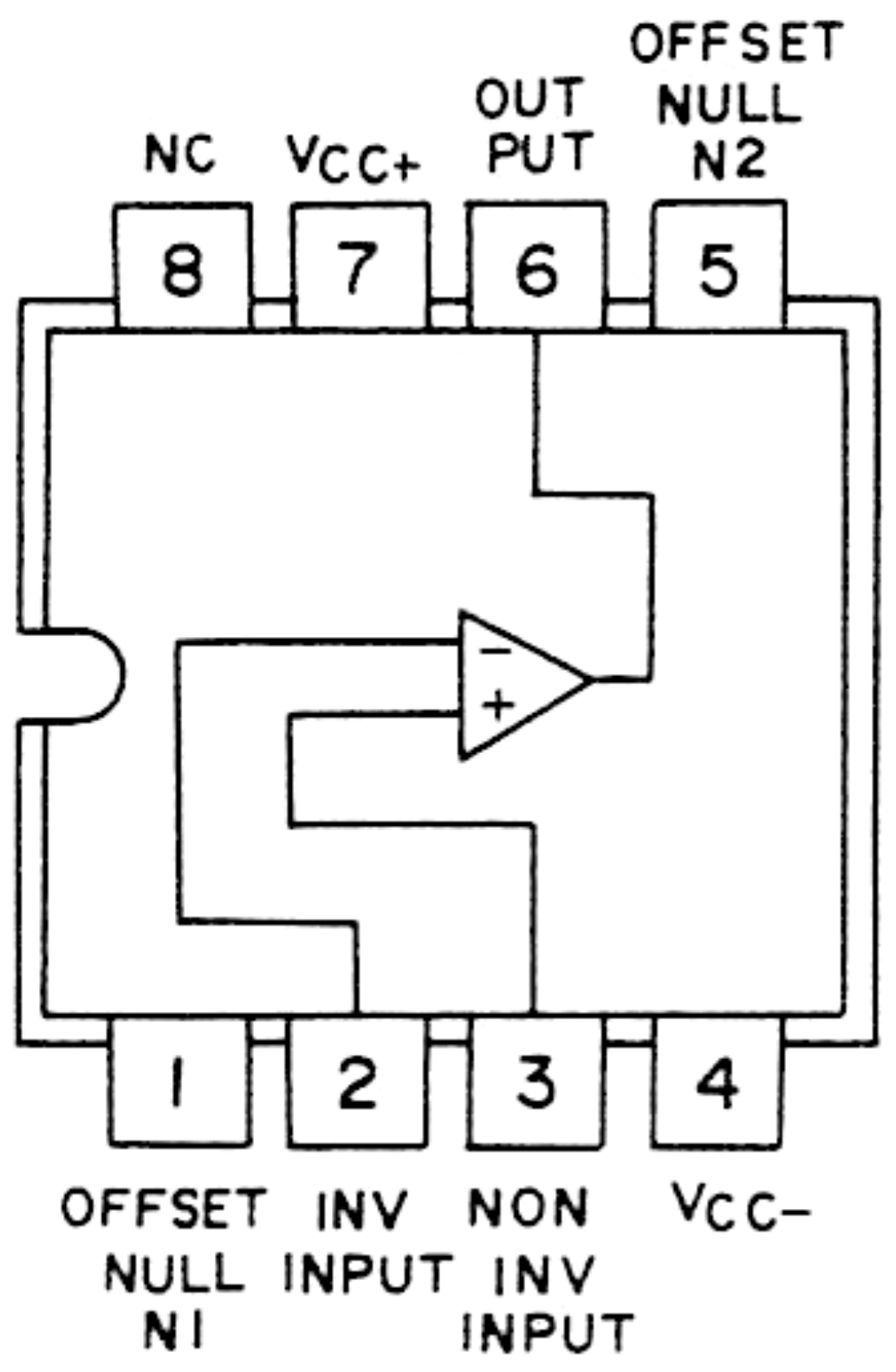

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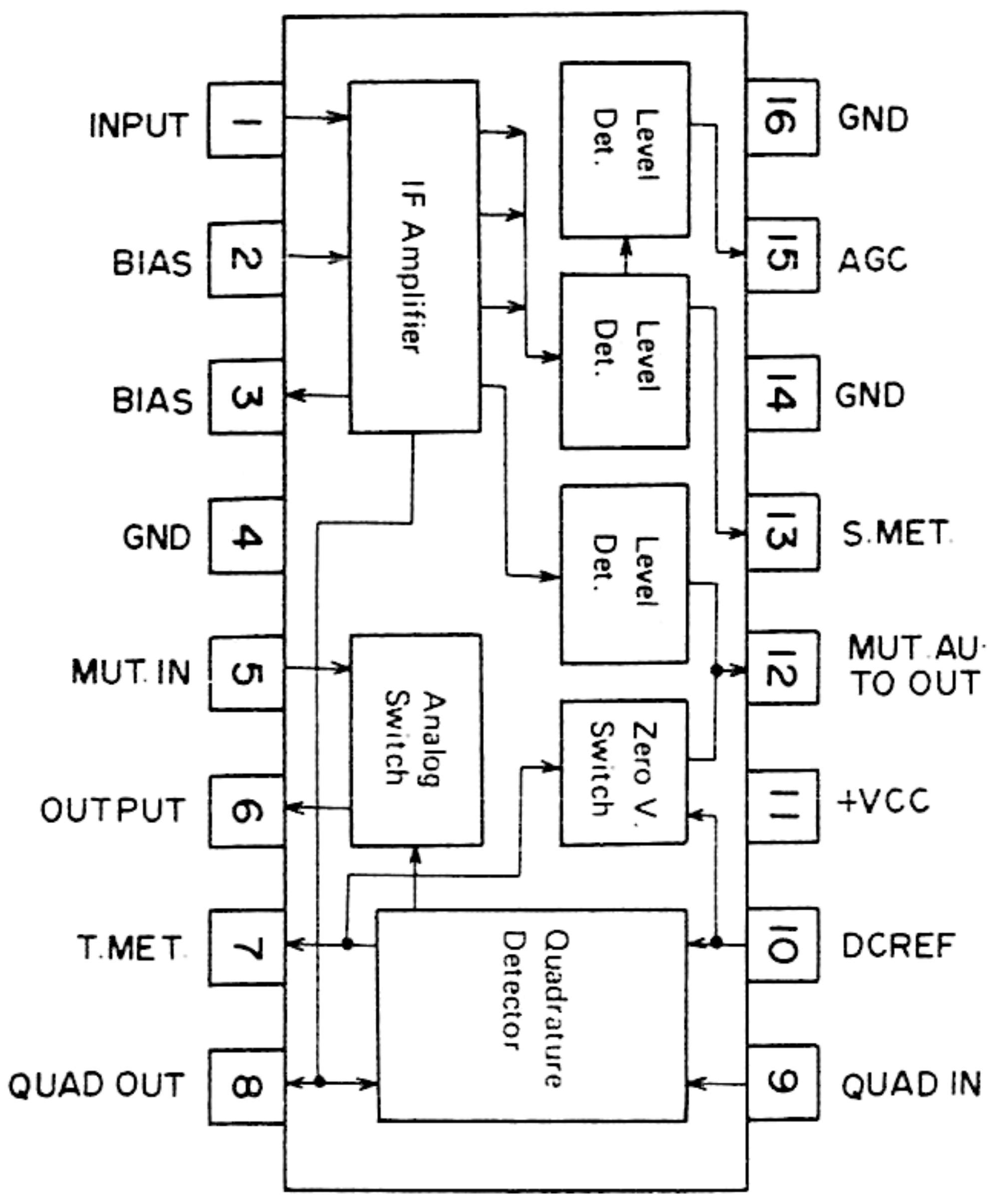

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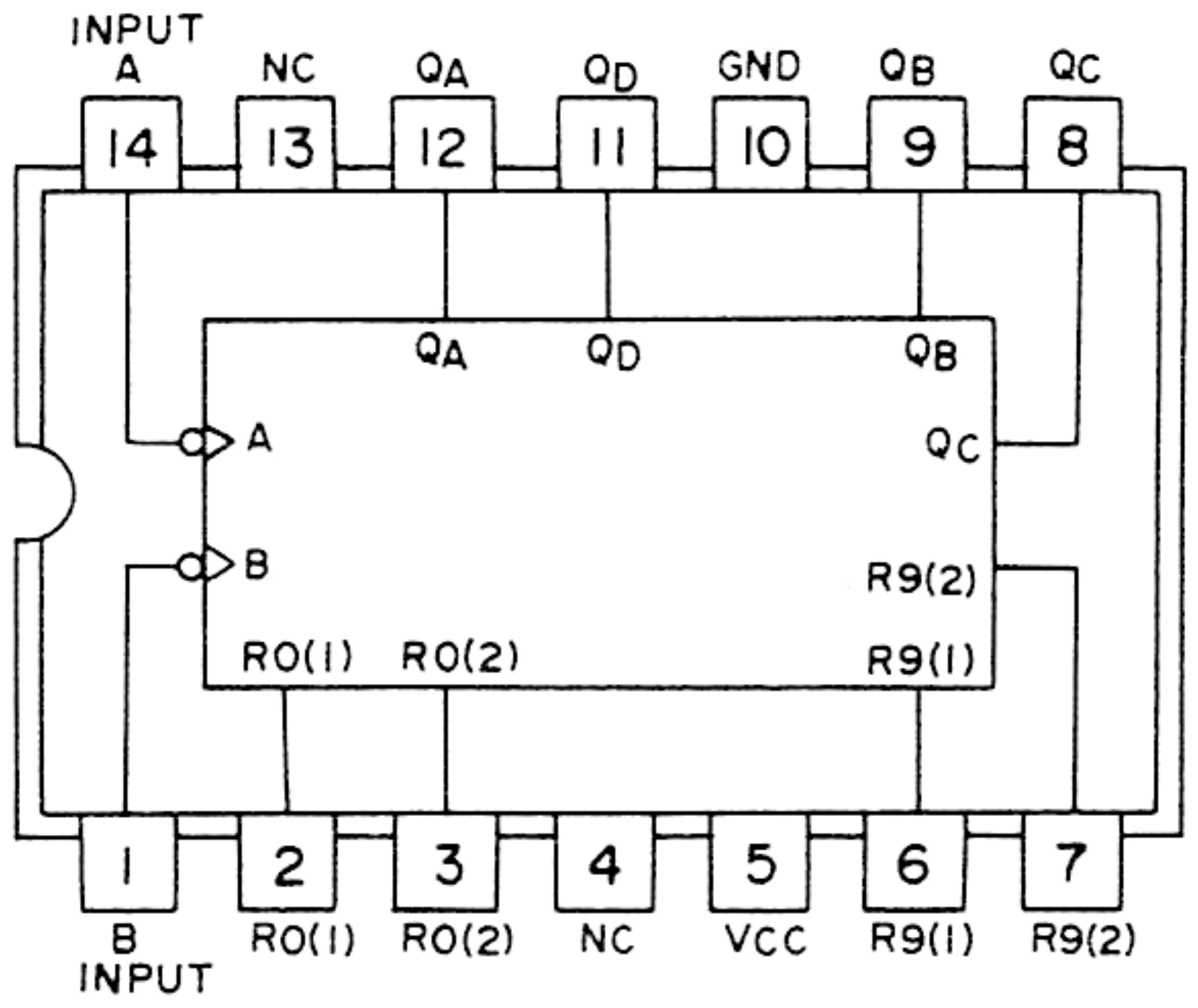
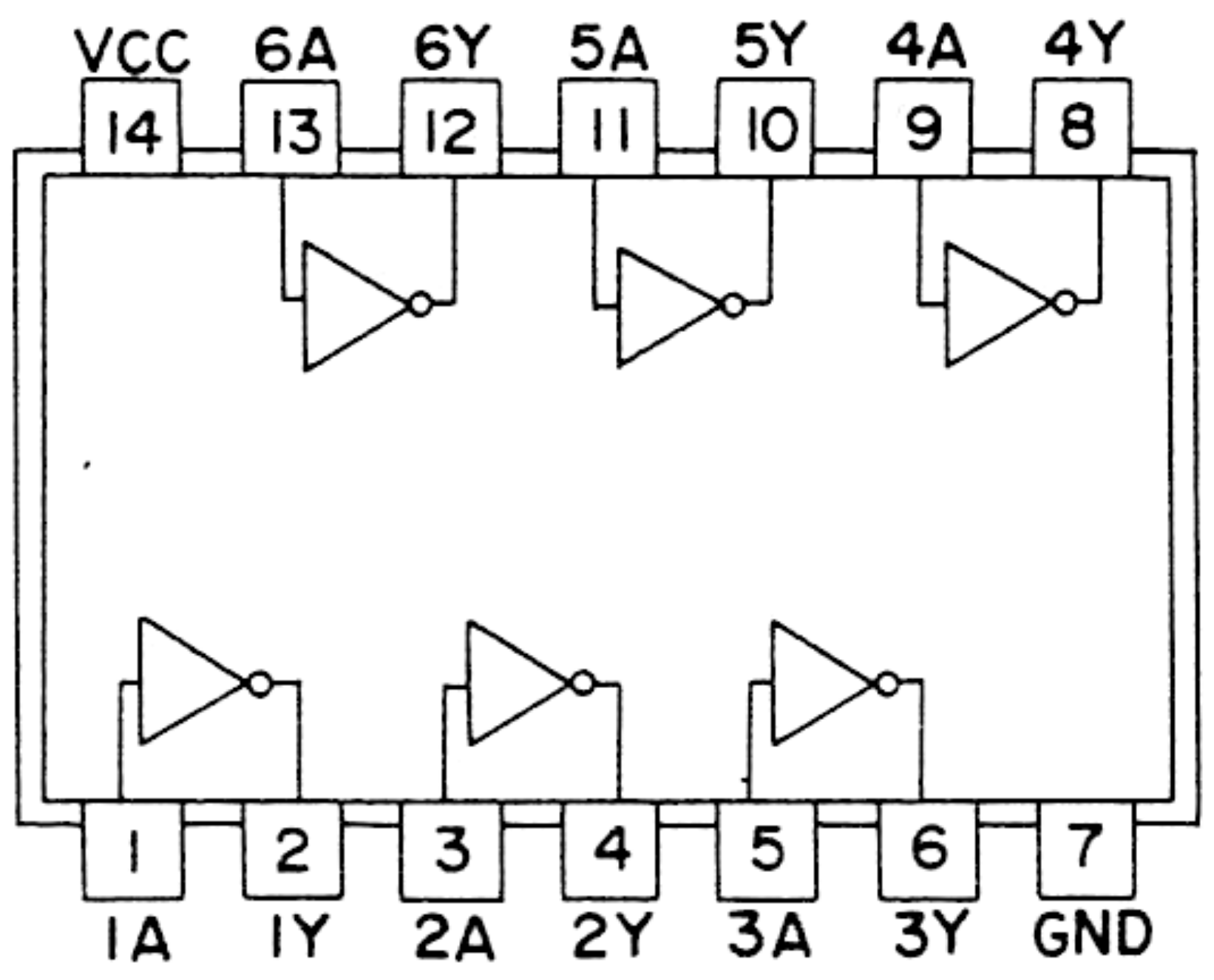
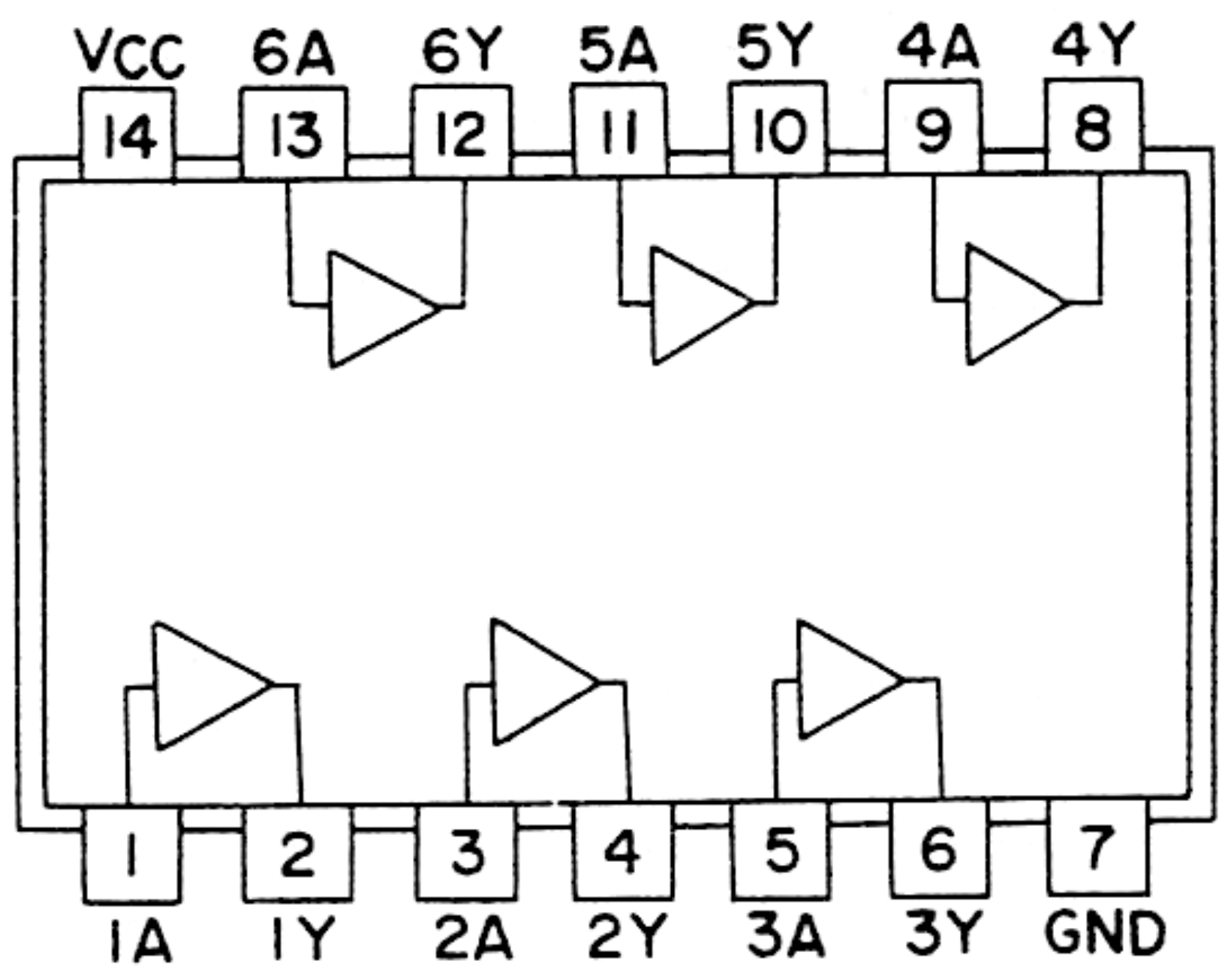


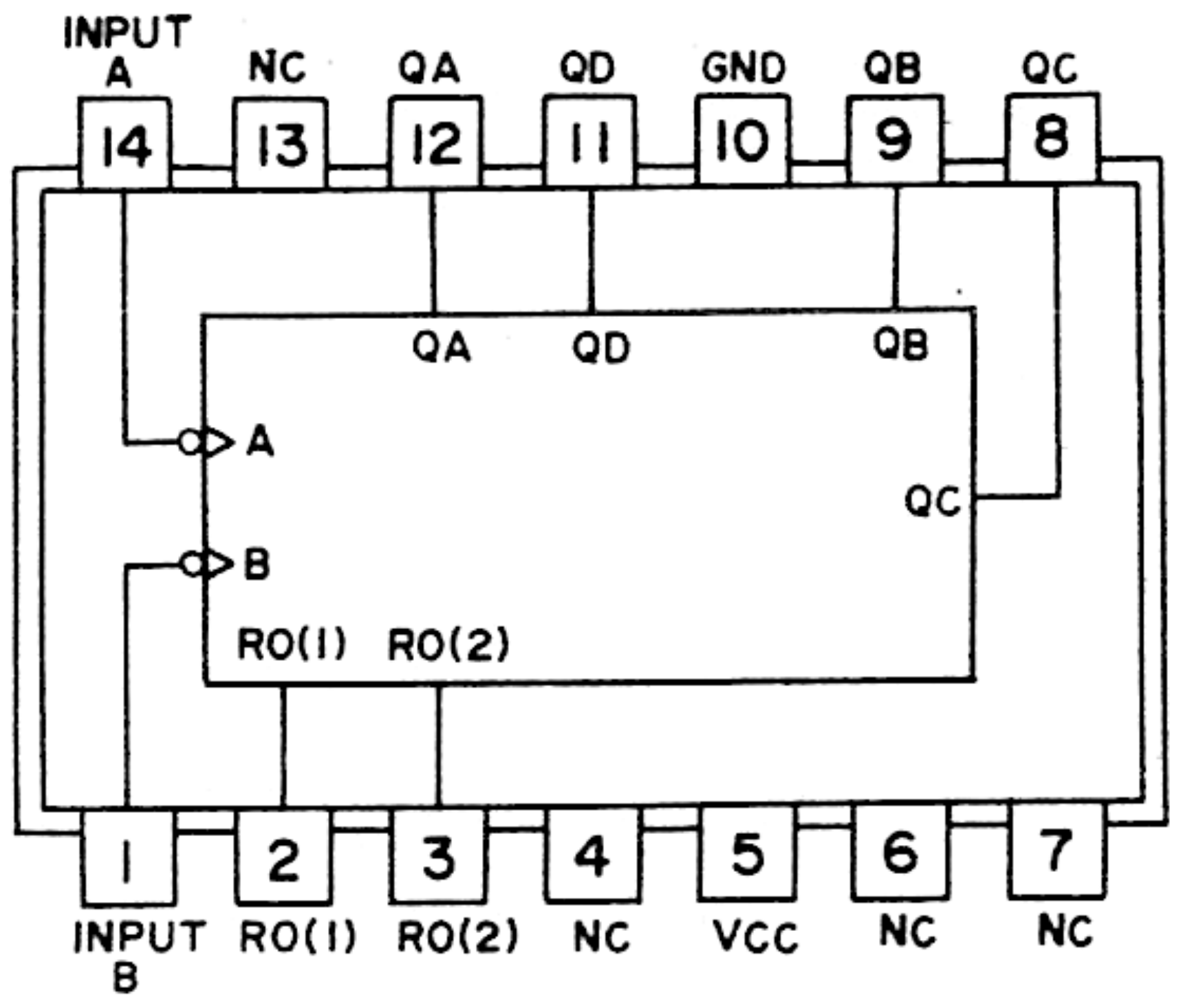
HD7406P
HD74LS04P
SN74S04N



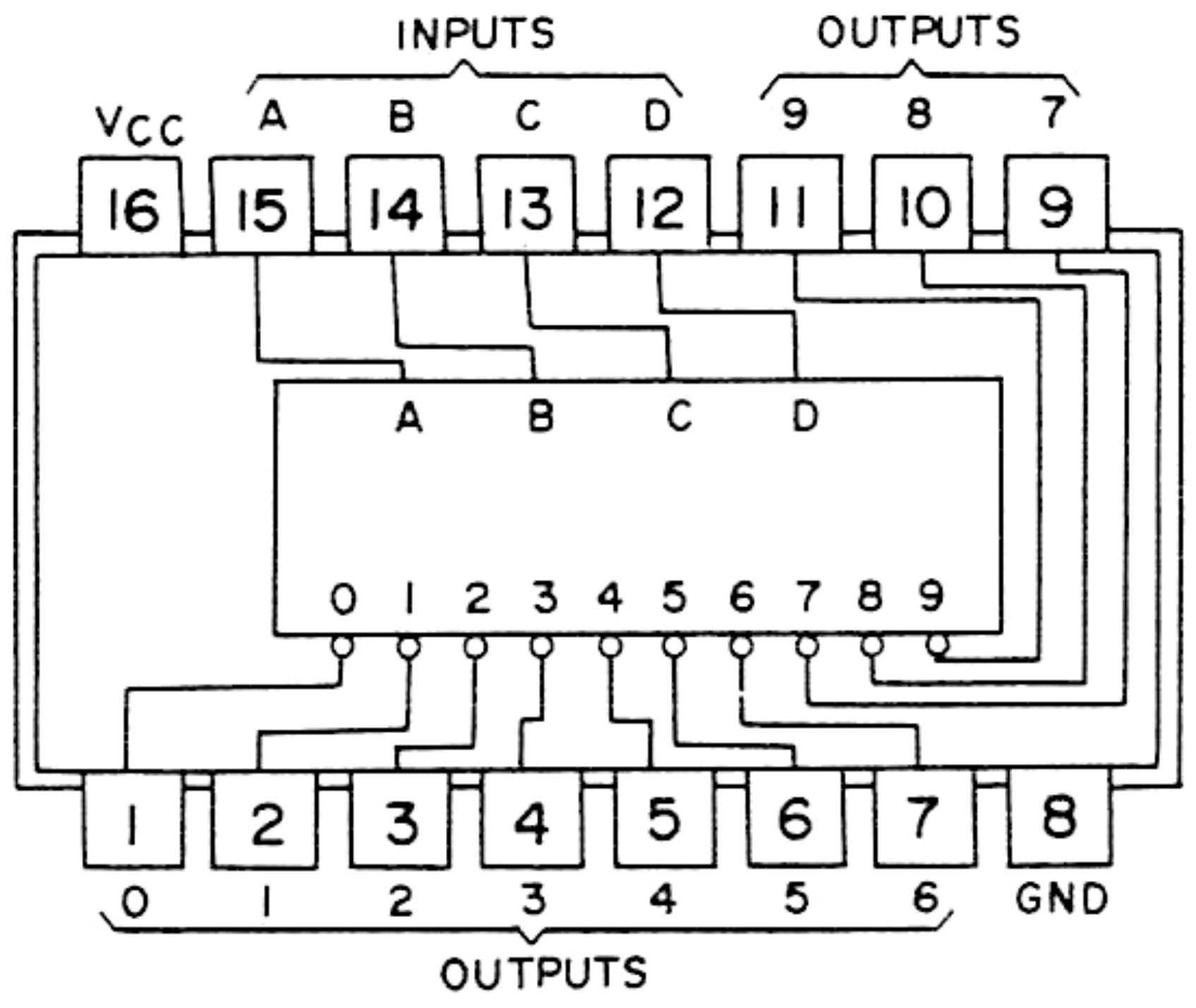
HD7407P



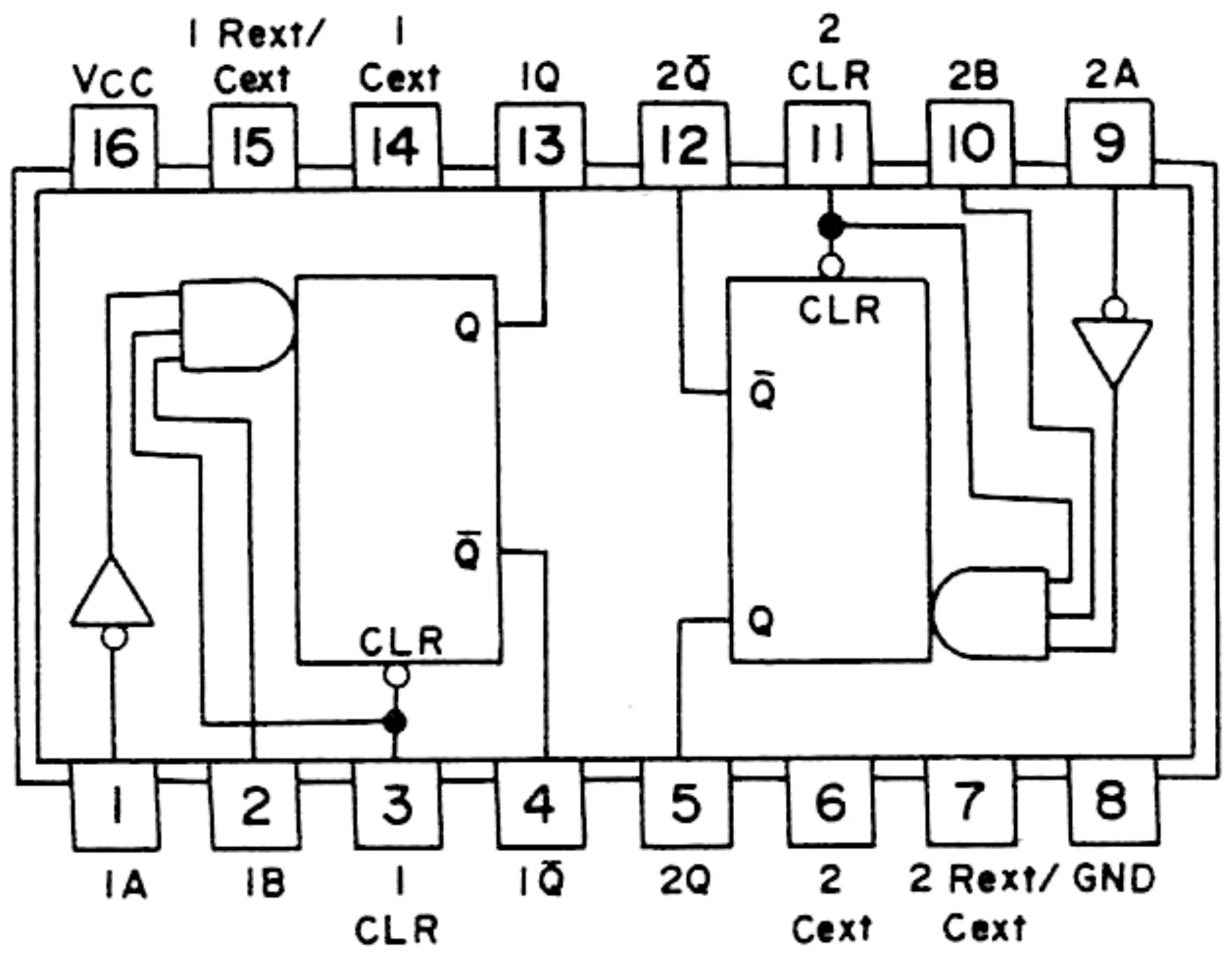
HD7493AP



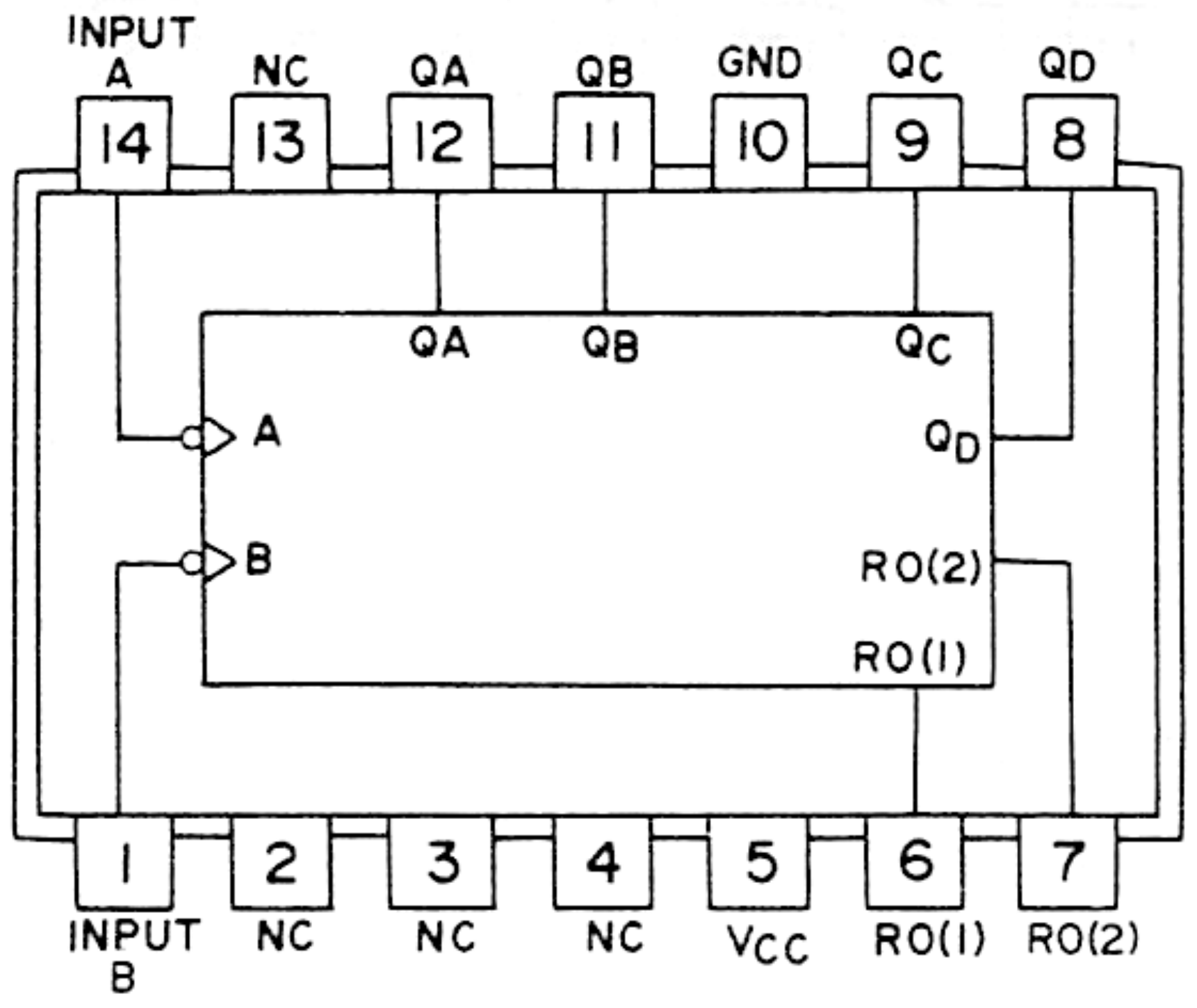
HD7445P



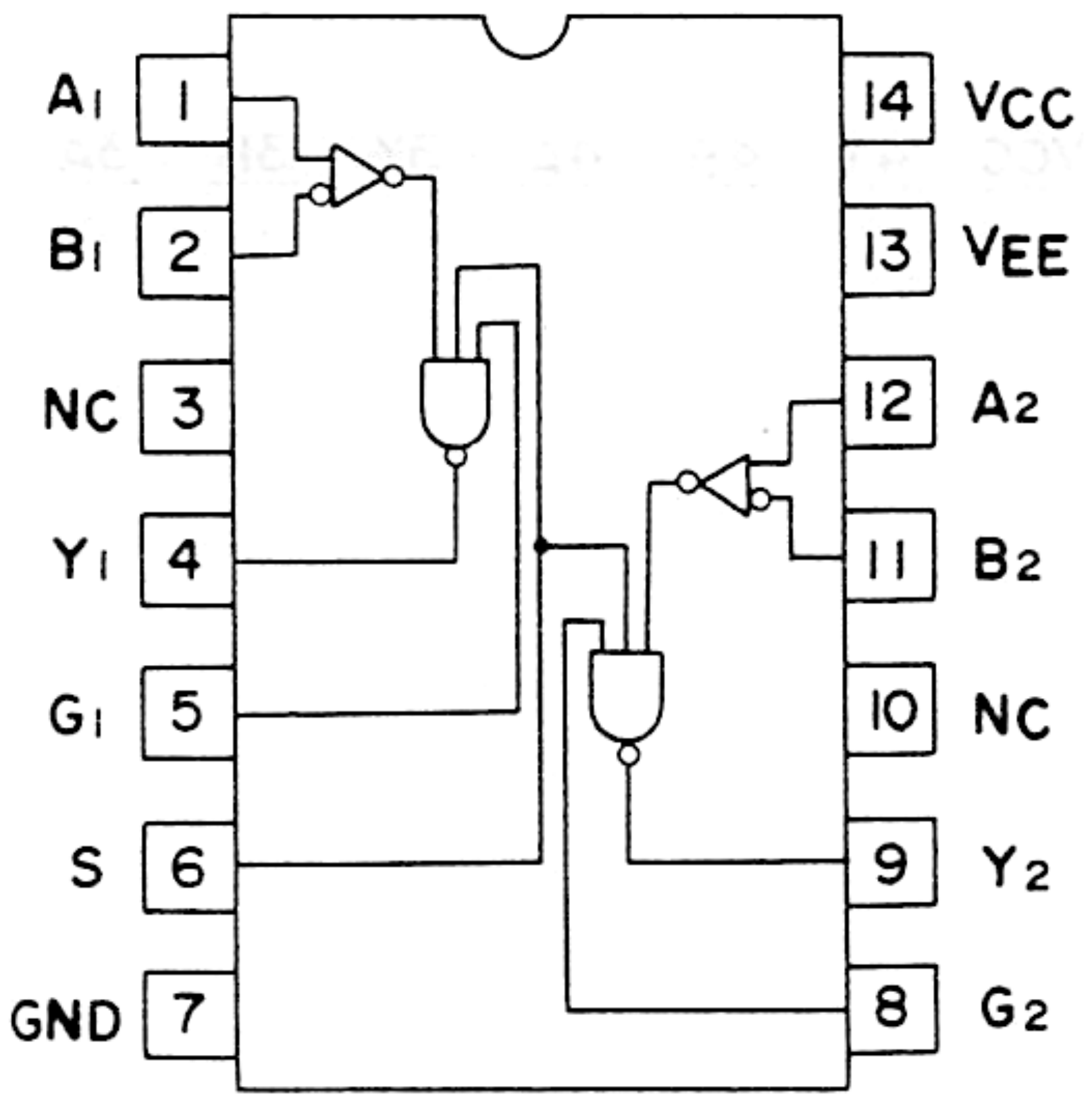
HD74123P
SN74LS123N



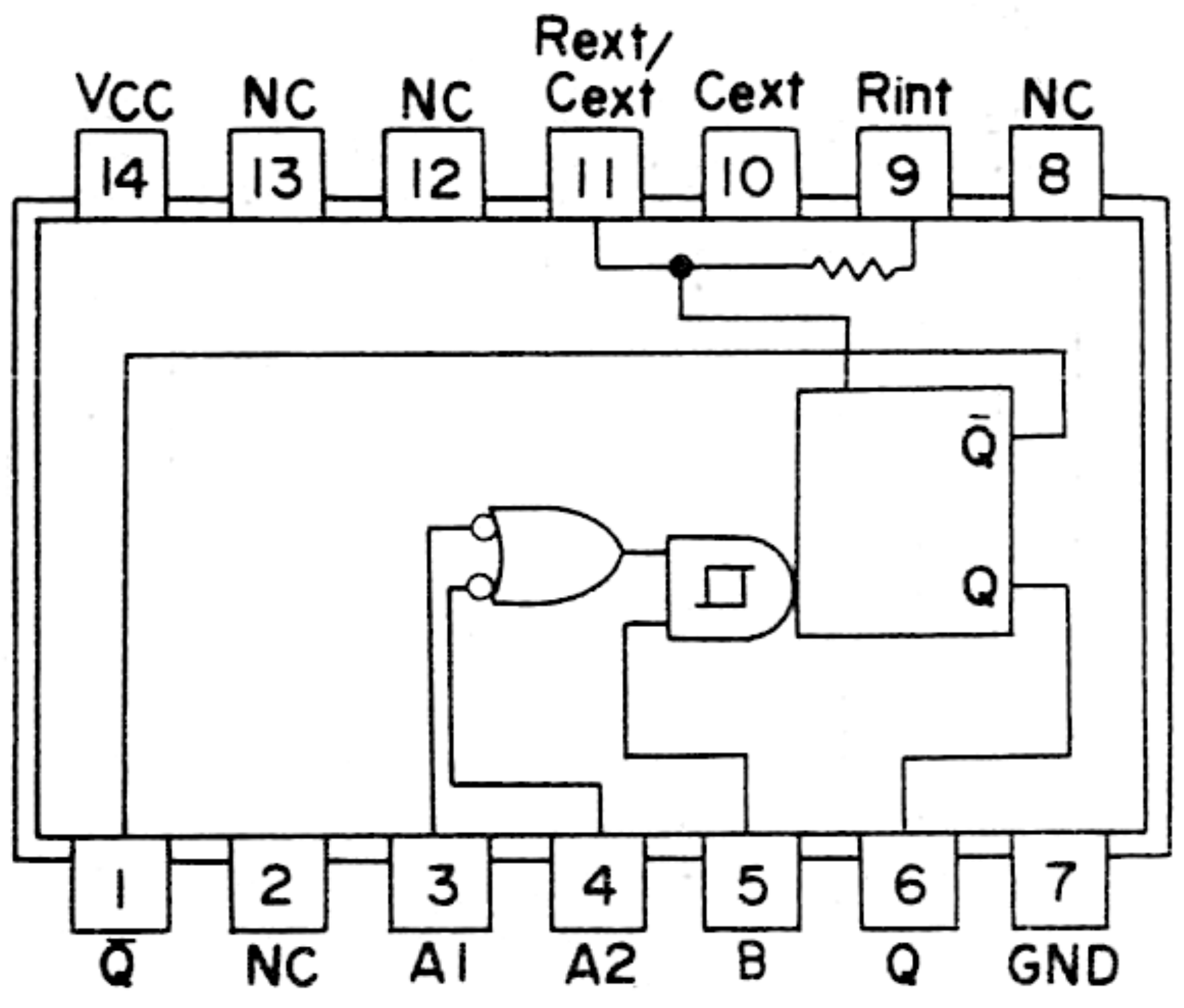
HD7492AP



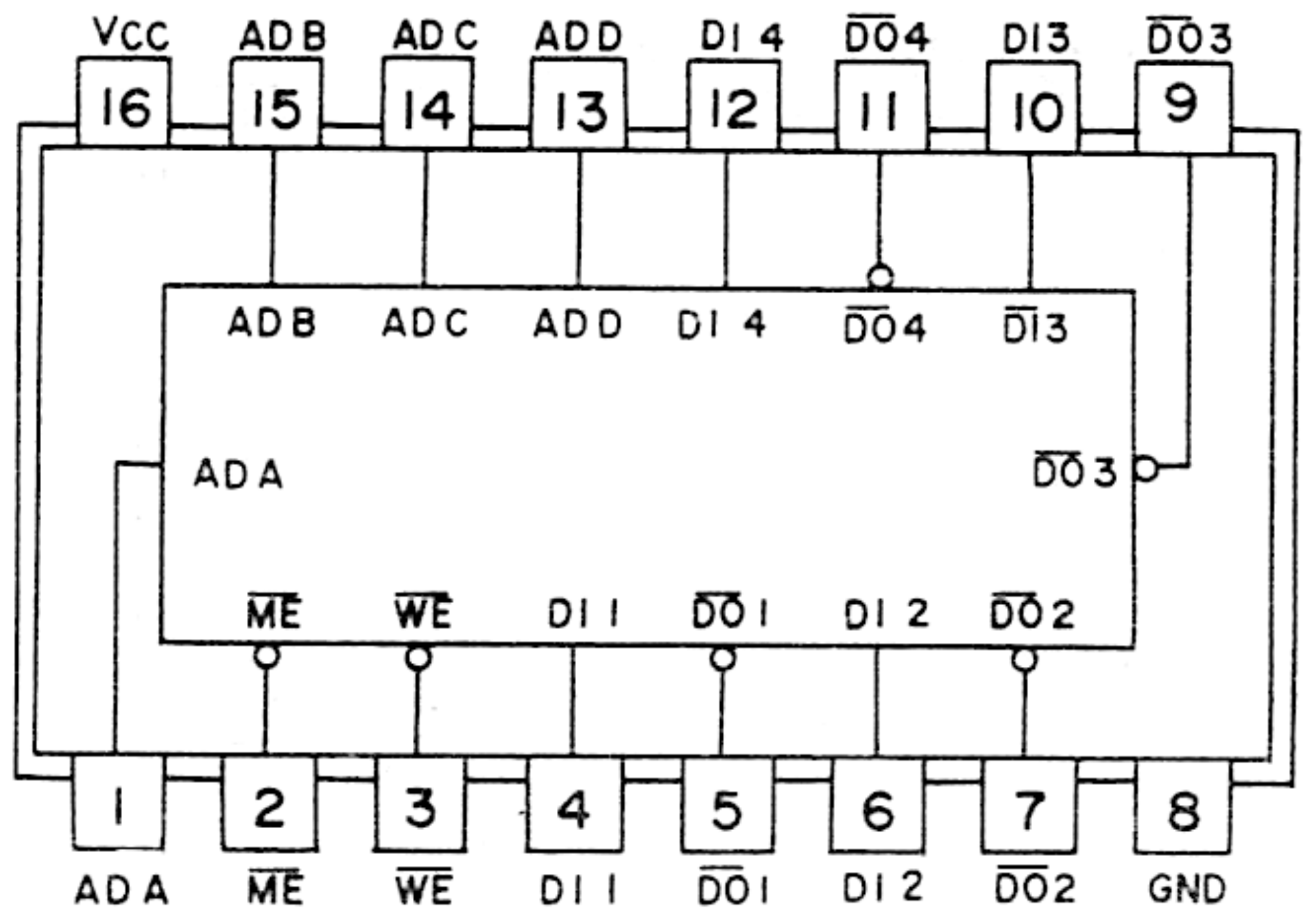
HD75107AP
SN75107AN



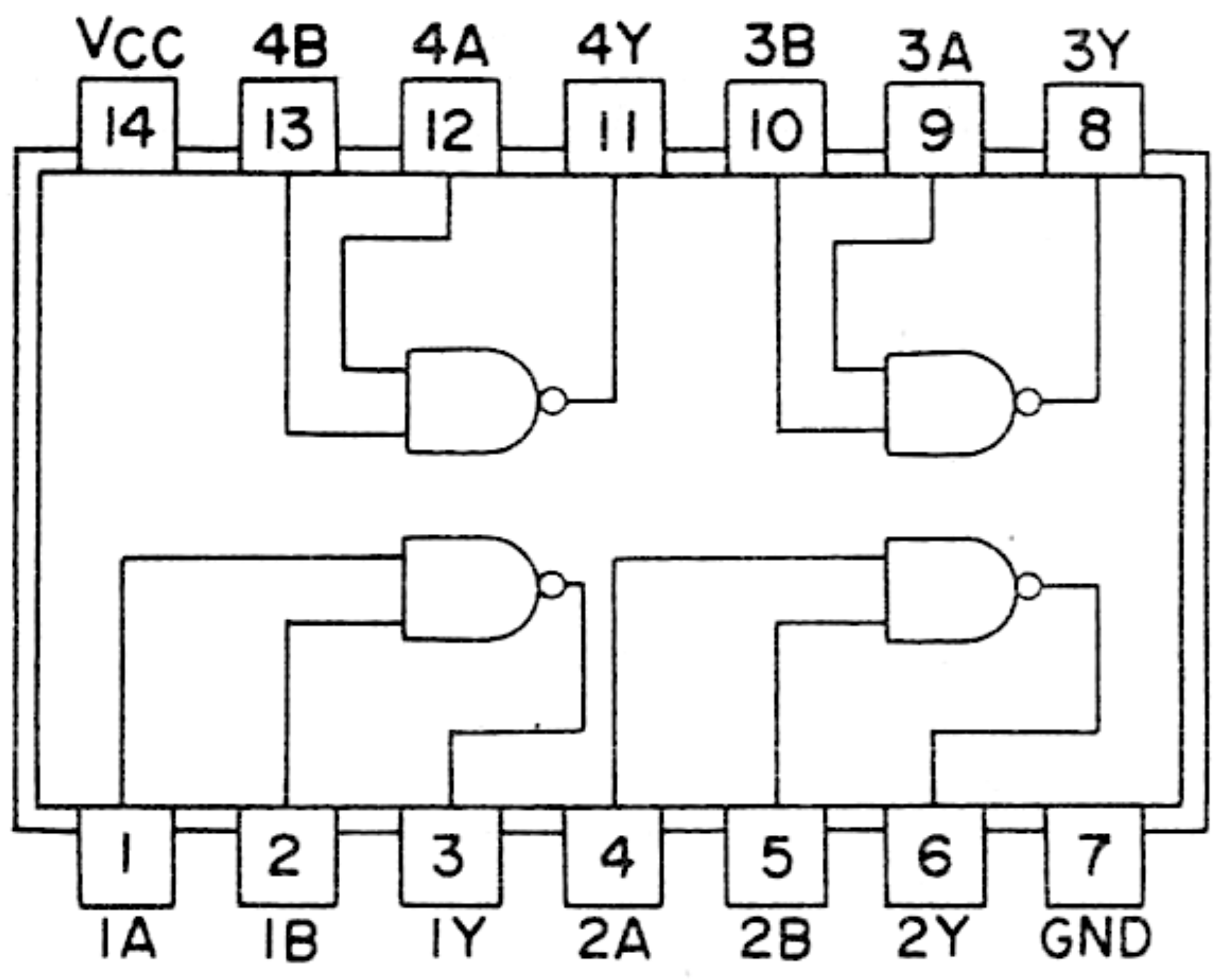
HD74121P



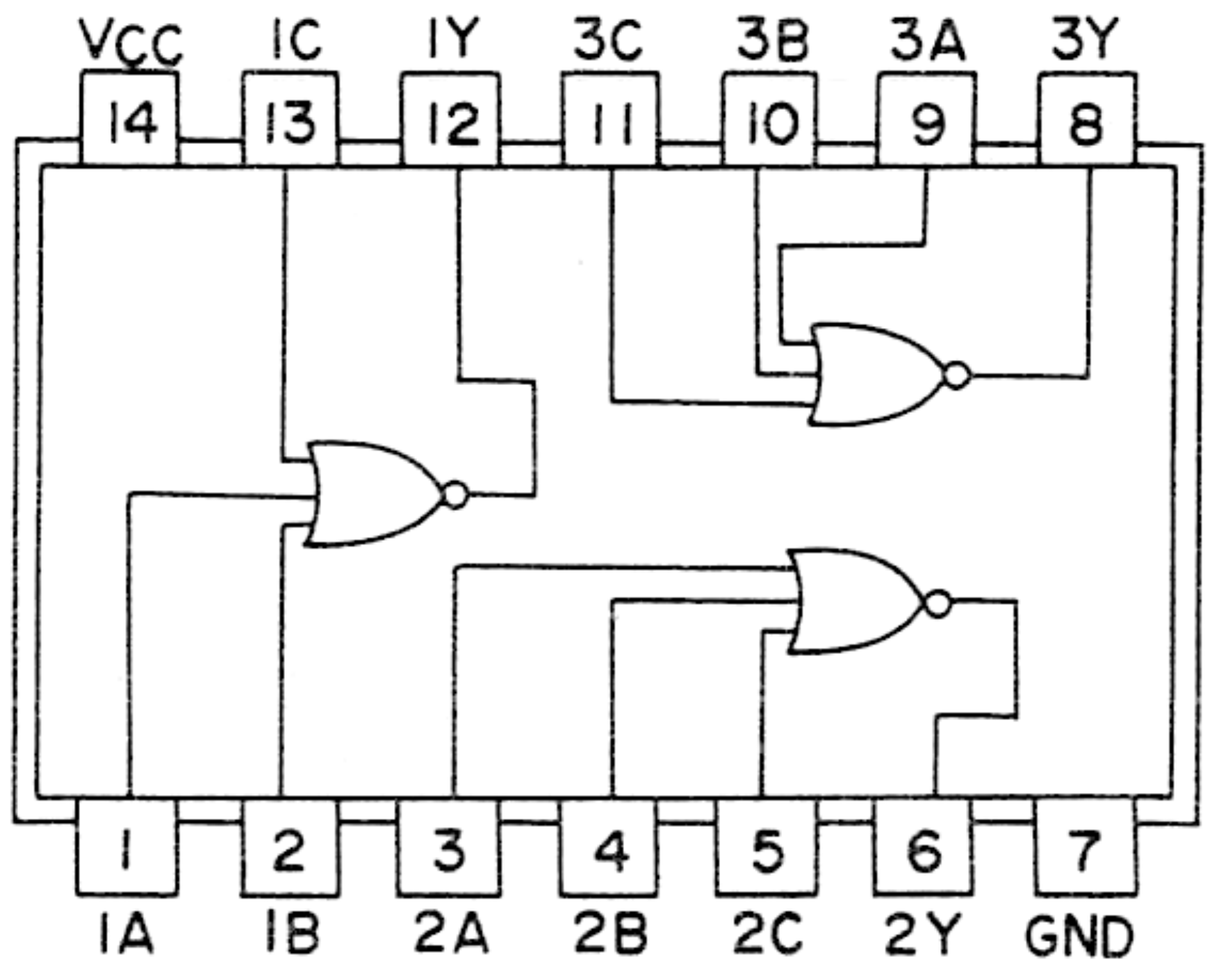
SN7489N



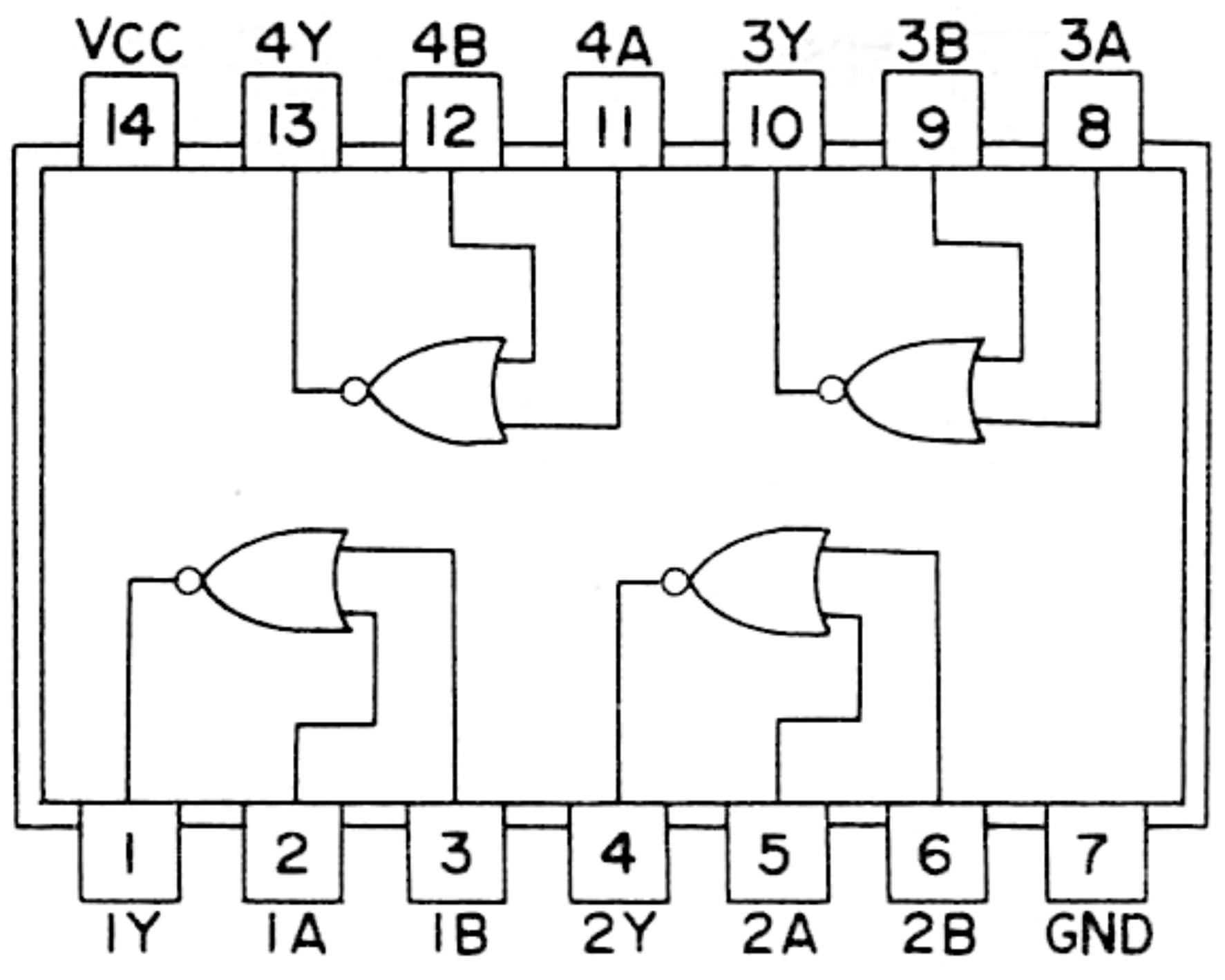
HD74LS00P
HD74LS03P
SN74S00N



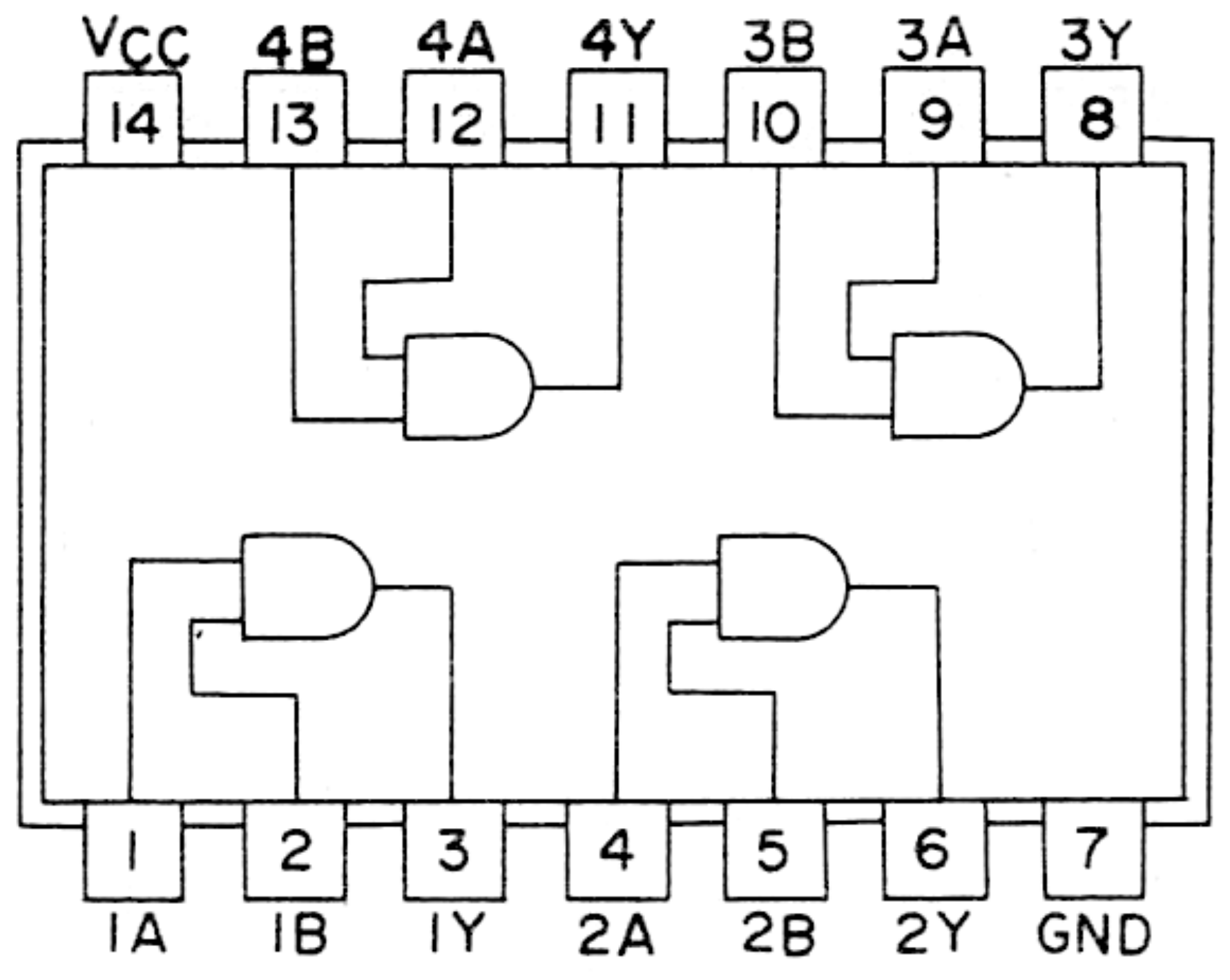
SN74LS27N



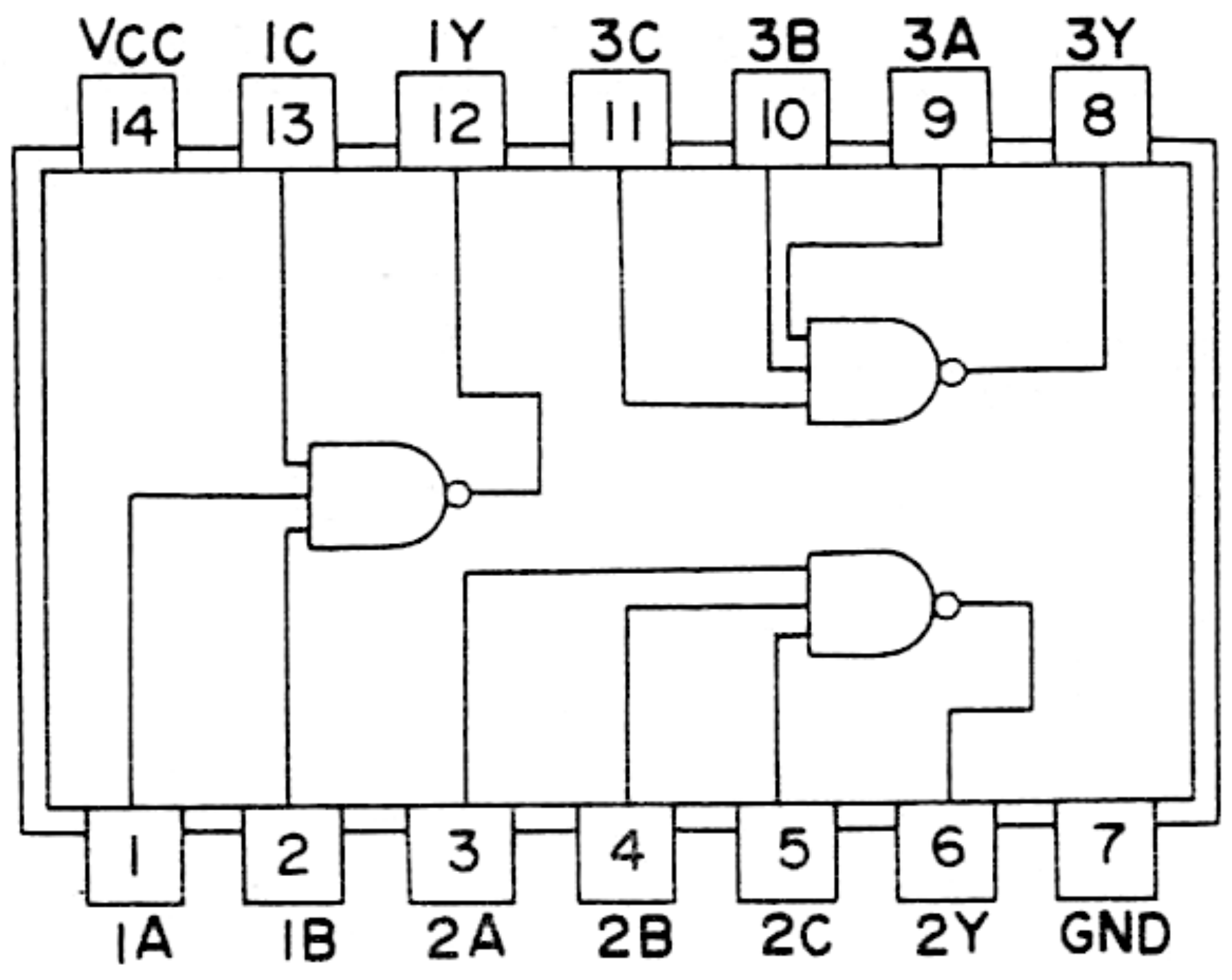
HD74LS02P



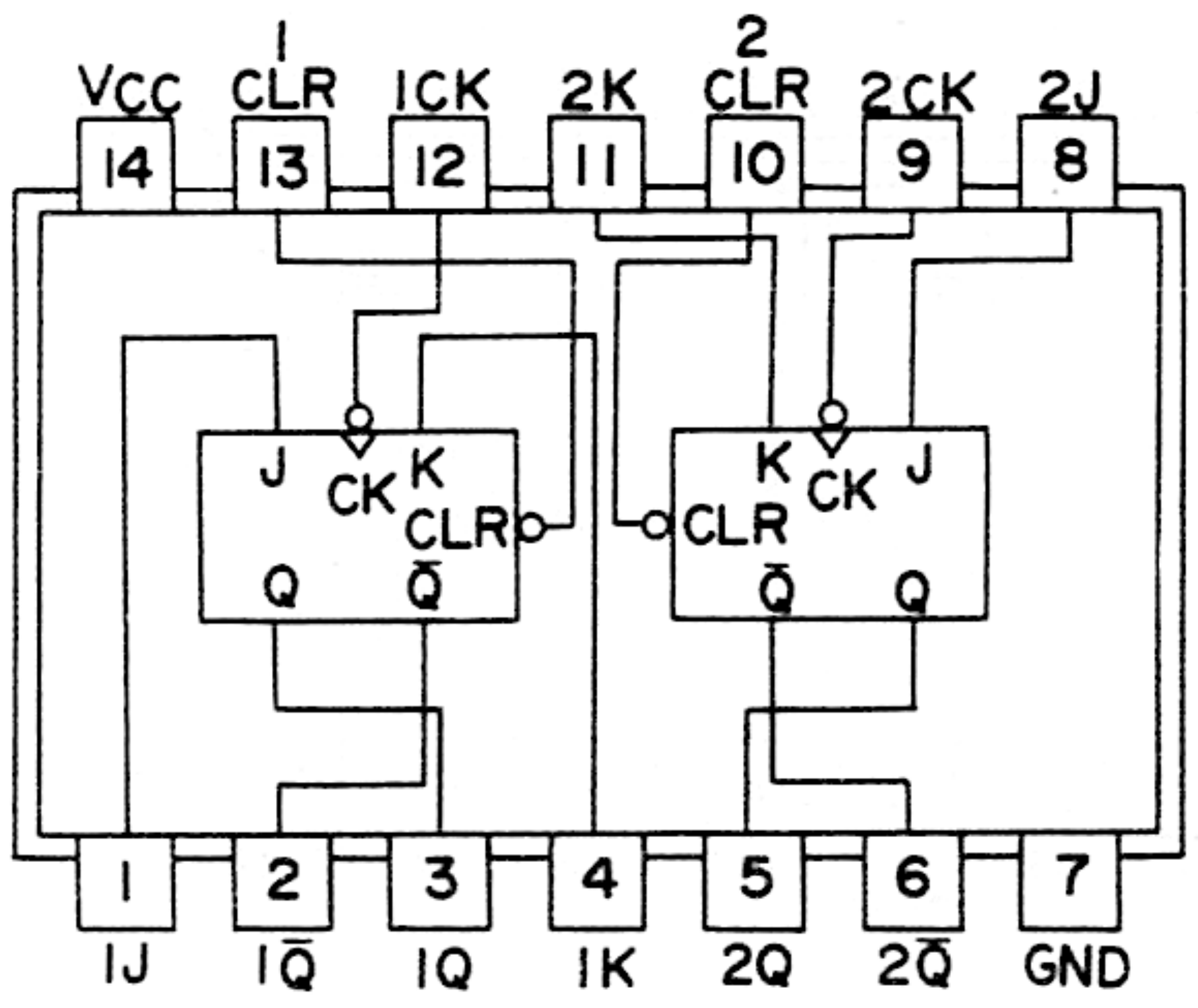
HD74LS08P



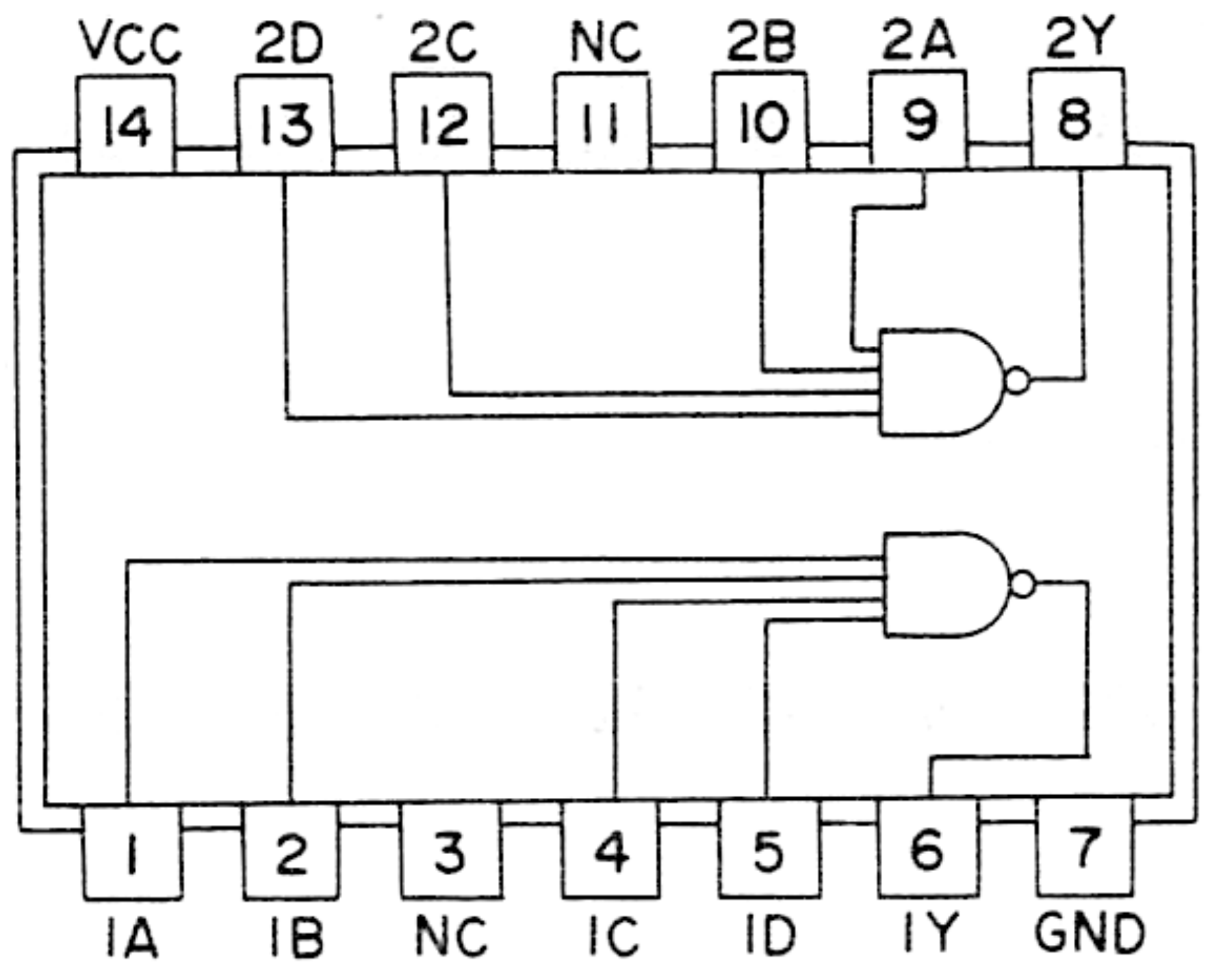
HD74LS10P



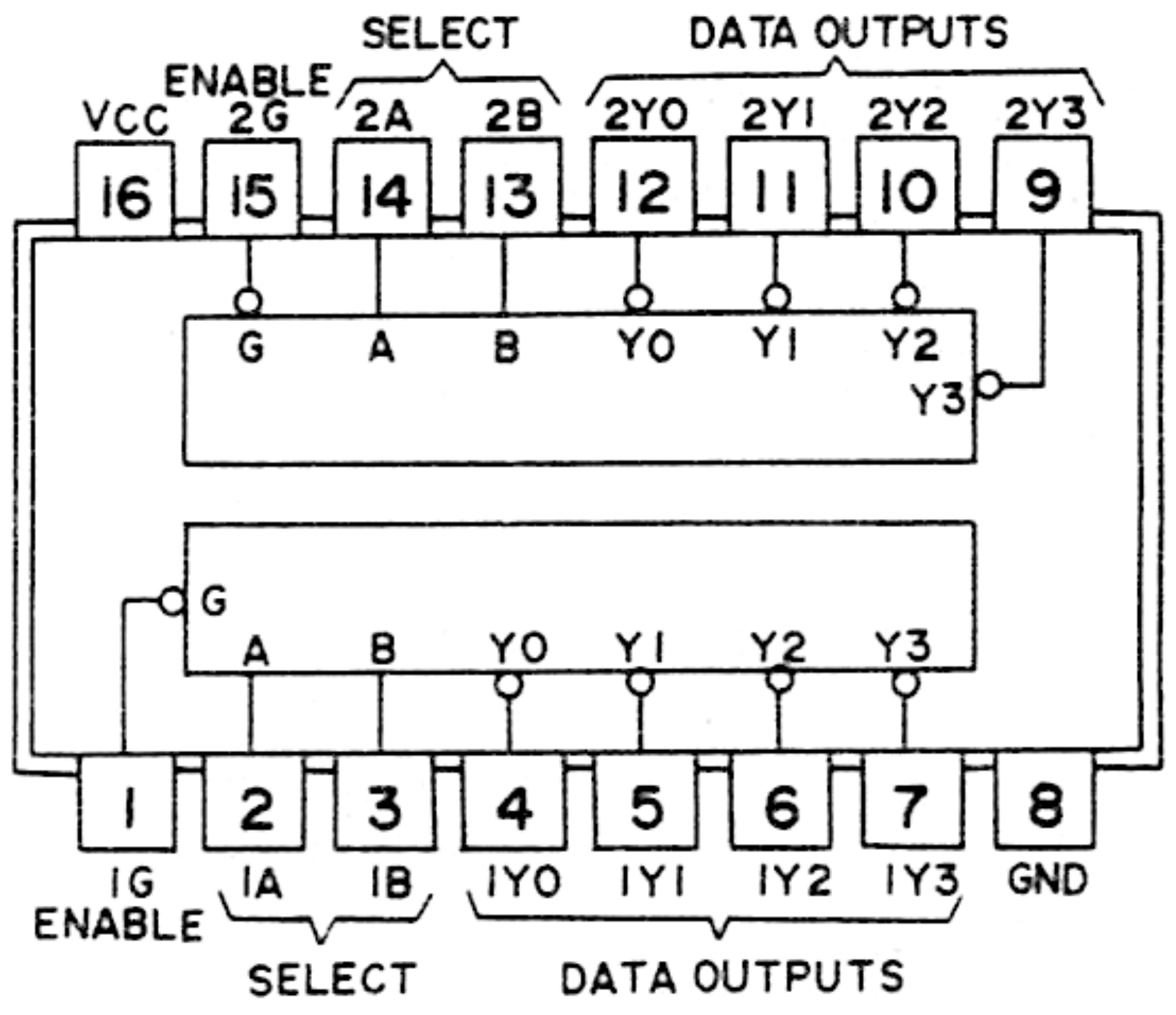
HD74LS107P



HD74LS20P



HD74LS139P



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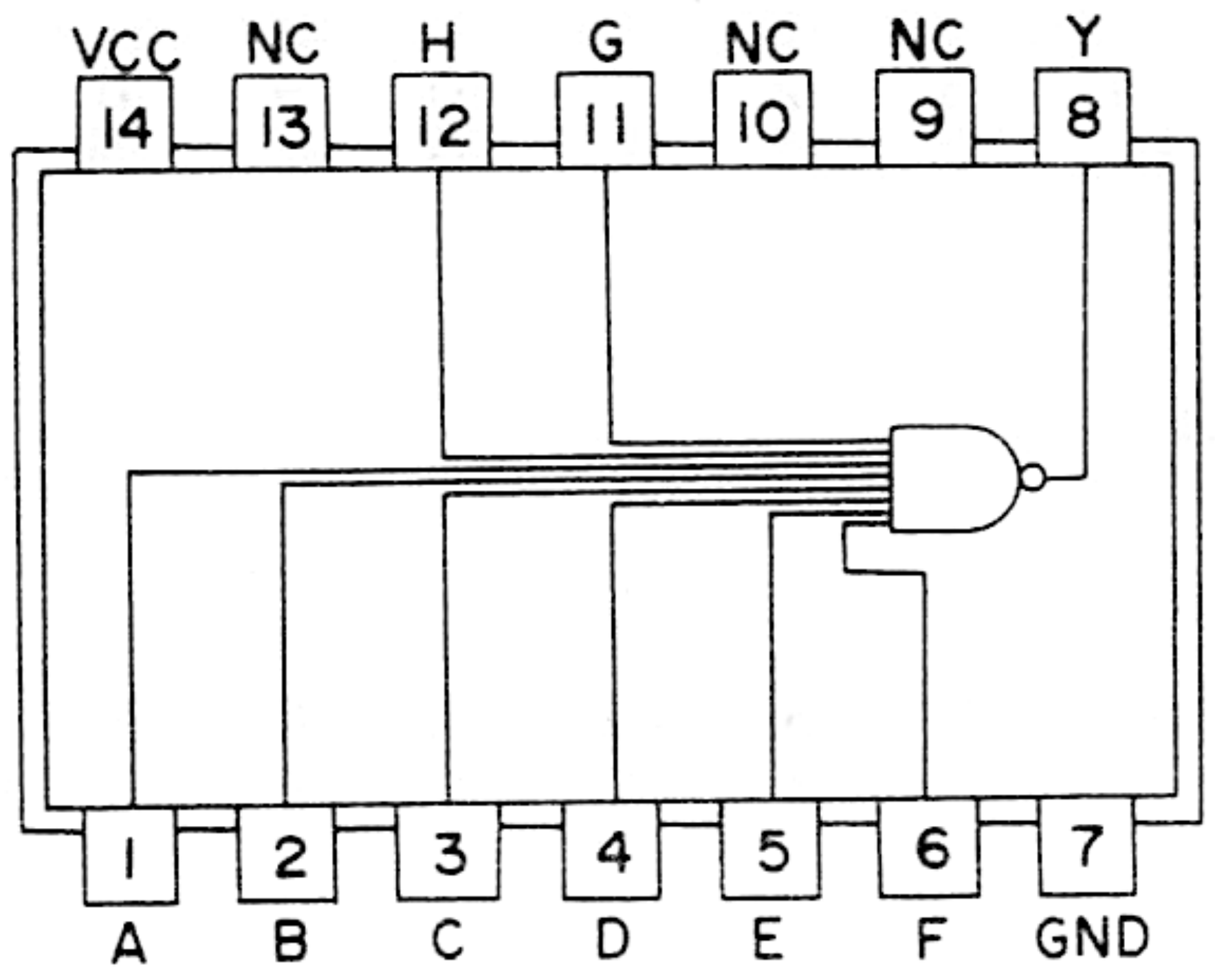
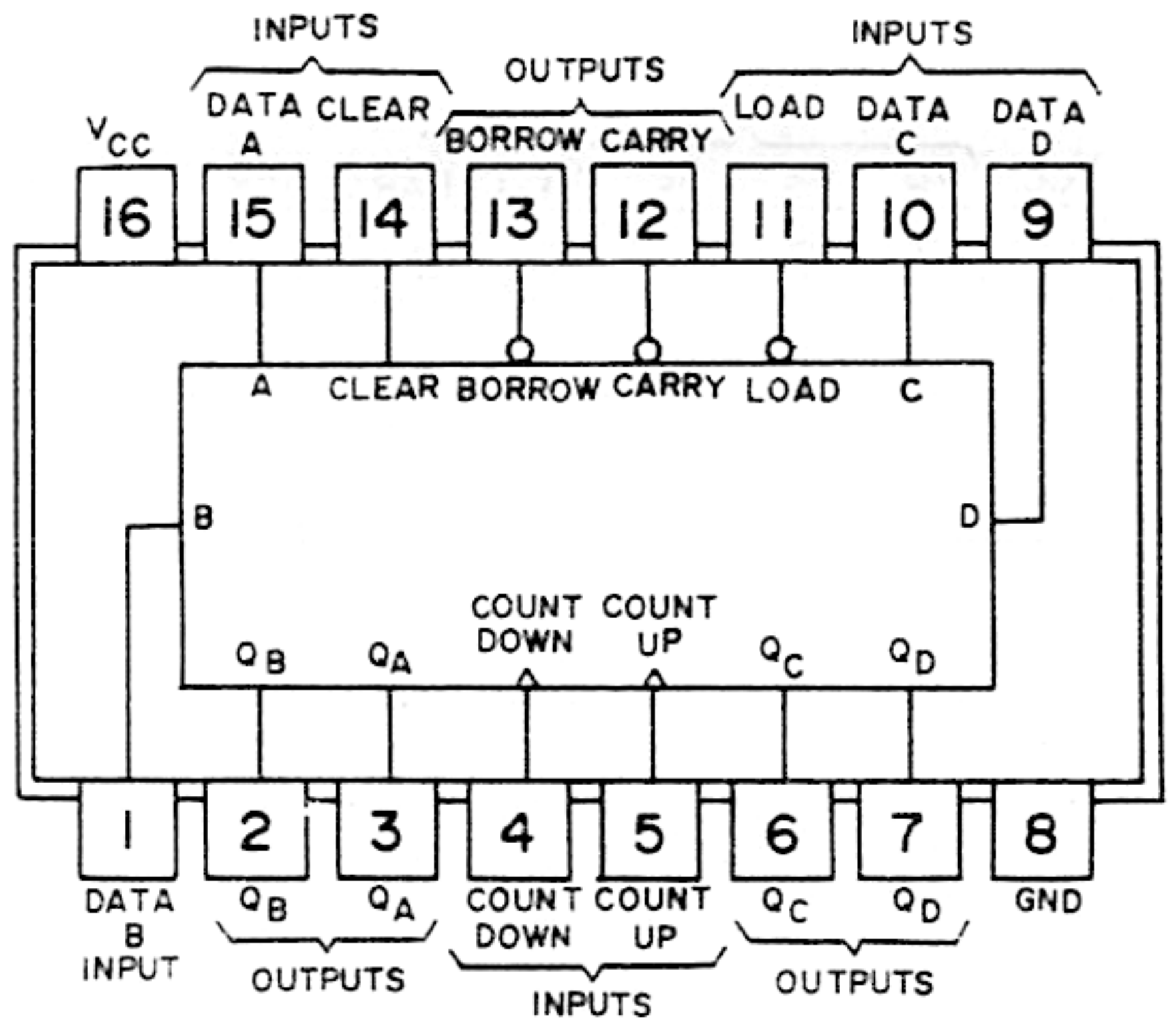


SN74LS193N



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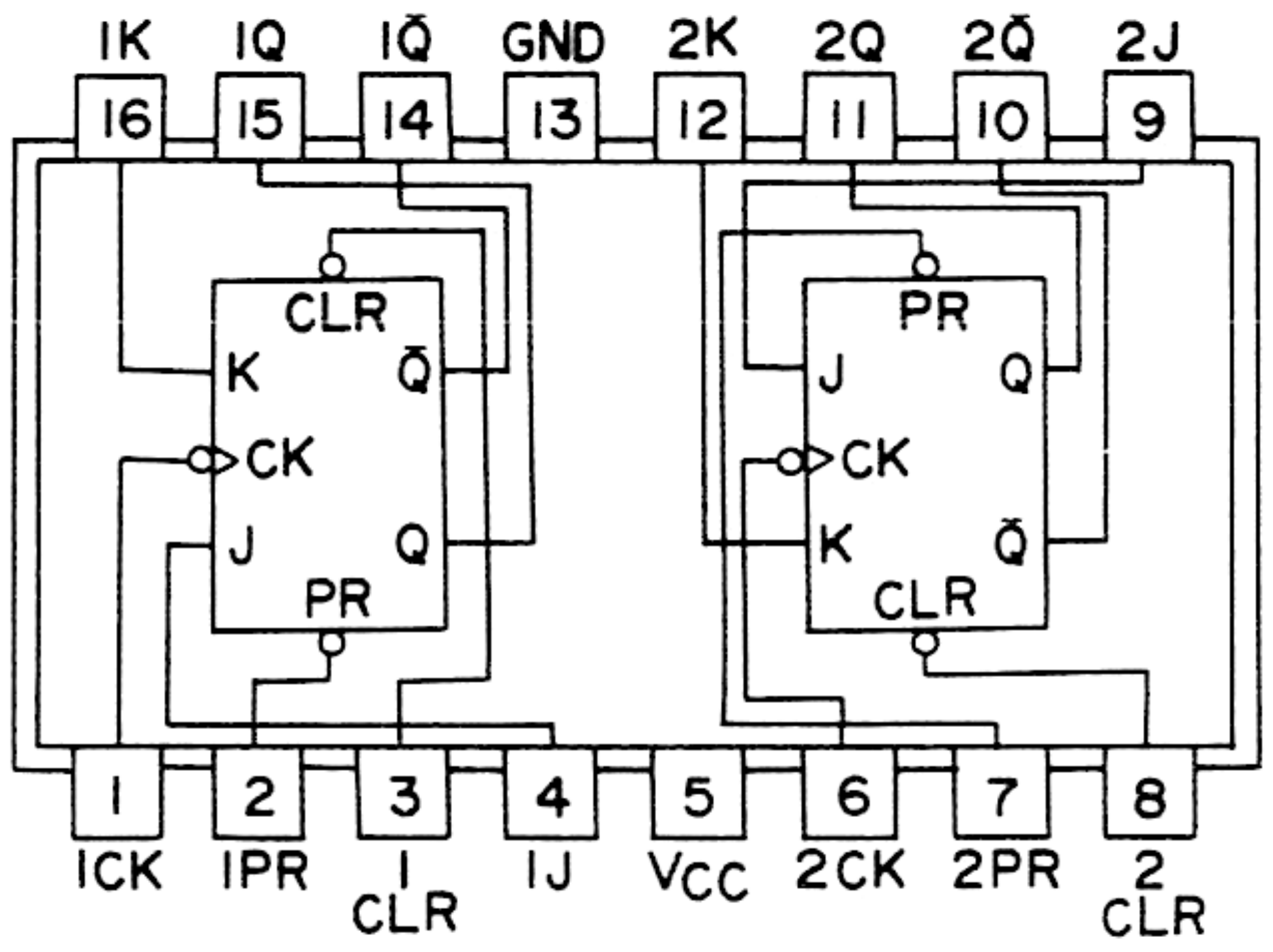

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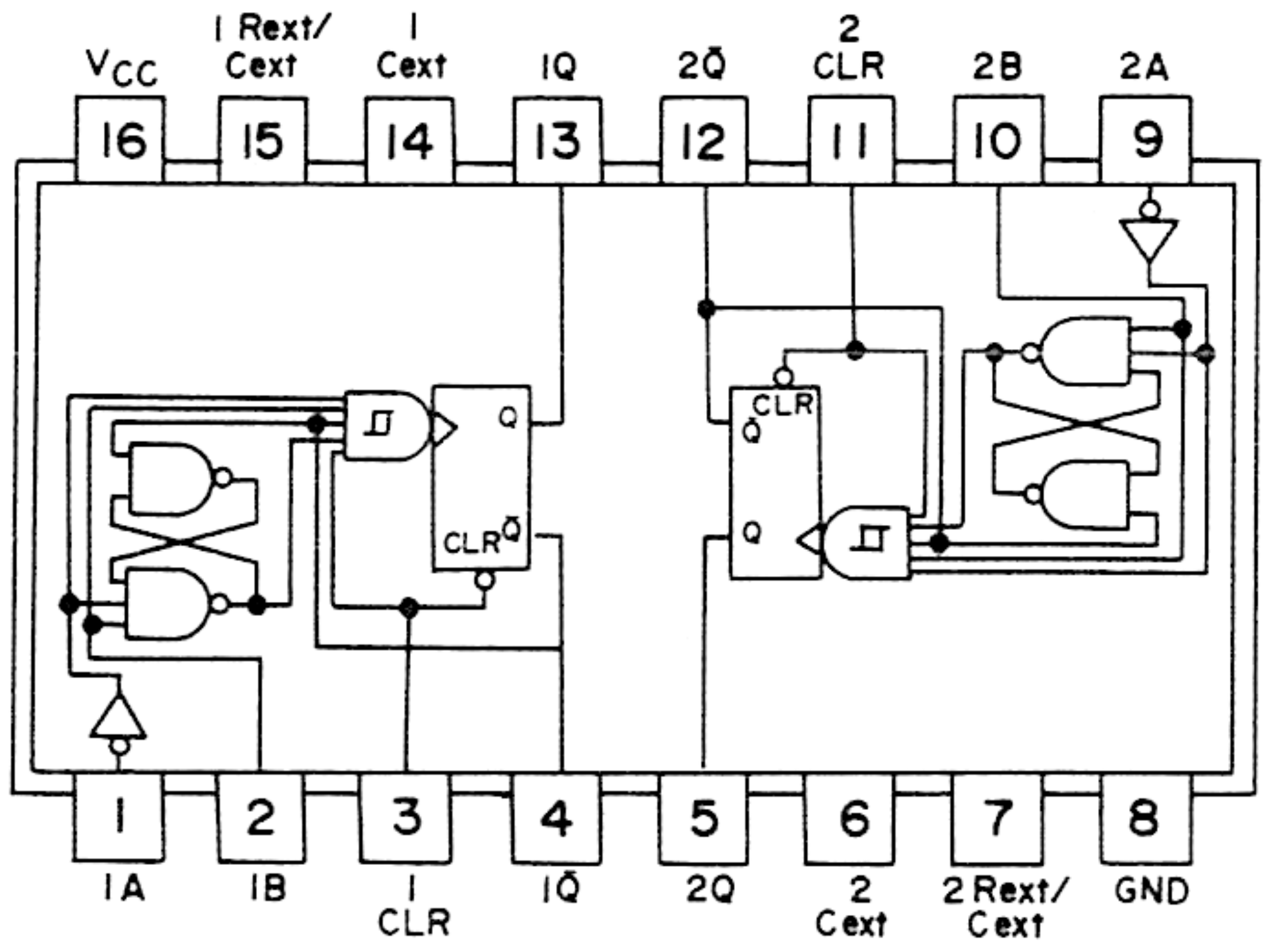

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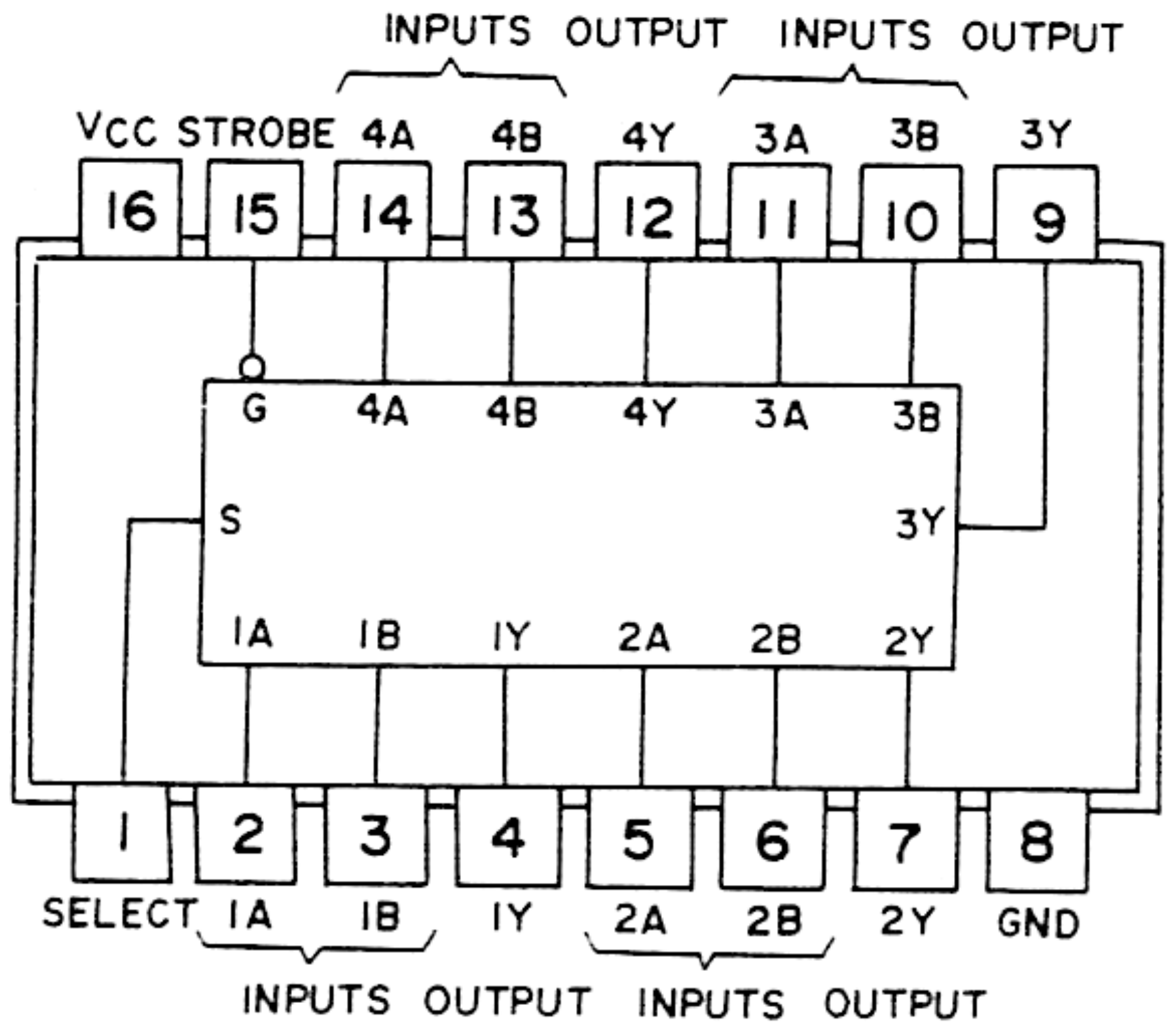
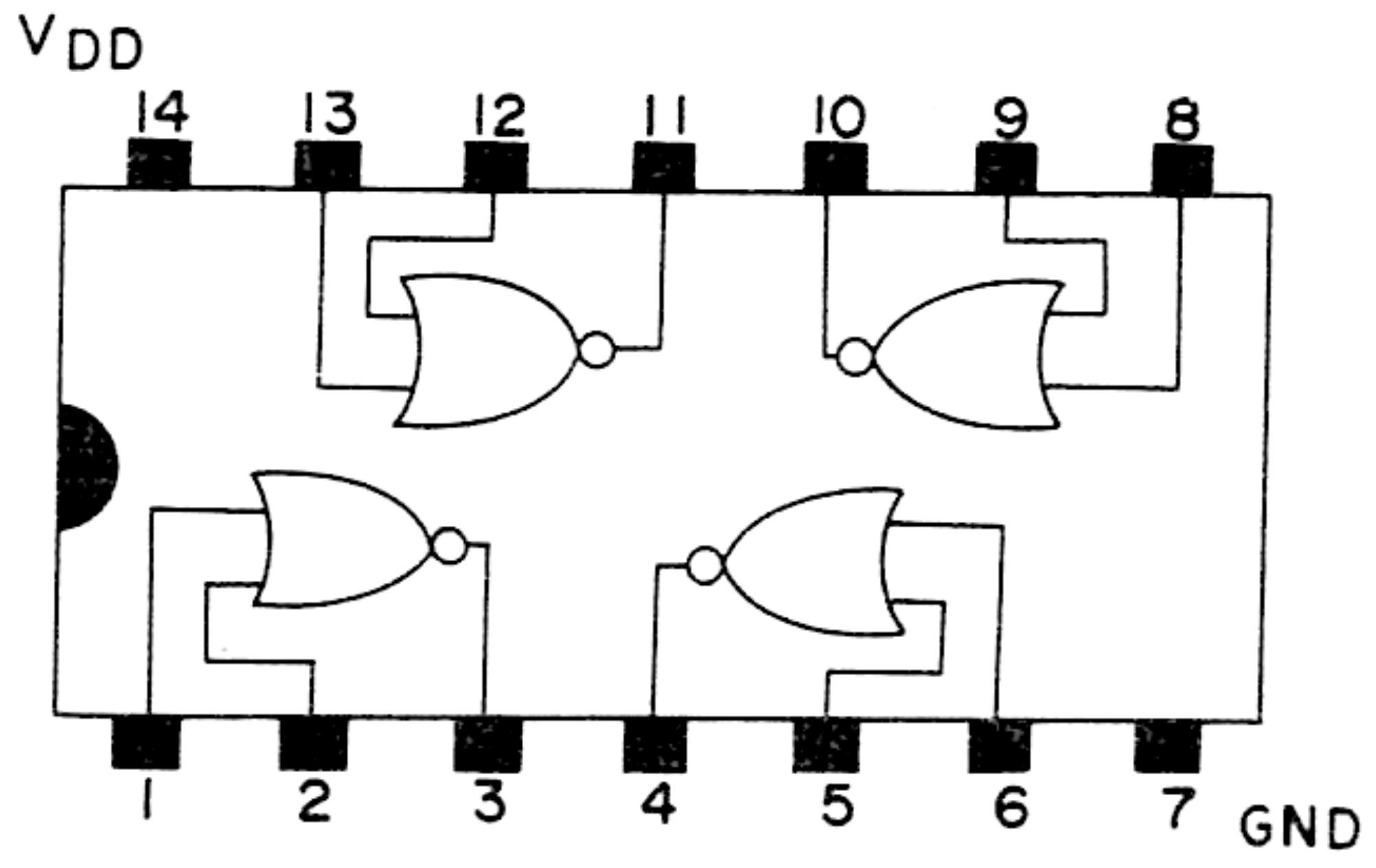
16 15 14 13 12 11 10 9
Q CLR Q̄
CLR Q̄ Q
1 2 3 4 5 6 7 8
1A 1B 1 CLR 1Q̄ 2Q 2 Cext 2 Rext/Cext GND

SN74LS157N



INPUTS OUTPUT INPUTS OUTPUT
VCC STROBE 4A 4B 4Y 3A 3B 3Y
16 15 14 13 12 11 10 9
G 4A 4B 4Y 3A 3B
S 3Y
1A 1B 1Y 2A 2B 2Y
1 2 3 4 5 6 7 8
SELECT 1A 1B 1Y 2A 2B 2Y GND
INPUTS OUTPUT INPUTS OUTPUT

TC4001BP



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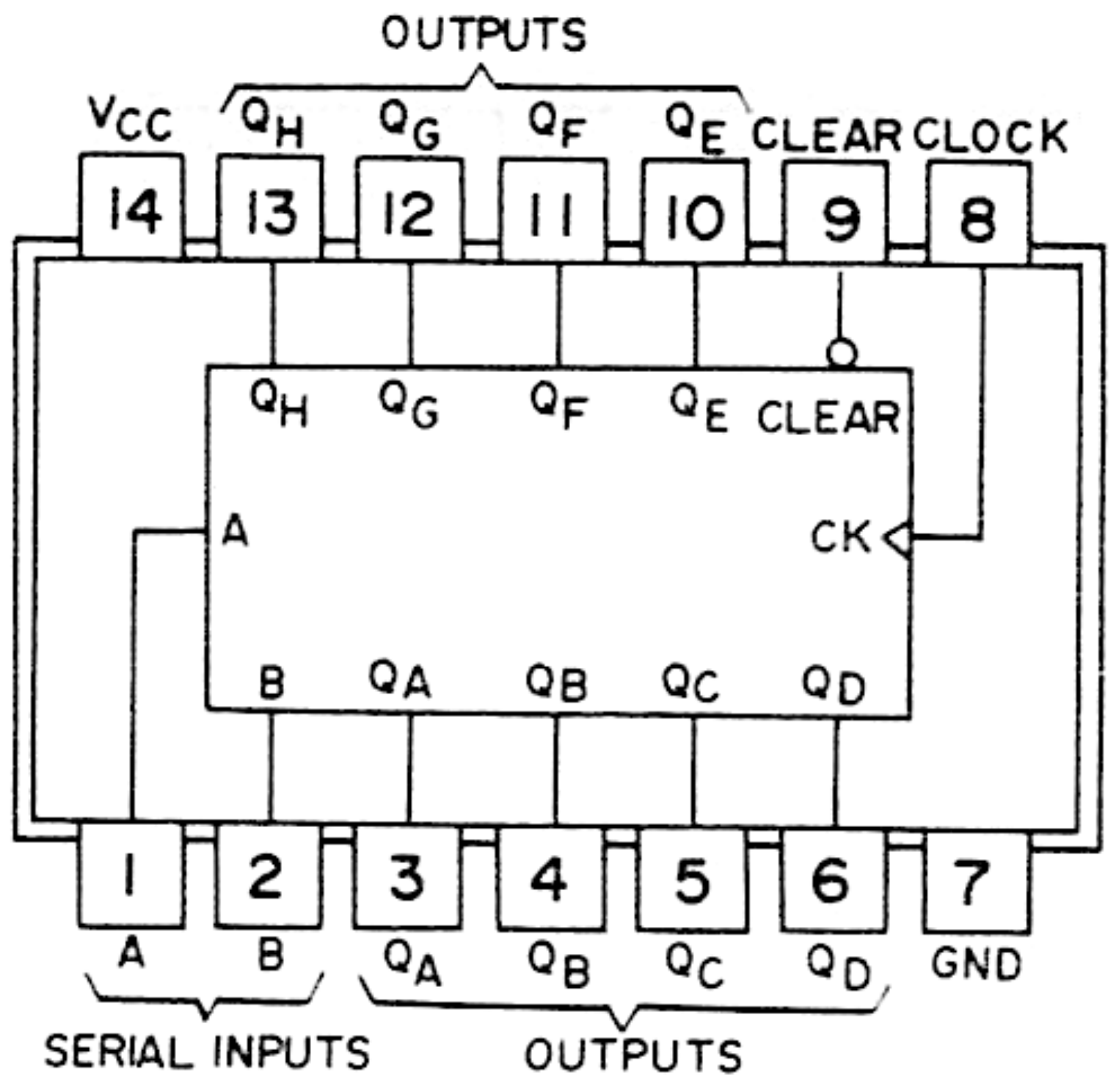

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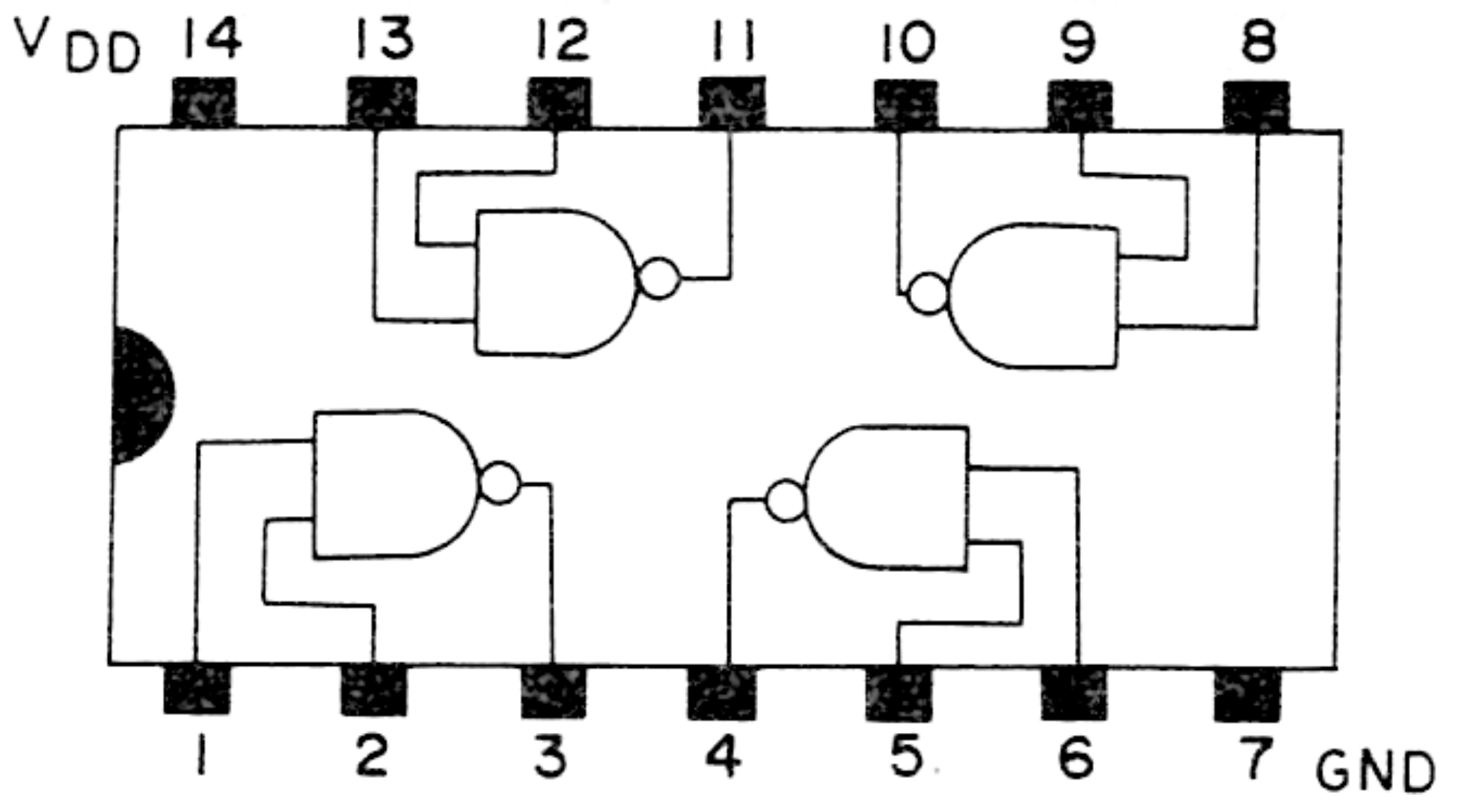

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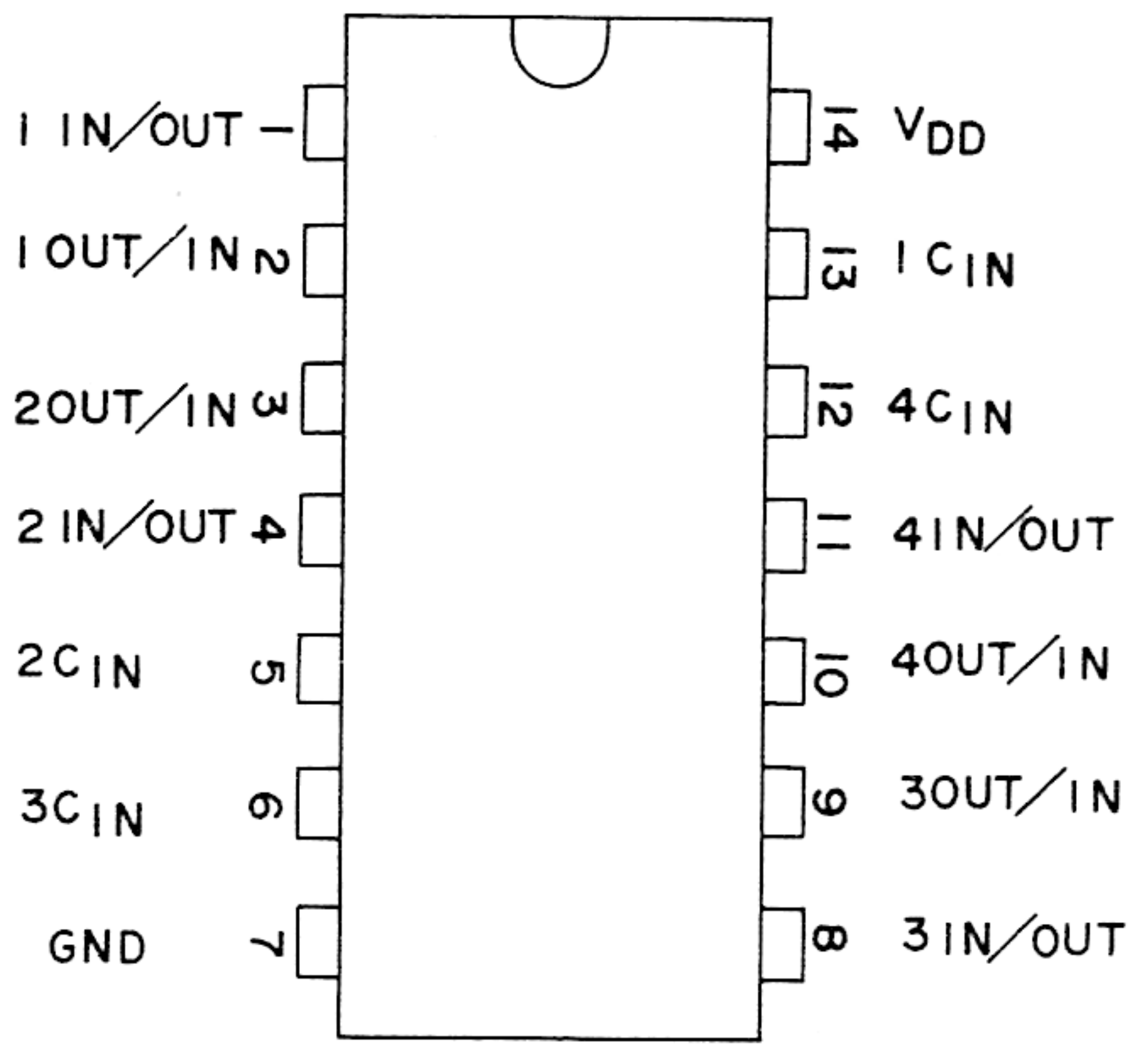

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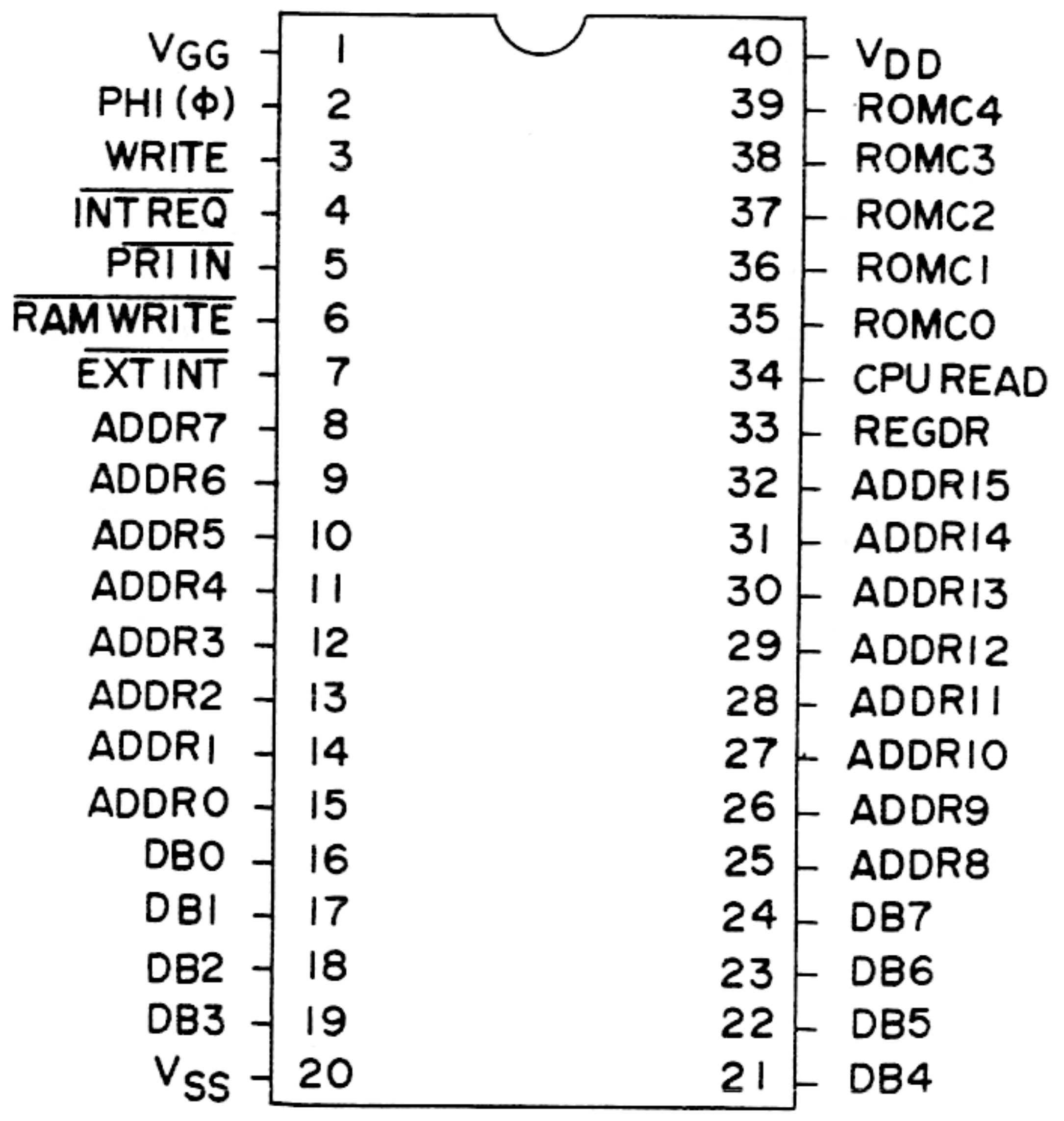

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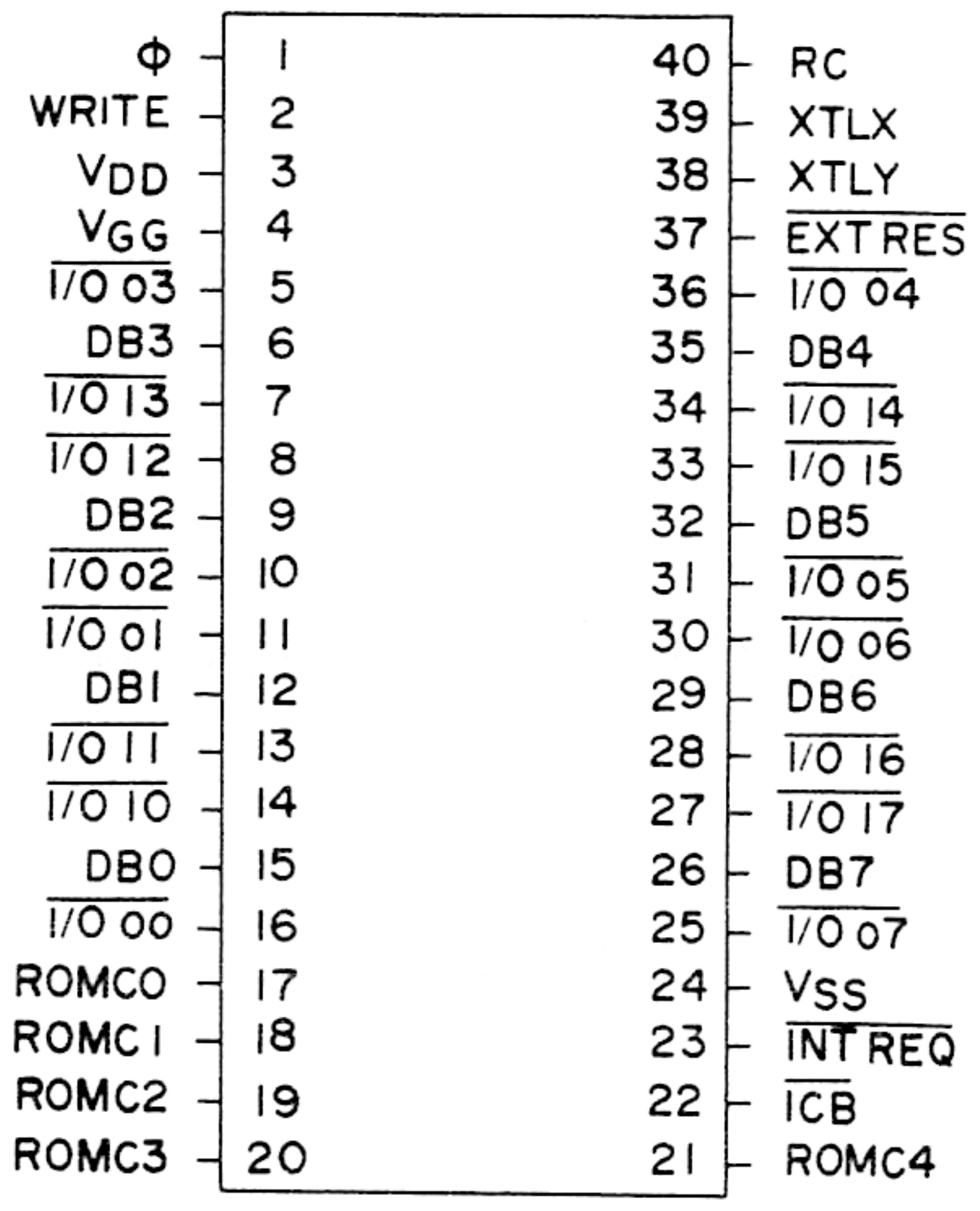

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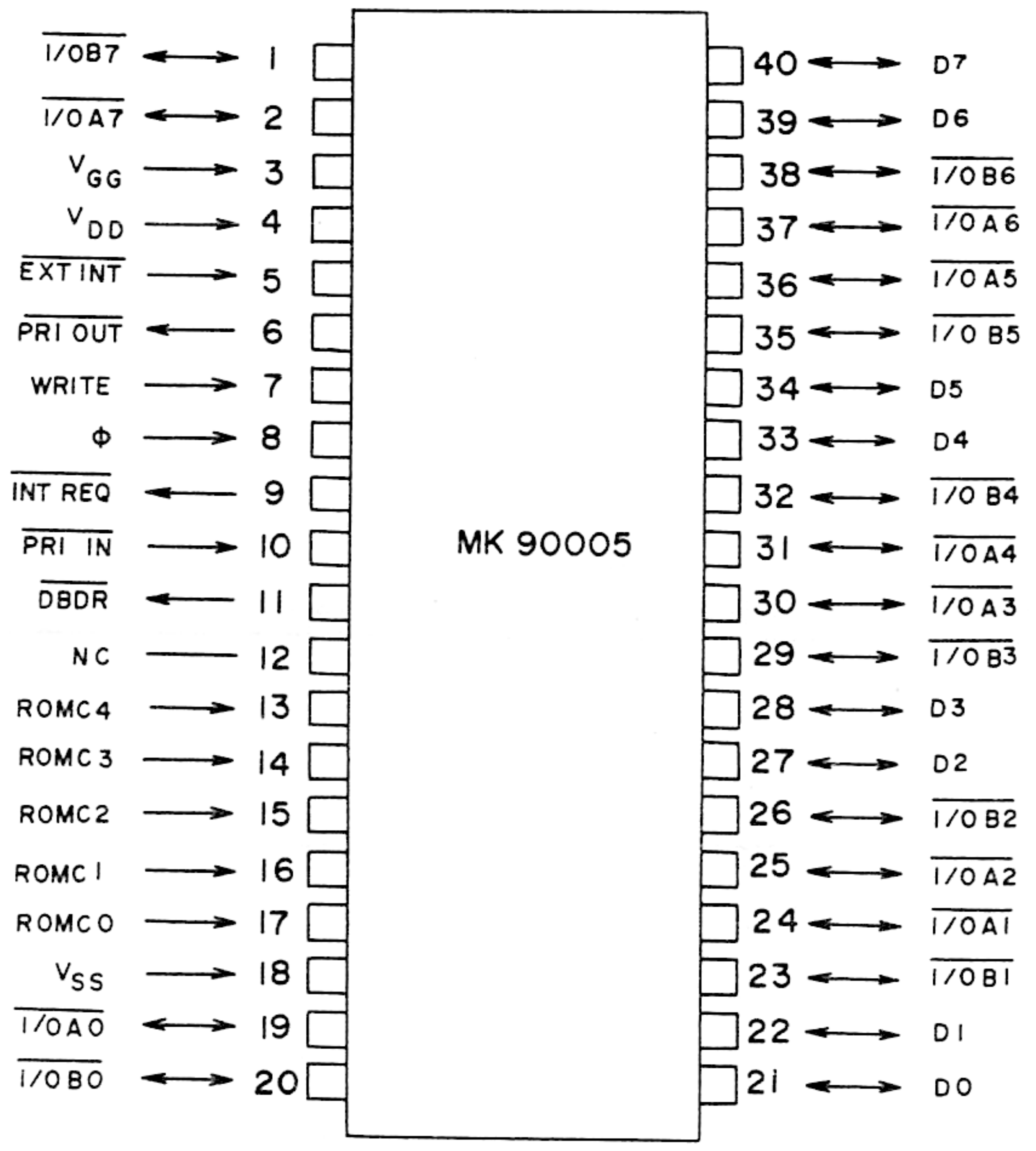

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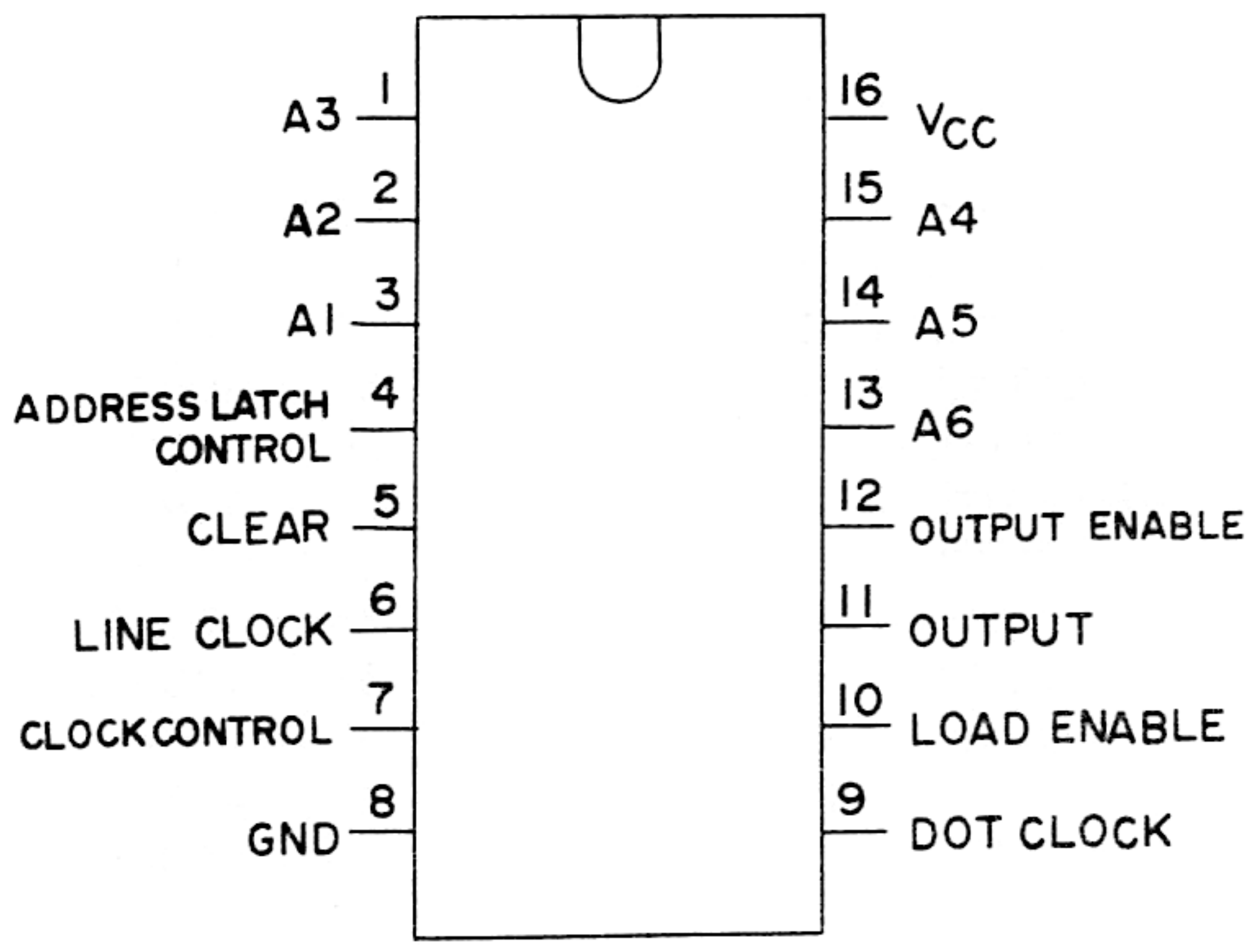

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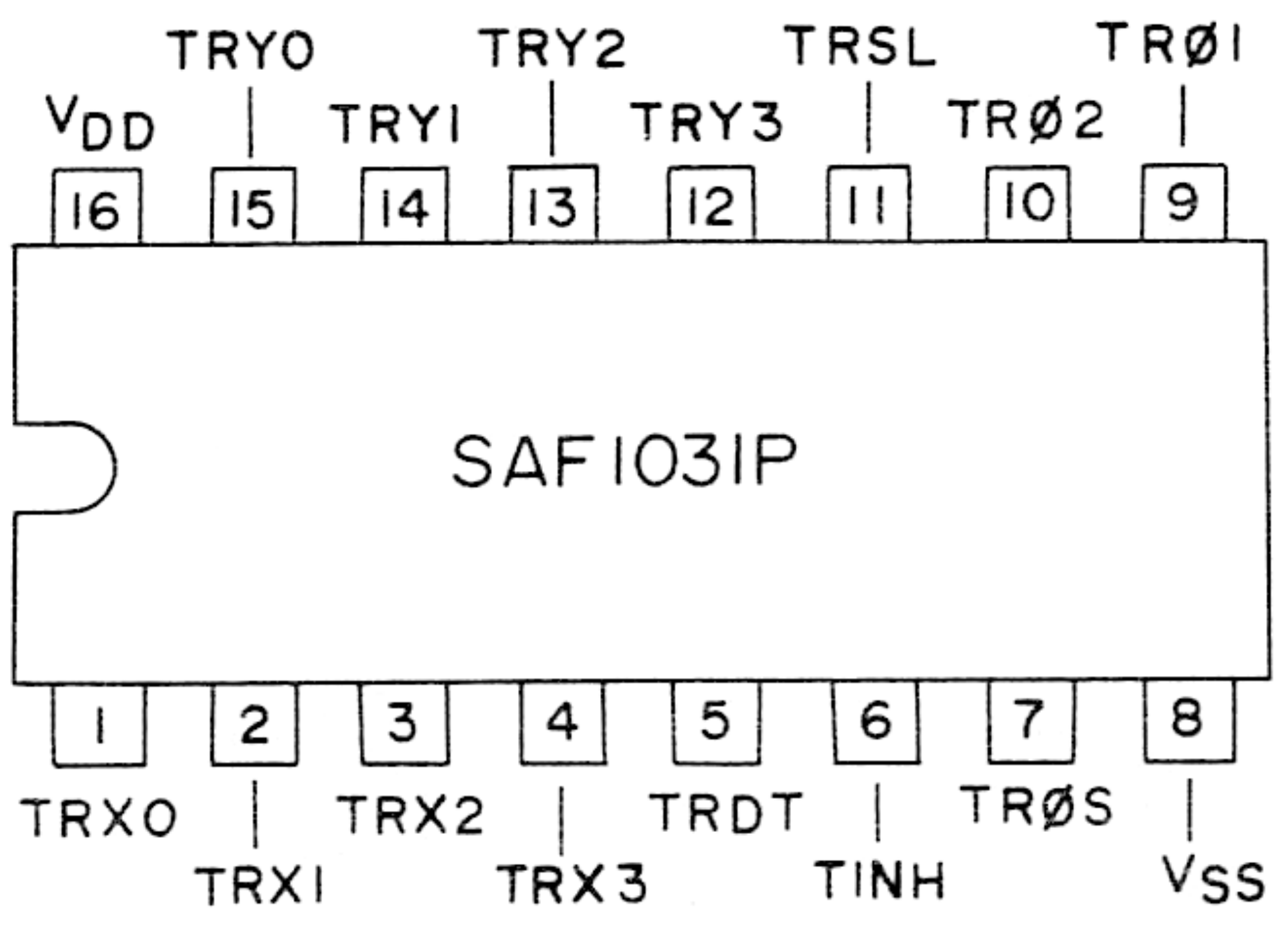

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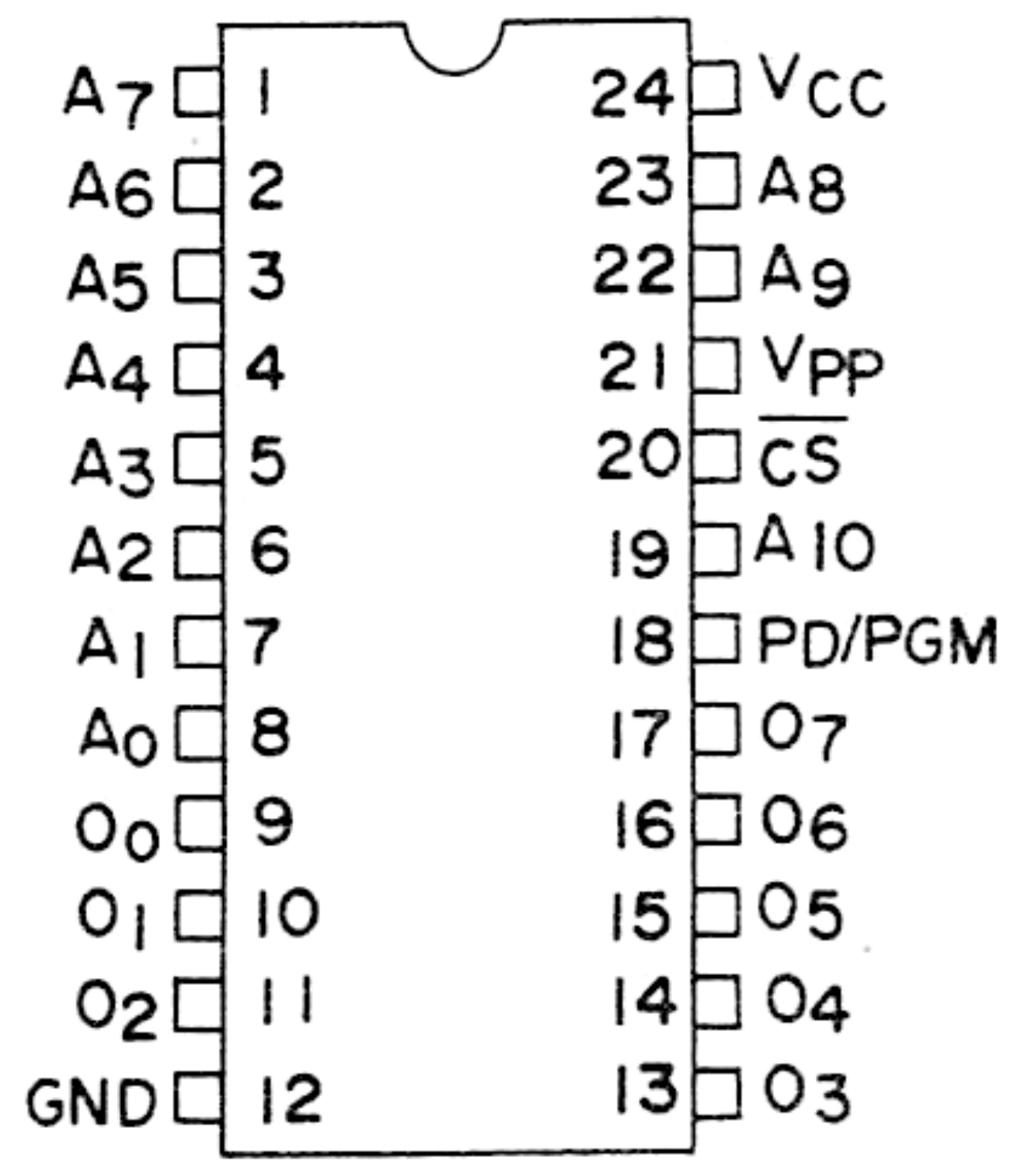

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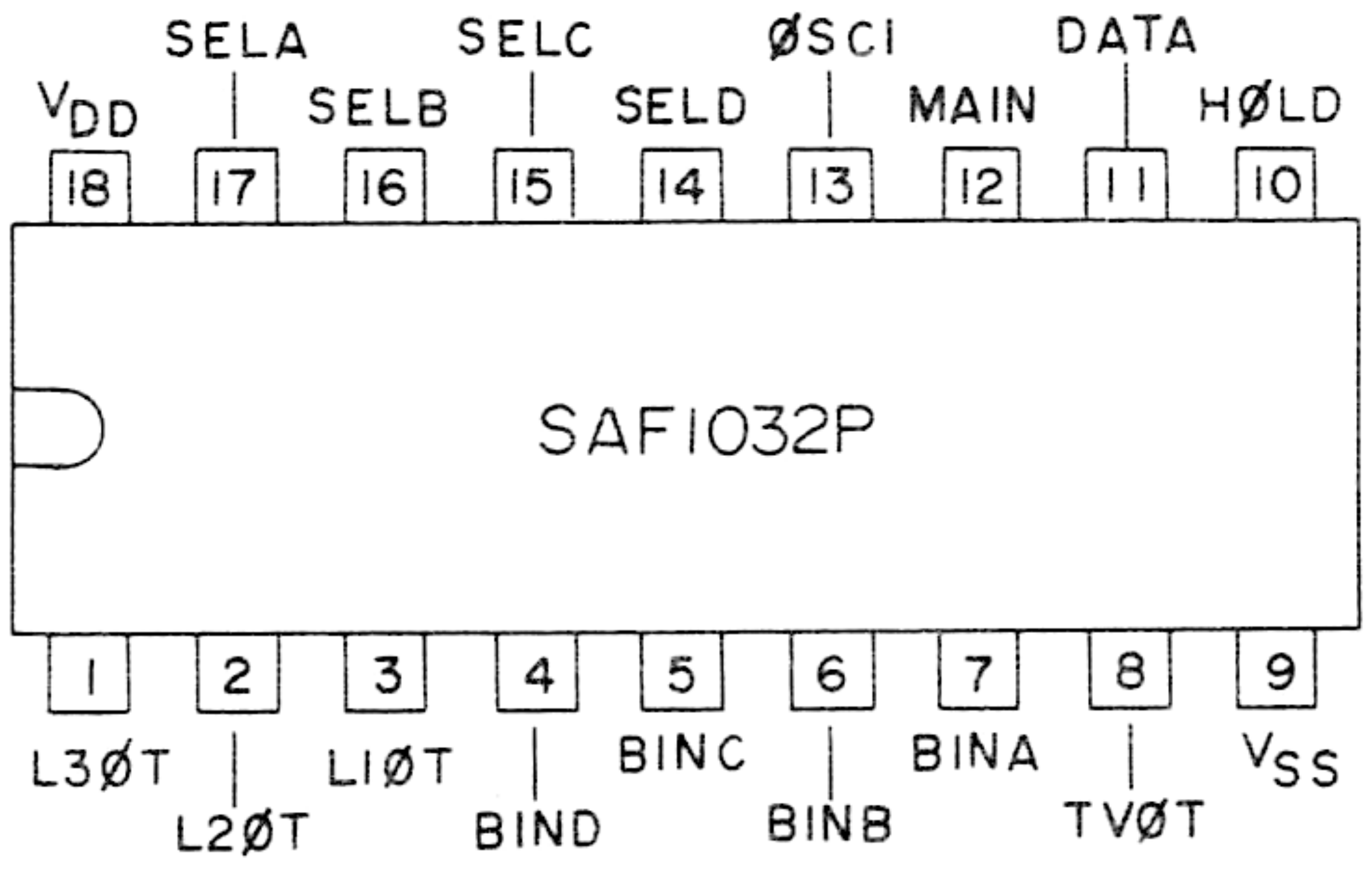

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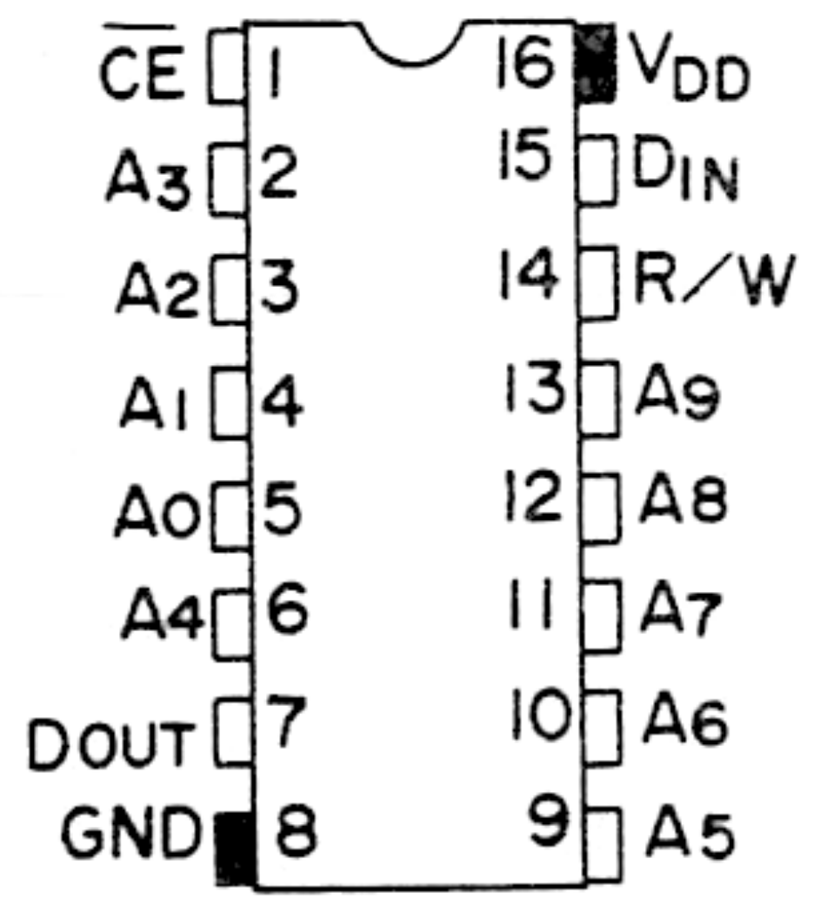

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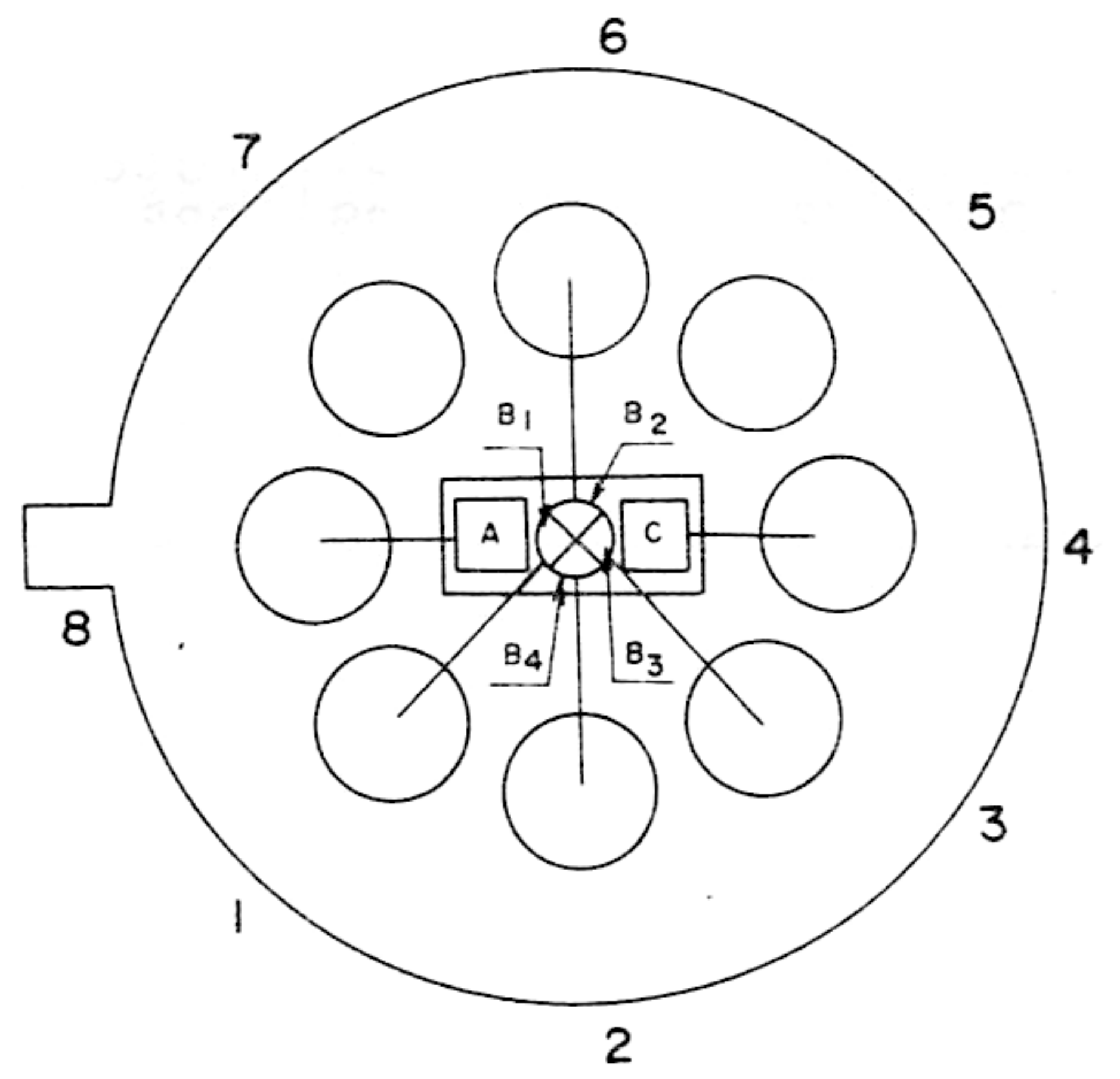

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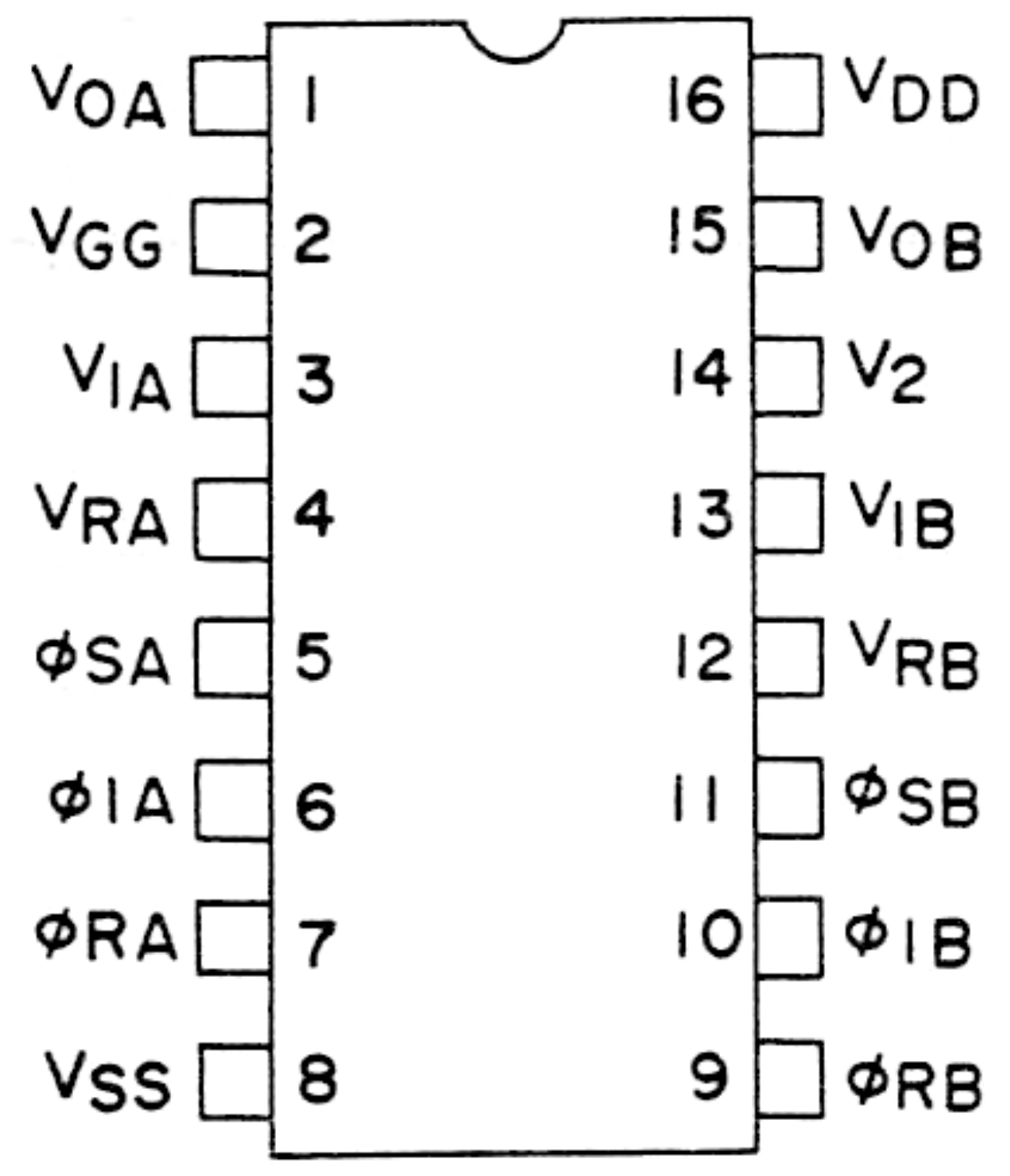


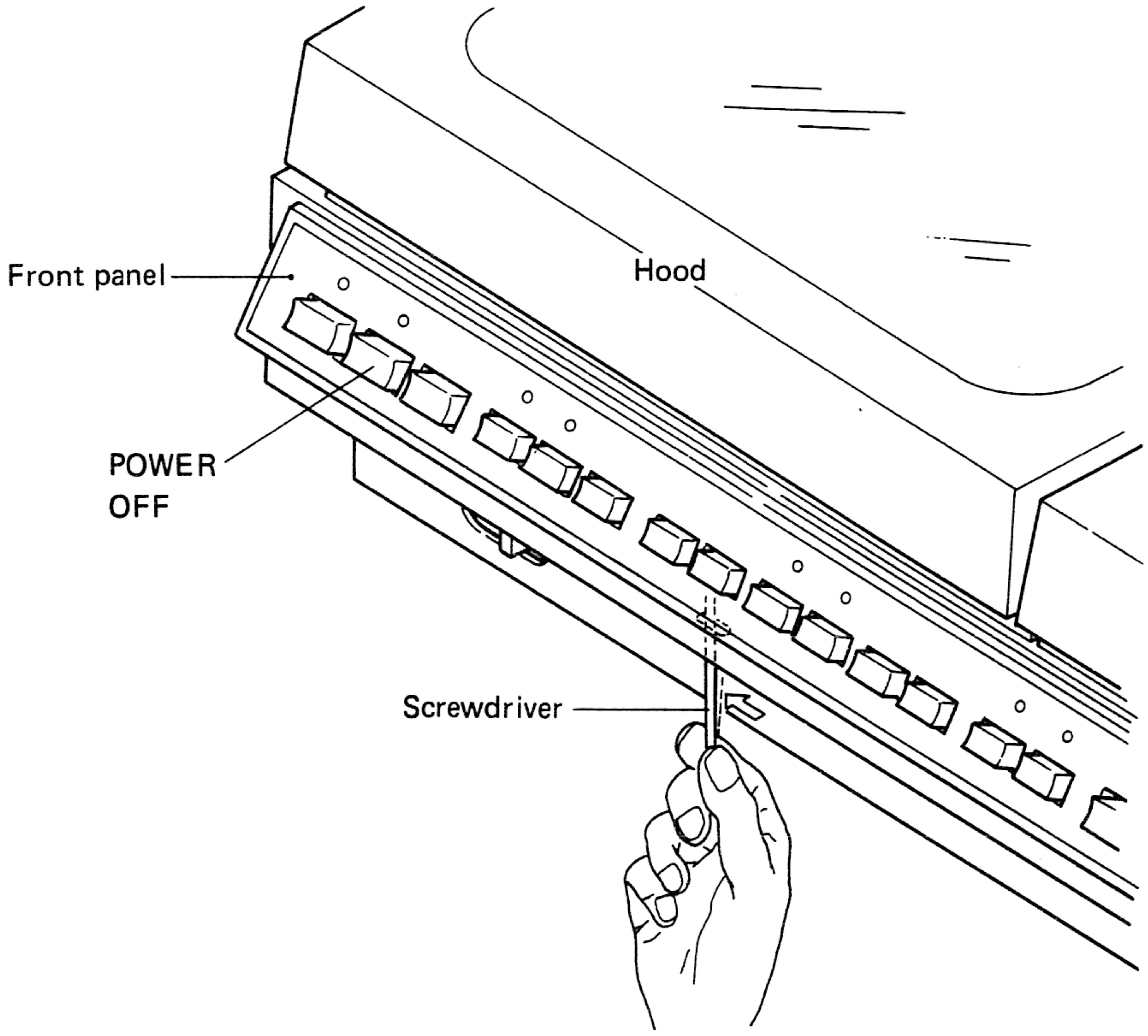
21. HOW TO OPEN THE HOOD UNDER NO POWER SOURCE

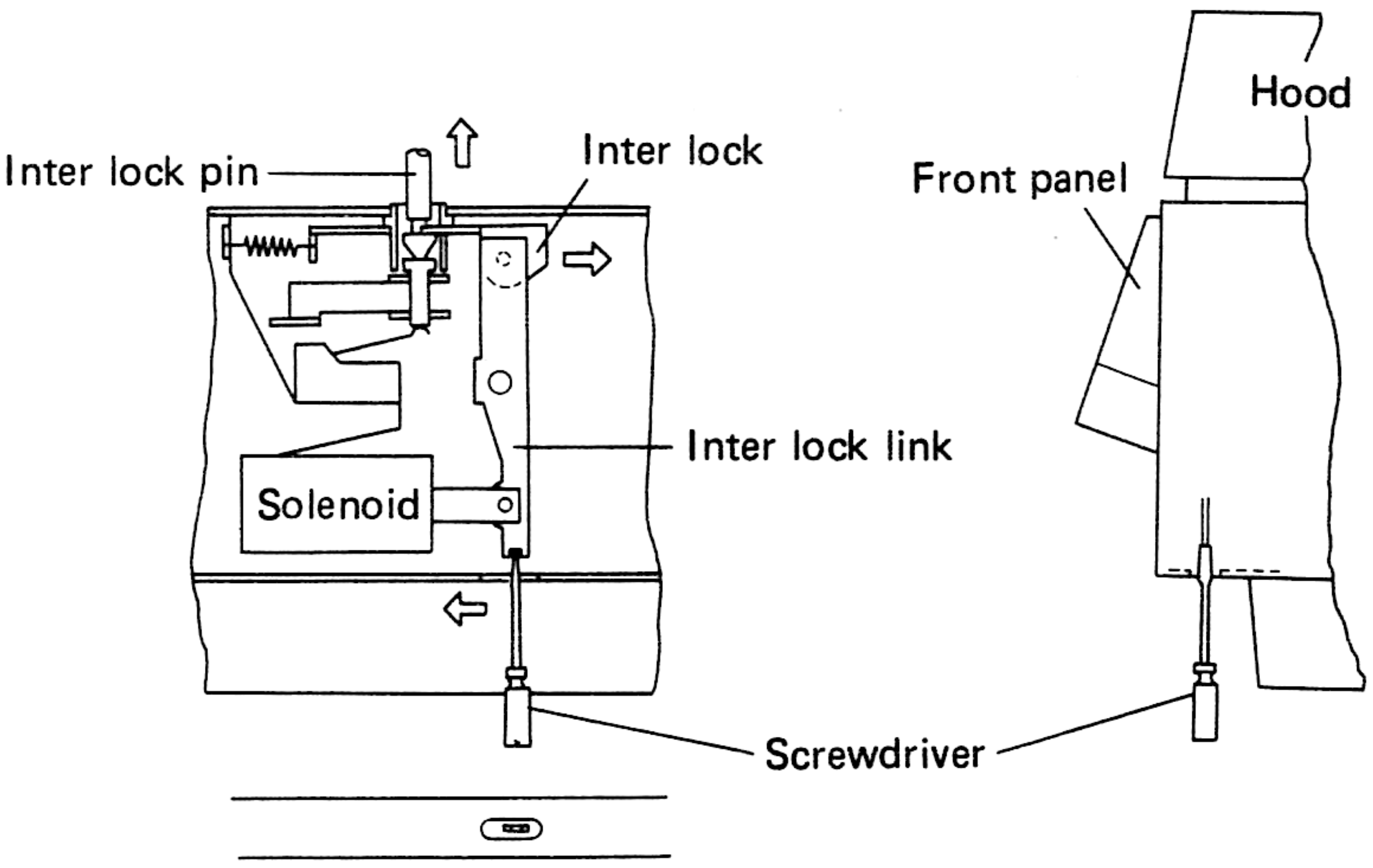
PR-7820s hood can't be opened unless power switch is turned on.

If it is necessary for servicing, you can open it without power supply through the following method shown below.

Put a screwdriver (less than 3, minus) into the slot under the front panel.

Then, move the interlock linkage to the left until hood lock to be unlocked.



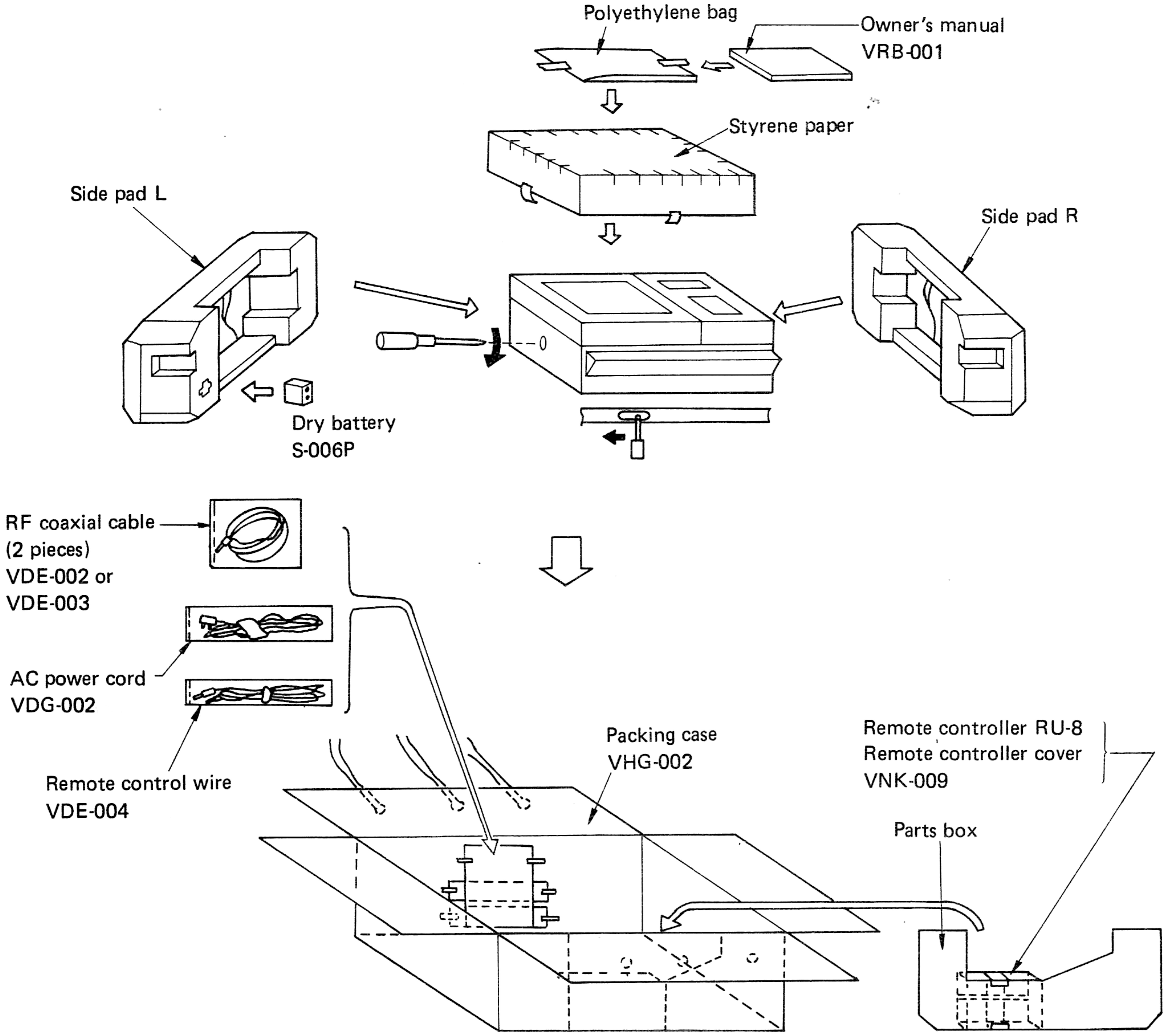


22. PACKING

1. Referring to page 205, move the interlock linkage and open the hood.
2. Holding the spindle motor (disc clamper) with one hand, turn the carriage stopper clockwise with a minus screwdriver (about 9 turns), and clamp the spindle motor.

NOTES:

- *Take care not to injure around the hole when clamping the spindle motor.*
- *Don't turn on the power with the spindle motor clamped, or the carriage motor will be damaged. It causes the trouble of the mechanism for the carriage motor when moving the player without clamping.*
- *Parts without part number cannot be supplied.*



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